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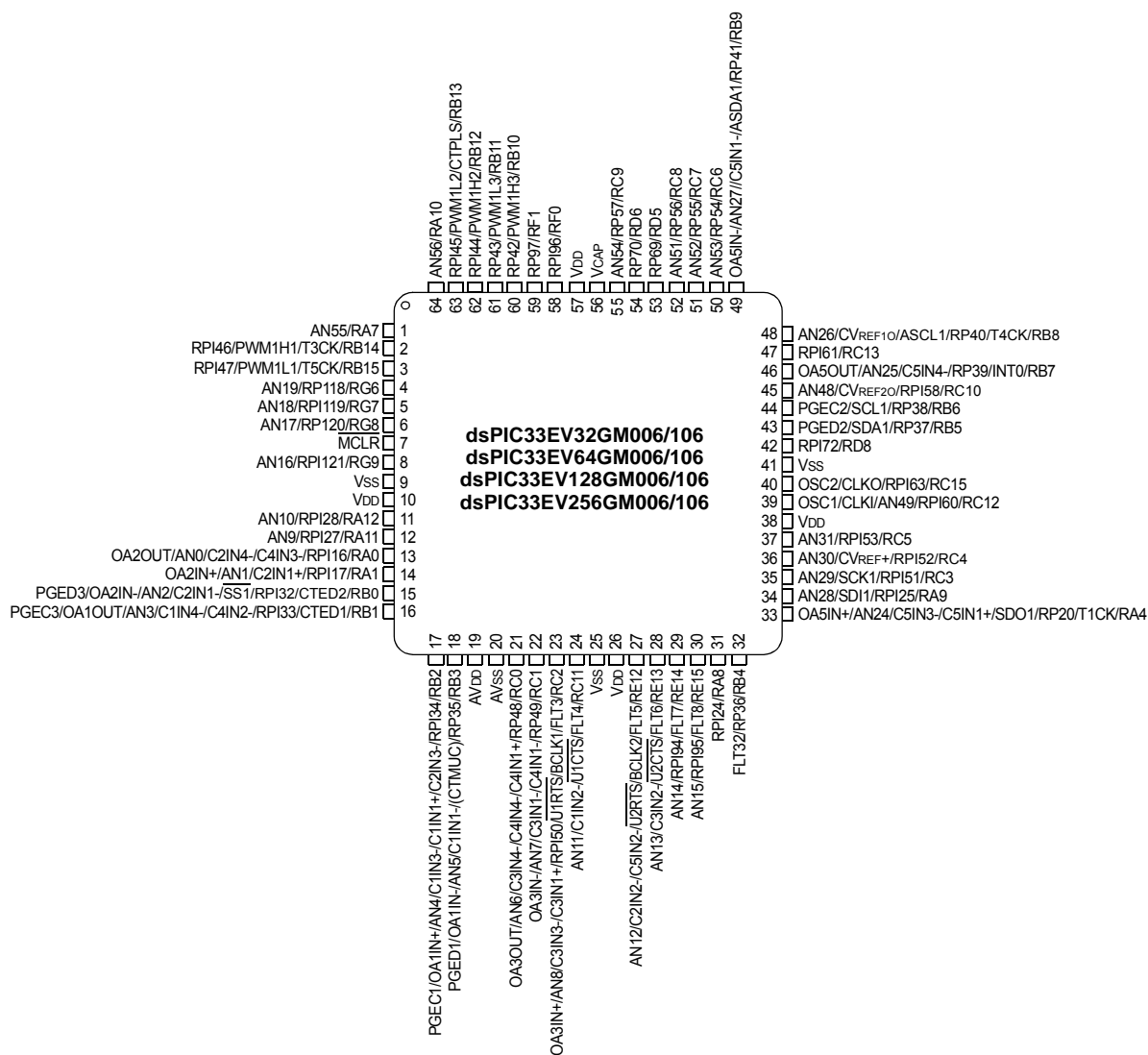
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm102-e-ss

dsPIC33EVXXXGM00X/10X FAMILY

Pin Diagrams (Continued)

64-Pin TQFP^(1,2,3)



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.5 “Peripheral Pin Select (PPS)”** for available peripherals and information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

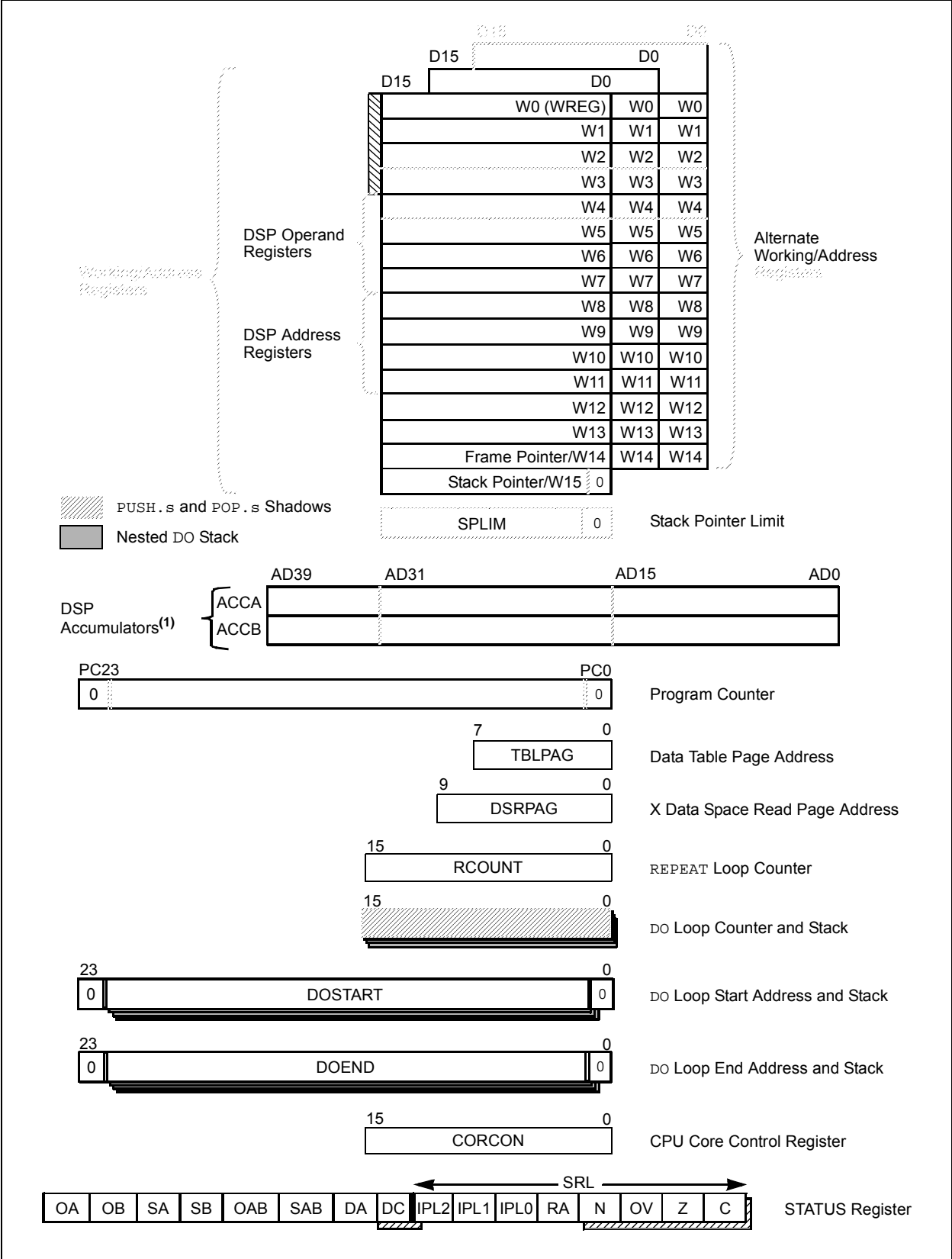
dsPIC33EVXXXGM00X/10X FAMILY

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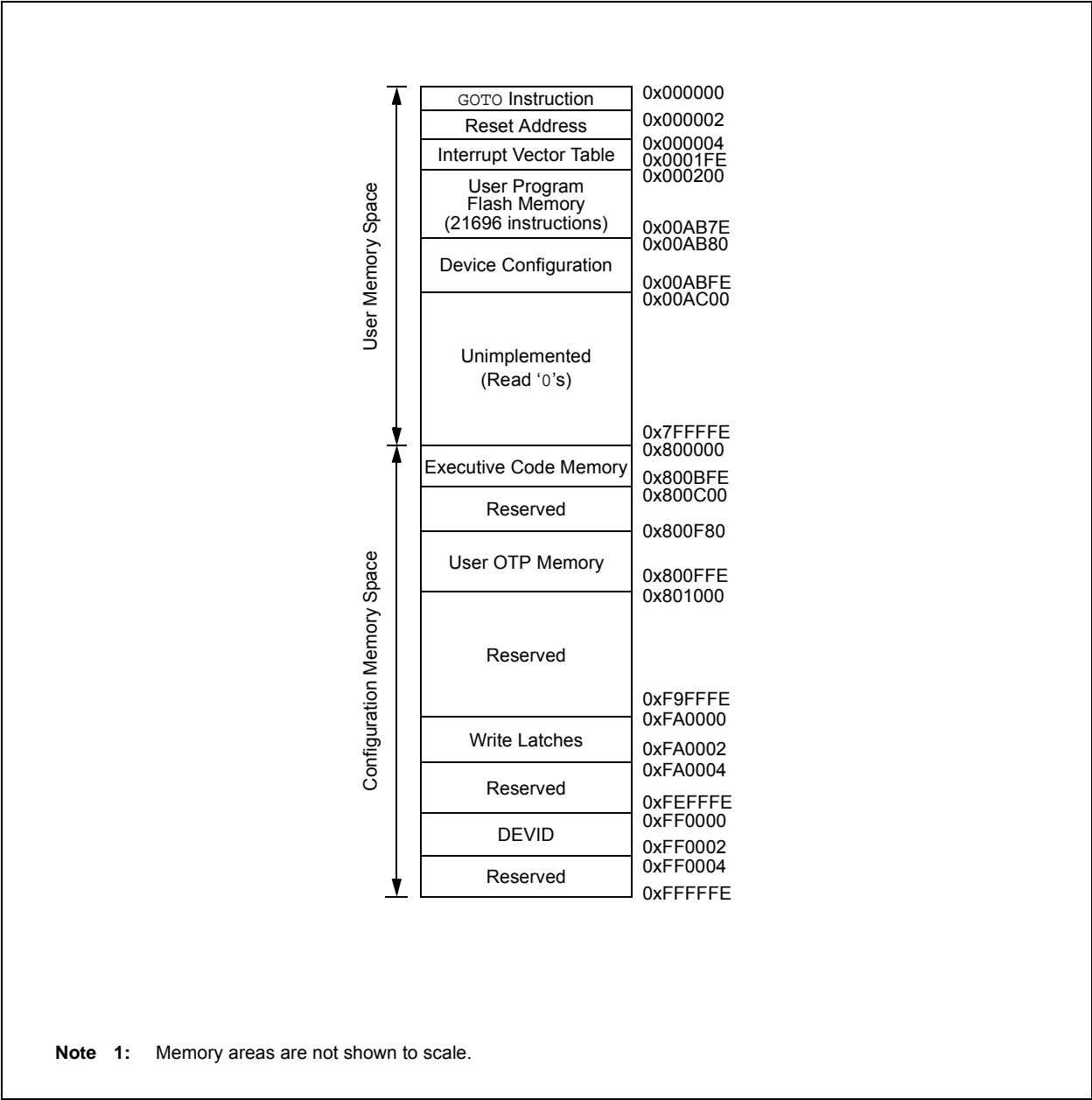
dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 3-2: PROGRAMMER'S MODEL



dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EV64GM00X/10X DEVICES⁽¹⁾



4.2.5 X AND Y DATA SPACES

The dsPIC33EVXXXGM00X/10X family core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified, linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X DS is used by all instructions and supports all addressing modes. The X DS has separate read and write data buses. The X read data bus is the read data path for all instructions that view the DS as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y DS is used in concert with the X DS by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSA, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to the X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

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REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit

1 = DMA3STB register is selected

0 = DMA3STA register is selected

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit

1 = DMA2STB register is selected

0 = DMA2STA register is selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit

1 = DMA1STB register is selected

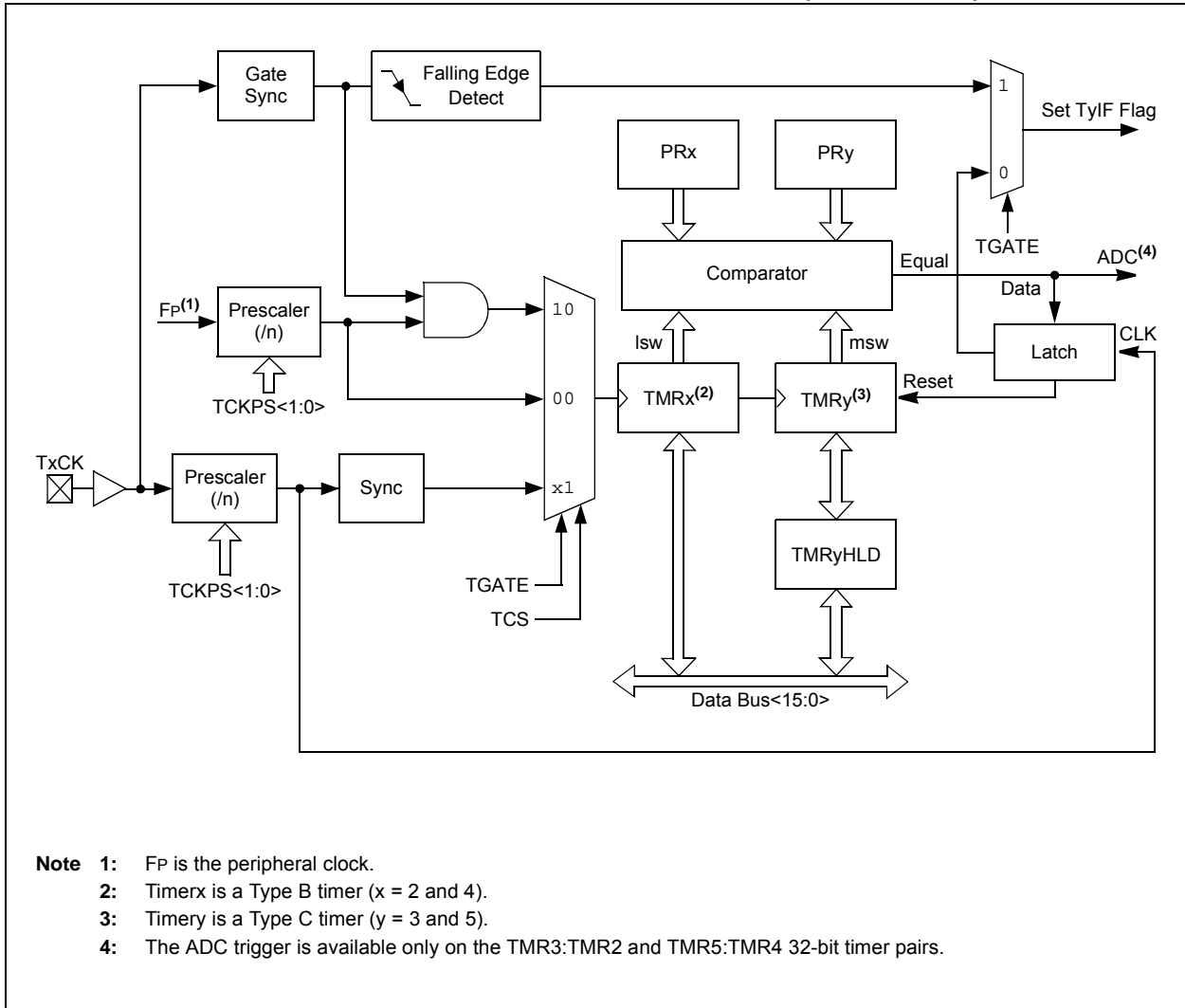
0 = DMA1STA register is selected

bit 0 **PPST0:** Channel 0 Ping-Pong mode Status Flag bit

1 = DMA0STB register is selected

0 = DMA0STA register is selected

FIGURE 13-3: TYPE B/TIME C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

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18.2 SPI Control Registers

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0
bit 15						bit 8	

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		C = Clearable bit

- bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the SPIx module and configures SCKx, SDOx, SDIx and \overline{SSx} as serial port pins
0 = Disables the SPIx module
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the SPIx module operation when the device enters Idle mode
0 = Continues the SPIx module operation in Idle mode
- bit 12-11 **Unimplemented:** Read as '0'
- bit 10-8 **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers are pending.
Slave mode:
Number of SPIx transfers are unread.
- bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = The SPIx Shift register is empty and ready to send or receive the data
0 = The SPIx Shift register is not empty
- bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = Overflow has not occurred
- bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty
- bit 4-2 **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
110 = Interrupt when the last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one data is shifted into SPIxSR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data is available in the SPIx receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the SPIx receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

19.0 INTER-INTEGRATED CIRCUIT (I²C)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Inter-Integrated Circuit™ (I²C™)**” (DS70000195) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains one Inter-Integrated Circuit (I²C) module, I2C1.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard, with a 16-bit interface.

The I²C module has the following 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I²C module offers the following key features:

- I²C Interface Supporting Both Master and Slave modes of Operation
- I²C Slave mode Supports 7 and 10-Bit Addressing
- I²C Master mode Supports 7 and 10-Bit Addressing
- I²C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I²C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- Support for Address Bit Masking up to Lower 7 Bits
- I²C Slave Enhancements:
 - SDAx hold time selection of SMBus (300 ns or 150 ns)
 - Start/Stop bit interrupt enables

Figure 19-1 shows a block diagram of the I²C module.

19.1 I²C Baud Rate Generator

The Baud Rate Generator (BRG) used for I²C mode operation is used to set the SCL clock frequency for 100 kHz, 400 kHz and 1 MHz. The BRG reload value is contained in the I2CxBRG register. The BRG will automatically begin counting on a write to the I2CxTRN register.

Equation 19-1 and Equation 19-2 provide the BRG reload formula and F_{SCL} frequency, respectively.

EQUATION 19-1: BRG FORMULA

$$I2CxBRG = \left(\left(\frac{1}{F_{SCL}} - Delay \right) \times \frac{F_{CY}}{2} \right) - 2$$

Where:

Delay varies from 110 ns to 130 ns.

EQUATION 19-2: F_{SCL} FREQUENCY

$$F_{SCL} = F_{CY} / ((I2CxBRG + 2) * 2)$$

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NOTES:

24.2 ADC Helpful Tips

1. The SMP1x control bits in the ADxCON2 registers:
 - a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the ADxCON2 register is set to '1', this determines when the ADC analog scan channel list, defined in the ADxCSSL/ADxCSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using the DMA peripheral.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMP1x bits and the condition described in 1.c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADCxBUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUX A selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. For configuration examples, refer to **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be ‘1111 1111 1111 1111’. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ‘1’s to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

28.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EV instruction set is almost identical to that of the dsPIC30F and dsPIC33F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into following five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the Status Flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have the following three operands:

- The first source operand, which is typically a register ‘Wb’ without any address modifier
- The second source operand, which is typically a register ‘Ws’ with or without an address modifier
- The destination of the result, which is typically a register ‘Wd’ with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value ‘f’
- The destination, which could be either the file register ‘f’ or the W0 register, which is denoted as ‘WREG’

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of ‘Ws’ or ‘f’)
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register ‘Wb’)

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by ‘k’)
- The W register or file register where the literal value is to be loaded (specified by ‘Wb’ or ‘f’)

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register ‘Wb’ without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register ‘Wd’ with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register ‘Wn’ or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for
Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICKit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,
Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

**FIGURE 30-23: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING CHARACTERISTICS**

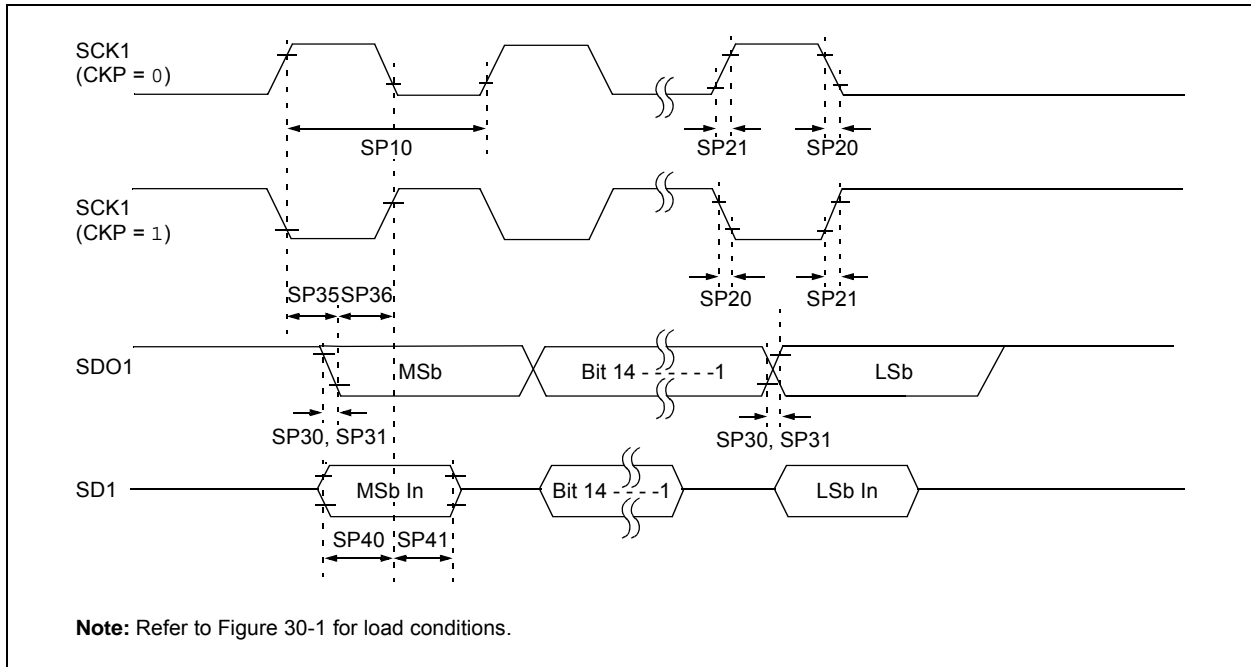
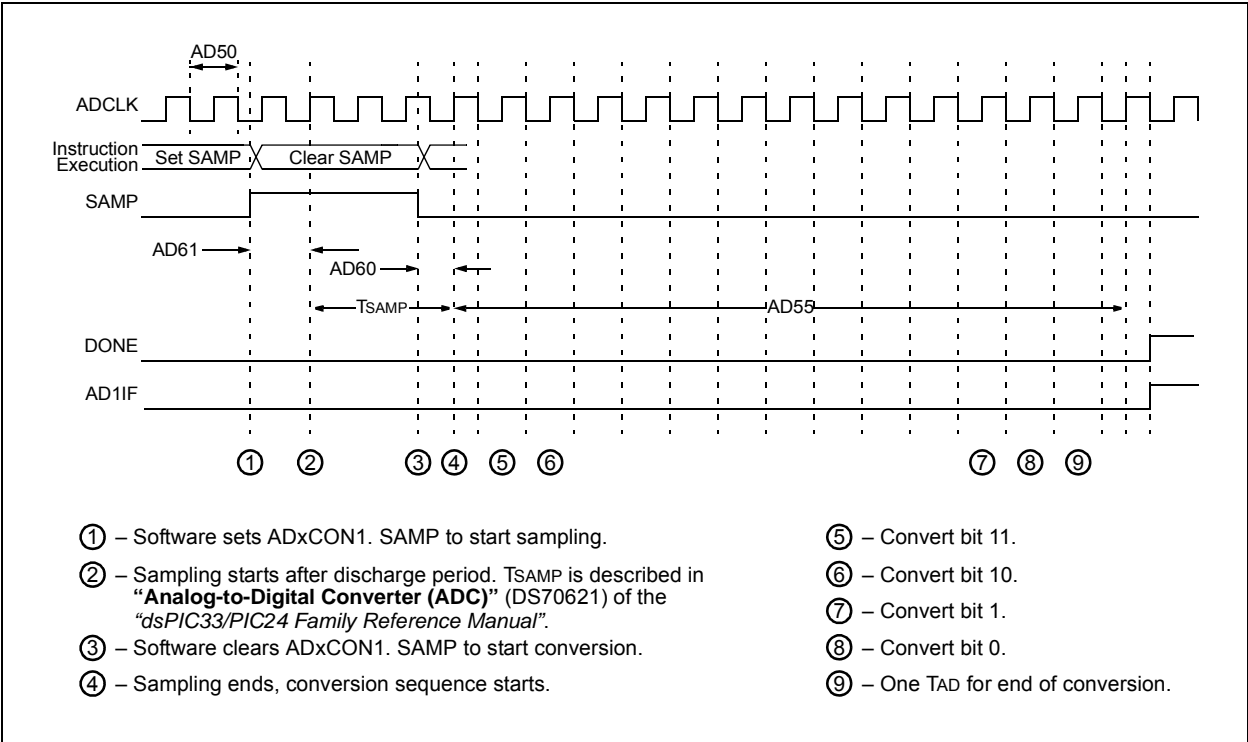


FIGURE 30-34: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS
(ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



32.19 ADC Gain Offset Error

FIGURE 32-49: TYPICAL ADC GAIN ERROR vs. TEMPERATURE

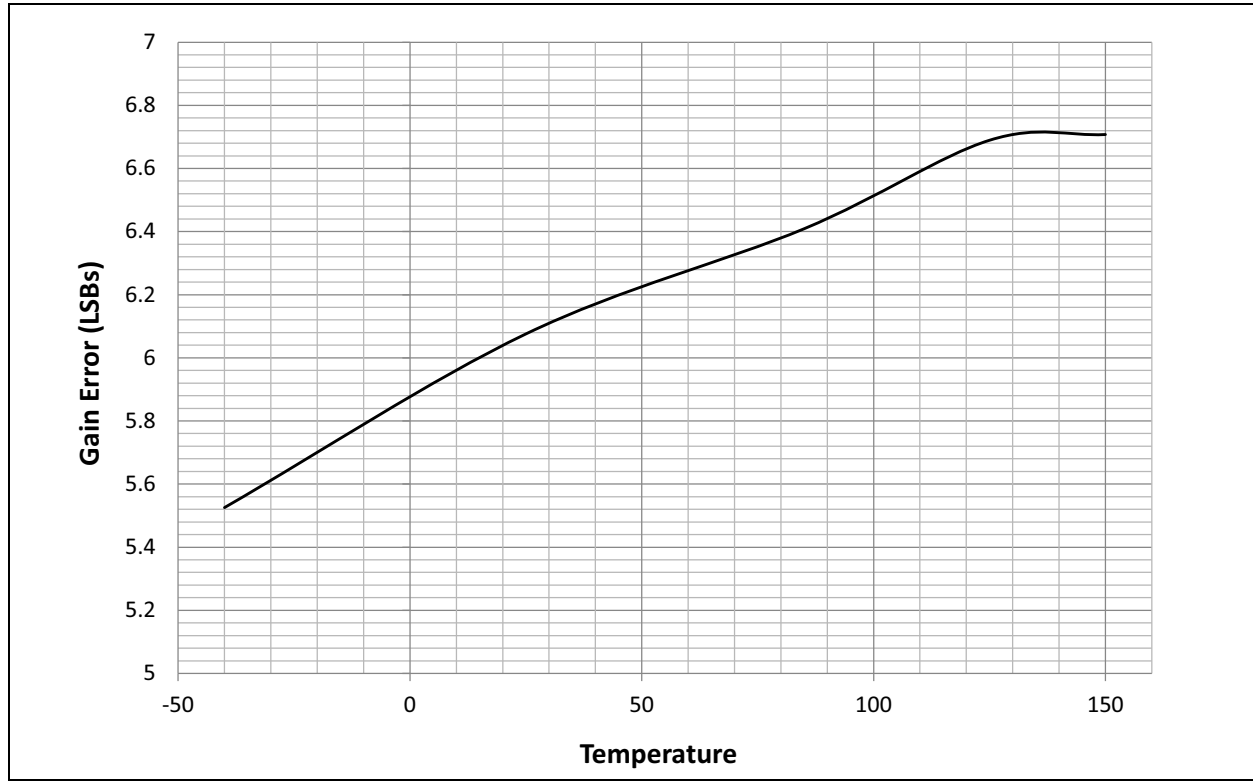
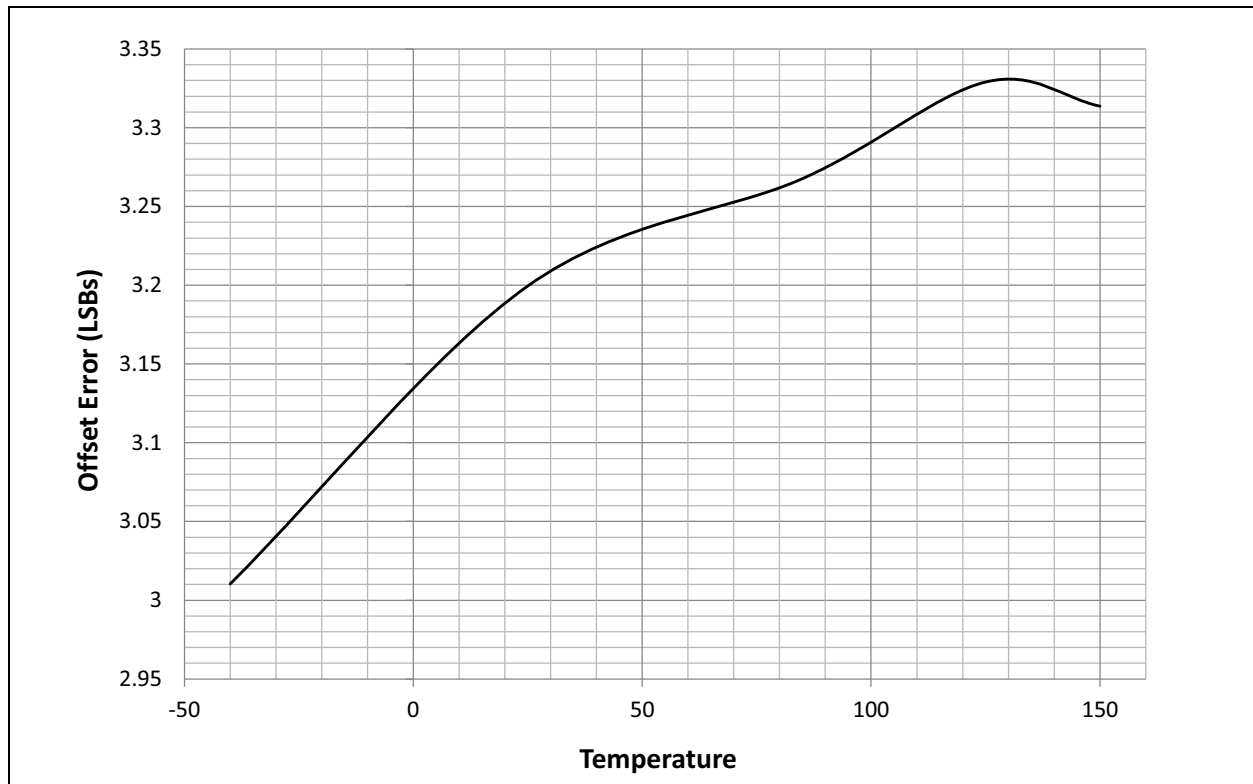


FIGURE 32-50: TYPICAL ADC OFFSET ERROR vs. TEMPERATURE



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FIGURE 33-7: TYPICAL I_{IDLE} vs. V_{DD} (EC MODE, 20 MIPS)

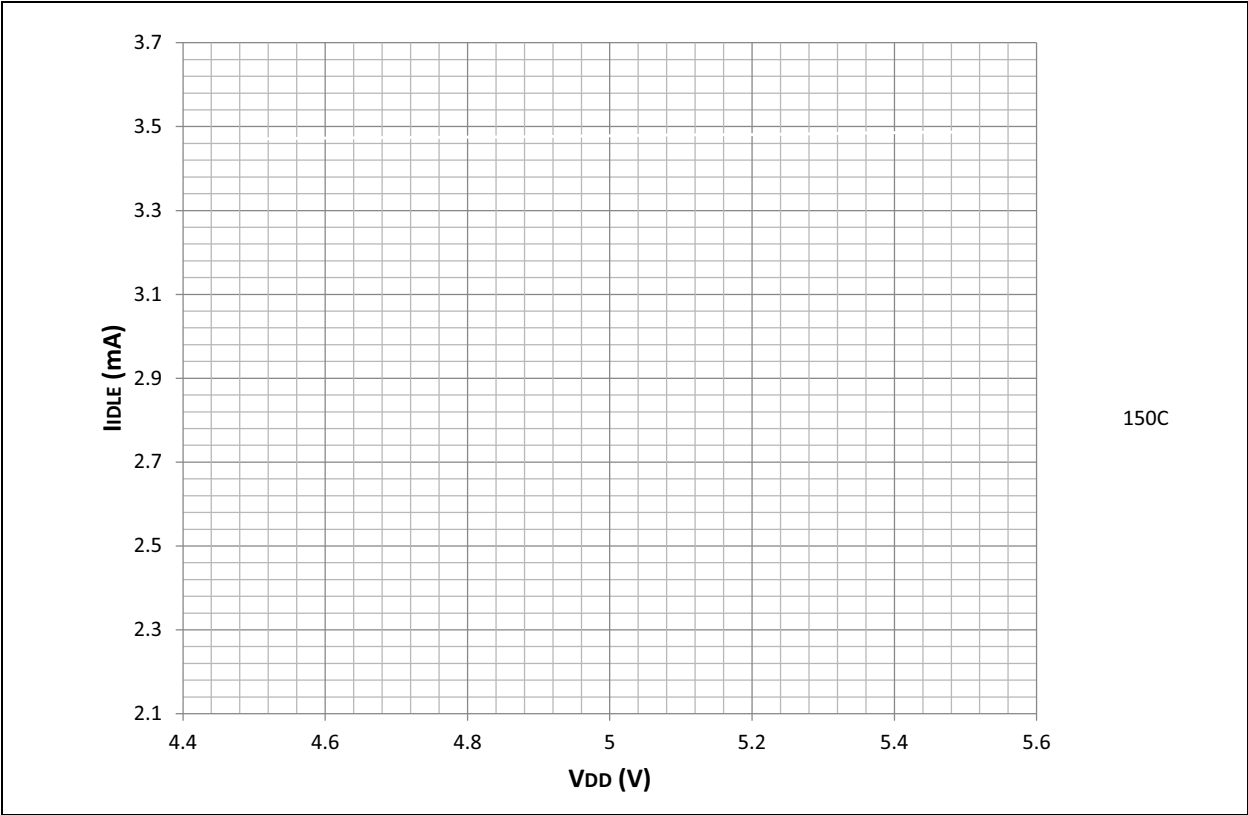
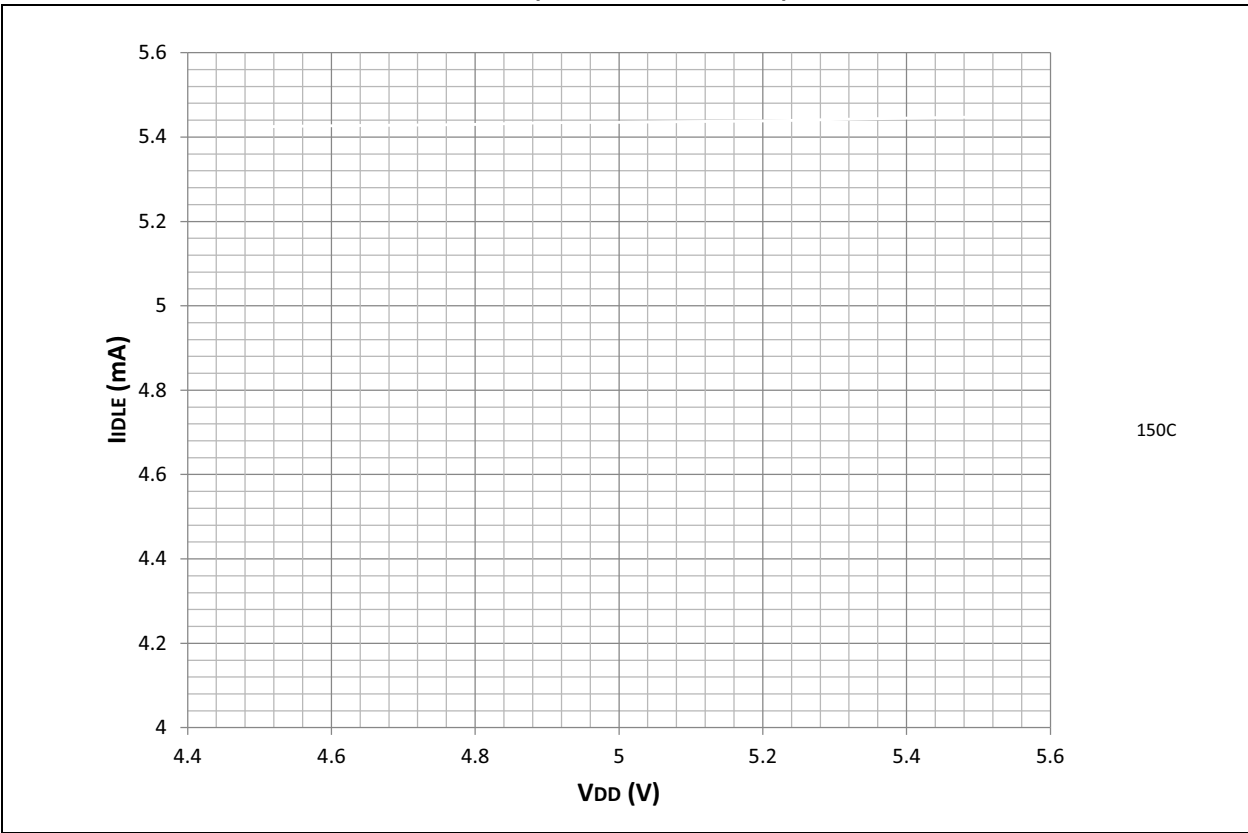


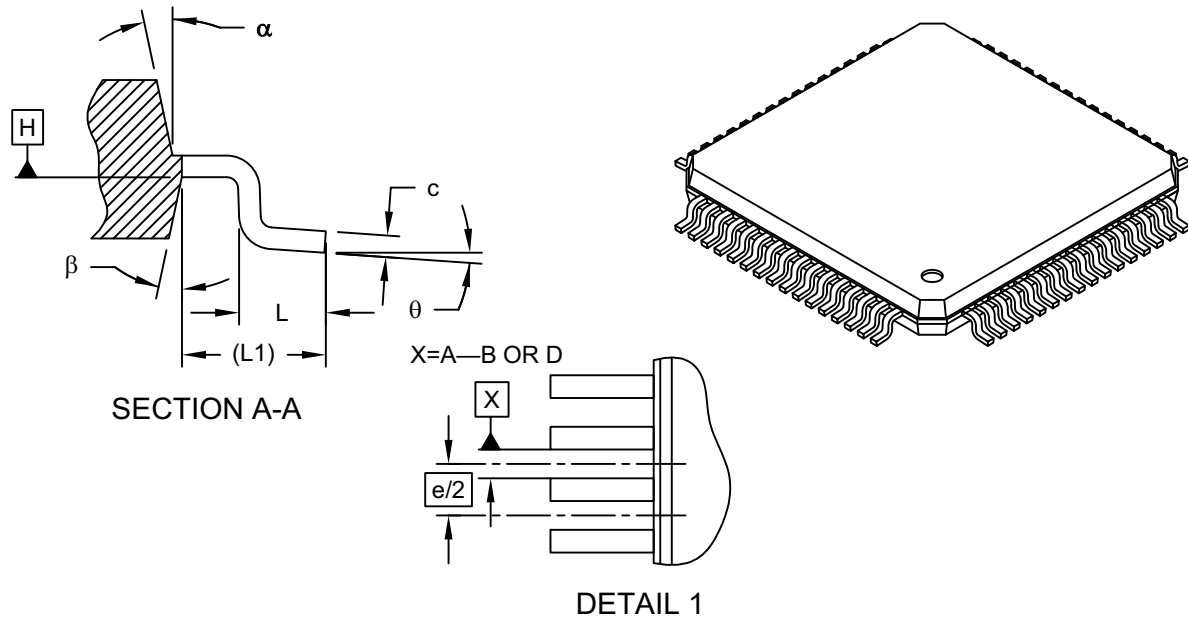
FIGURE 33-8: TYPICAL I_{IDLE} vs. V_{DD} (EC MODE, 40 MIPS)



dsPIC33EVXXXGM00X/10X FAMILY

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	64		
Lead Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2