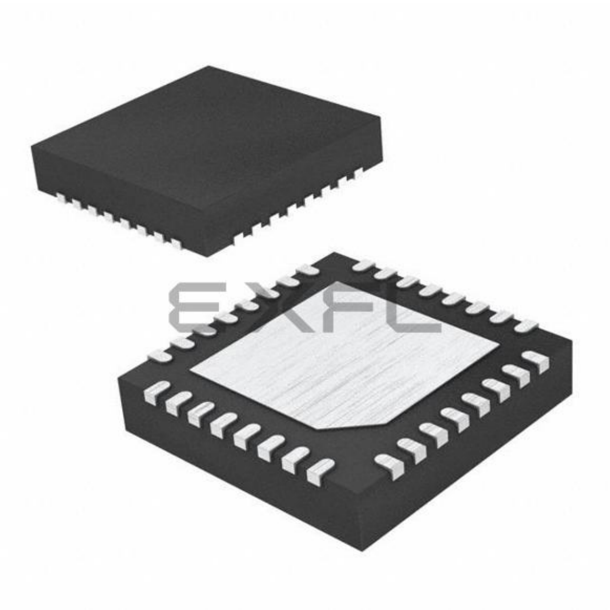





## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 256KB (85.5K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 11x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-VQFN Exposed Pad |
| Supplier Device Package | 28-QFN-S (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm102t-i-mm |

## TABLE 4-3: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC1CON1 | 0140 | — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — | — | ICI1 | ICI0 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC1CON2 | 0142 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000D |
| IC1BUF | 0144 | Input Capture 1 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC1TMR | 0146 | Input Capture 1 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC2CON1 | 0148 | — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — | — | ICI1 | ICI0 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC2CON2 | 014A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000D |
| IC2BUF | 014C | Input Capture 2 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC2TMR | 014E | Input Capture 2 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC3CON1 | 0150 | — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — | — | ICI1 | ICI0 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC3CON2 | 0152 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000D |
| IC3BUF | 0154 | Input Capture 3 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC3TMR | 0156 | Input Capture 3 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC4CON1 | 0158 | — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — | — | ICI1 | ICI0 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 | 0000 |
| IC4CON2 | 015A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000D |
| IC4BUF | 015C | Input Capture 4 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC4TMR | 015E | Input Capture 4 Timer Register | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

## TABLE 4-4: I2C1 REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I2C1CON1 | 0200 | I2CEN | — | I2CSIDL | SCLREL | STRICT | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C1CON2 | 0202 | — | — | — | — | — | — | — | — | — | PCIE | SCIE | BOEN | SDAHT | SBCDE | AHEN | DHEN | 1000 |
| I2C1STAT | 0204 | ACKSTAT | TRSTAT | ACKTIM | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C1ADD | 0206 | — | — | — | — | — | — | I2C1 Address Register | | | | | | | | | | 0000 |
| I2C1MSK | 0208 | — | — | — | — | — | — | I2C1 Address Mask Register | | | | | | | | | | 0000 |
| I2C1BRG | 020A | Baud Rate Generator Register | | | | | | | | | | | | | | | | 0000 |
| I2C1TRN | 020C | — | — | — | — | — | — | — | — | I2C1 Transmit Register | | | | | | | | 00FF |
| I2C1RCV | 020E | — | — | — | — | — | — | — | — | I2C1 Receive Register | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

### TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1BUFPNT1 | 0420 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 | 0000 |
| C1BUFPNT2 | 0422 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C1BUFPNT3 | 0424 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C1BUFPNT4 | 0426 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C1RXM0SID | 0430 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM0EID | 0432 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM1EID | 0436 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM2EID | 043A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF0EID | 0442 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF1EID | 0446 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF2EID | 044A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF3EID | 044E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF4EID | 0452 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF5EID | 0456 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF6EID | 045A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF7EID | 045E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF8EID | 0462 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF9EID | 0466 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF10EID | 046A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**FIGURE 4-16: BIT-REVERSED ADDRESSING EXAMPLE**

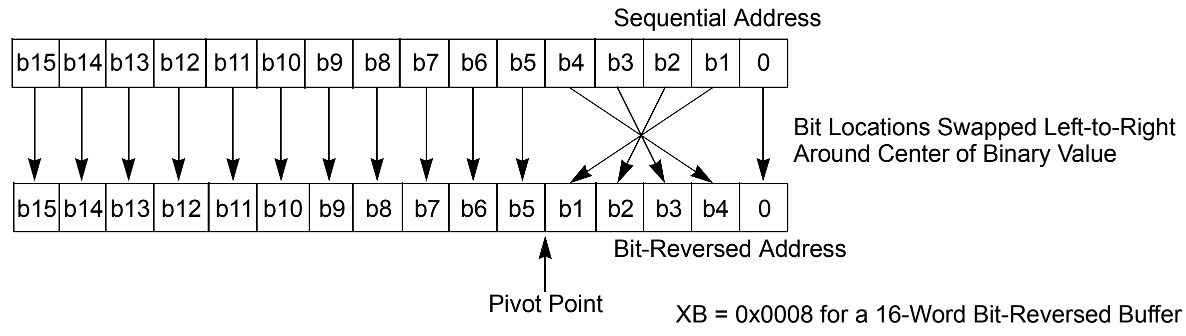



**TABLE 4-46: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)**

| Normal Address | | | | | Bit-Reversed Address | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **A3** | **A2** | **A1** | **A0** | **Decimal** | **A3** | **A2** | **A1** | **A0** | **Decimal** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 0 | 4 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 14 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 | 3 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 1 | 0 | 14 | 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 15 |

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel or channels are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA Channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

**TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS**

| Peripheral to DMA Association | DMAxREQ Register IRQSEL<7:0> Bits | DMAxPAD Register (Values to Read from Peripheral) | DMAxPAD Register (Values to Write to Peripheral) |
|---|---|---|---|
| External Interrupt 0 (INT0) | 00000000 | — | — |
| Input Capture 1 (IC1) | 00000001 | 0x0144 (IC1BUF) | — |
| Input Capture 2 (IC2) | 00000101 | 0x014C (IC2BUF) | — |
| Input Capture 3 (IC3) | 00100101 | 0x0154 (IC3BUF) | — |
| Input Capture 4 (IC4) | 00100110 | 0x015C (IC4BUF) | — |
| Output Compare 1 (OC1) | 00000010 | — | 0x0906 (OC1R)<br>0x0904 (OC1RS) |
| Output Compare 2 (OC2) | 00000110 | — | 0x0910 (OC2R)<br>0x090E (OC2RS) |
| Output Compare 3 (OC3) | 00011001 | — | 0x091A (OC3R)<br>0x0918 (OC3RS) |
| Output Compare 4 (OC4) | 00011010 | — | 0x0924 (OC4R)<br>0x0922 (OC4RS) |
| Timer2 (TMR2) | 00000111 | — | — |
| Timer3 (TMR3) | 00001000 | — | — |
| Timer4 (TMR4) | 00011011 | — | — |
| Timer5 (TMR5) | 00011100 | — | — |
| SPI1 Transfer Done | 00001010 | 0x0248 (SPI1BUF) | 0x0248 (SPI1BUF) |
| SPI2 Transfer Done | 00100001 | 0x0268 (SPI2BUF) | 0x0268 (SPI2BUF) |
| UART1 Receiver (UART1RX) | 00001011 | 0x0226 (U1RXREG) | — |
| UART1 Transmitter (UART1TX) | 00001100 | — | 0x0224 (U1TXREG) |
| UART2 Receiver (UART2RX) | 00011110 | 0x0236 (U2RXREG) | — |
| UART2 Transmitter (UART2TX) | 00011111 | — | 0x0234 (U2TXREG) |
| RX Data Ready (CAN1) | 00100010 | 0x0440 (C1RXD) | — |
| TX Data Request (CAN1) | 01000110 | — | 0x0442 (C1TXD) |
| ADC1 Convert Done (ADC1) | 00001101 | 0x0300 (ADC1BUF0) | — |

### REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLT2R7 | FLT2R6 | FLT2R5 | FLT2R4 | FLT2R3 | FLT2R2 | FLT2R1 | FLT2R0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLT1R7 | FLT1R6 | FLT1R5 | FLT1R4 | FLT1R3 | FLT1R2 | FLT1R1 | FLT1R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **FLT2R<7:0>:** Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to VSS

bit 7-0 **FLT1R<7:0>:** Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to VSS

## 13.0 TIMER2/3 AND TIMER4/5

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

**Note:** For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

**Note:** Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

### REGISTER 14-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STEP2<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** DMT Clear Timer bits

`00001000` = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if preceded by the correct loading of the STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H register and observing the counter being reset.

All Other Write Patterns = Sets the BAD2 bit; the value of STEP1<7:0> will remain unchanged and the new value being written to STEP2<7:0> will be captured. These bits are cleared when a DMT Reset event occurs.

### REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER

| HS-0, HC | HS-0, HC | HS-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC1 | DTC0 | DTCP(3) | — | — | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = Fault interrupt is not pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = Current-limit interrupt is not pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = Trigger interrupt is not pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = Trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; else, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

### REGISTER 17-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled through the BCH and BCL bits in the LEBCONx register).
1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the state blank source
0010 = PWM2H is selected as the state blank source
0001 = PWM1H is selected as the state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits

The selected signal will enable and disable (Chop) the selected PWMx outputs.
1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the chop clock source
0010 = PWM2H is selected as the chop clock source
0001 = PWM1H is selected as the chop clock source
0000 = Chop clock generator is selected as the chop clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

### REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 **S:** I2Cx Start bit
Updated when Start, Reset or Stop is detected; cleared when the $I^2C$ module is disabled, I2CEN = 0.
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Indicates that a Start bit was not detected last

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)
1 = Read: Indicates that the data transfer is output from the slave
0 = Write: Indicates that the data transfer is input to the slave

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, the I2CxRCV bit is full
0 = Receive is not complete, the I2CxRCV bit is empty

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full (8 bits of data)
0 = Transmit is complete, I2CxTRN is empty

### REGISTER 19-4: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | MSK<9:8> | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MSK<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as ‘0’

bit 9-0 **MSK<9:0>:** I2Cx Mask for Address Bit x Select bits
1 = Enables masking for bit x of the incoming message address; bit match is not required in this position
0 = Disables masking for bit x; bit match is required in this position

### REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

### REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| | | | |
|---|---|---|---|
| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

**REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)**

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENn | TXABTn | TXLARBn | TXERRn | TXREQn | RTRENn | TXnPRI1 | TXnPRI0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENm | TXABTm(1) | TXLARBm(1) | TXERRm(1) | TXREQm | RTRENm | TXmPRI1 | TXmPRI0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 See Definition for bits 7-0, controls Buffer n.

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer, TRBm, is a transmit buffer
0 = Buffer, TRBm, is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

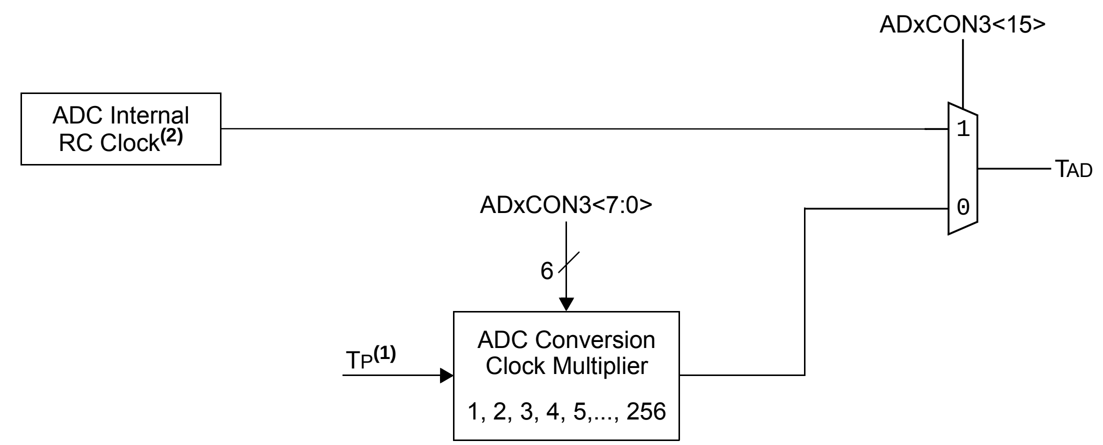
bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQm is set.

**Note:** The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

**FIGURE 24-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM**




**Note 1:** TP = 1/FP.

**2:** Refer to the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

**TABLE 30-35: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |
| SP60 | TssL2doV | SDO2 Data Output Valid after $\overline{SS2}$ Edge | — | — | 50 | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV,<br>TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH,<br>TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH,<br>TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL,<br>TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH,<br>TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH<br>TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

### TABLE 30-58: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(4)** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 75 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 | — | TAD | |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | Using simultaneous sampling |
| AD57a | TSAMP | Sample Time When Sampling Any ANx Input | 2 | — | — | TAD | |
| AD57b | TSAMP | Sample Time When Sampling the Op Amp Outputs | 4 | — | — | TAD | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger(2) | 2 | — | 3 | TAD | Auto-convert trigger is not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit(2) | 2 | — | 3 | TAD | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)(2) | — | 0.5 | — | TAD | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On(2) | — | — | 20 | μs | See **Note 3** |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

**2:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**3:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1<15>) = 1). During this time, the ADC result is indeterminate.

**4:** These parameters are characterized but not tested in manufacturing.

### TABLE 30-59: DMA MODULE TIMING REQUIREMENTS

| AC CHARACTERISTICS | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| DM1 | DMA Byte/Word Transfer Latency | 1 TCY(2) | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

FIGURE 32-3: TYPICAL IDD vs. VDD (EC MODE, 20 MIPS)

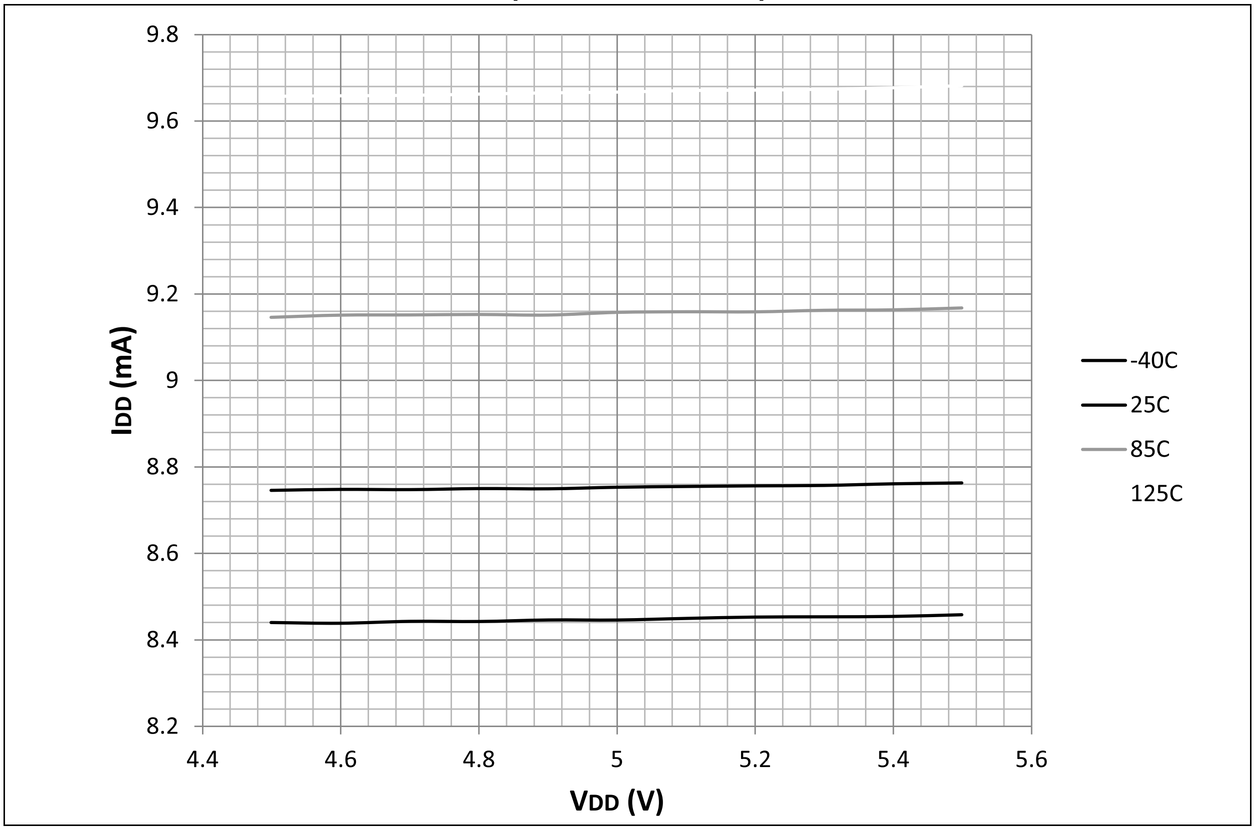
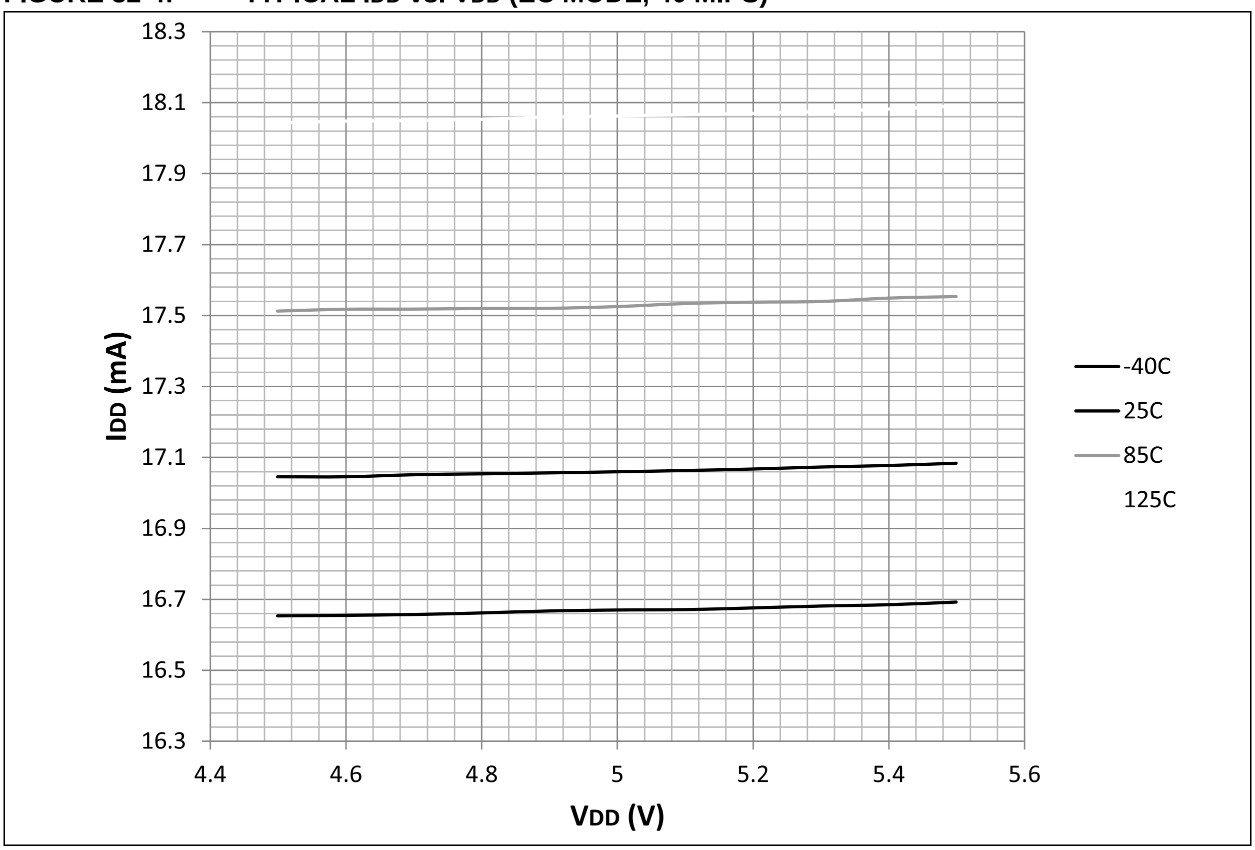



FIGURE 32-4: TYPICAL IDD vs. VDD (EC MODE, 40 MIPS)



## 32.4 IPD

FIGURE 32-17: TYPICAL IPD vs. VDD

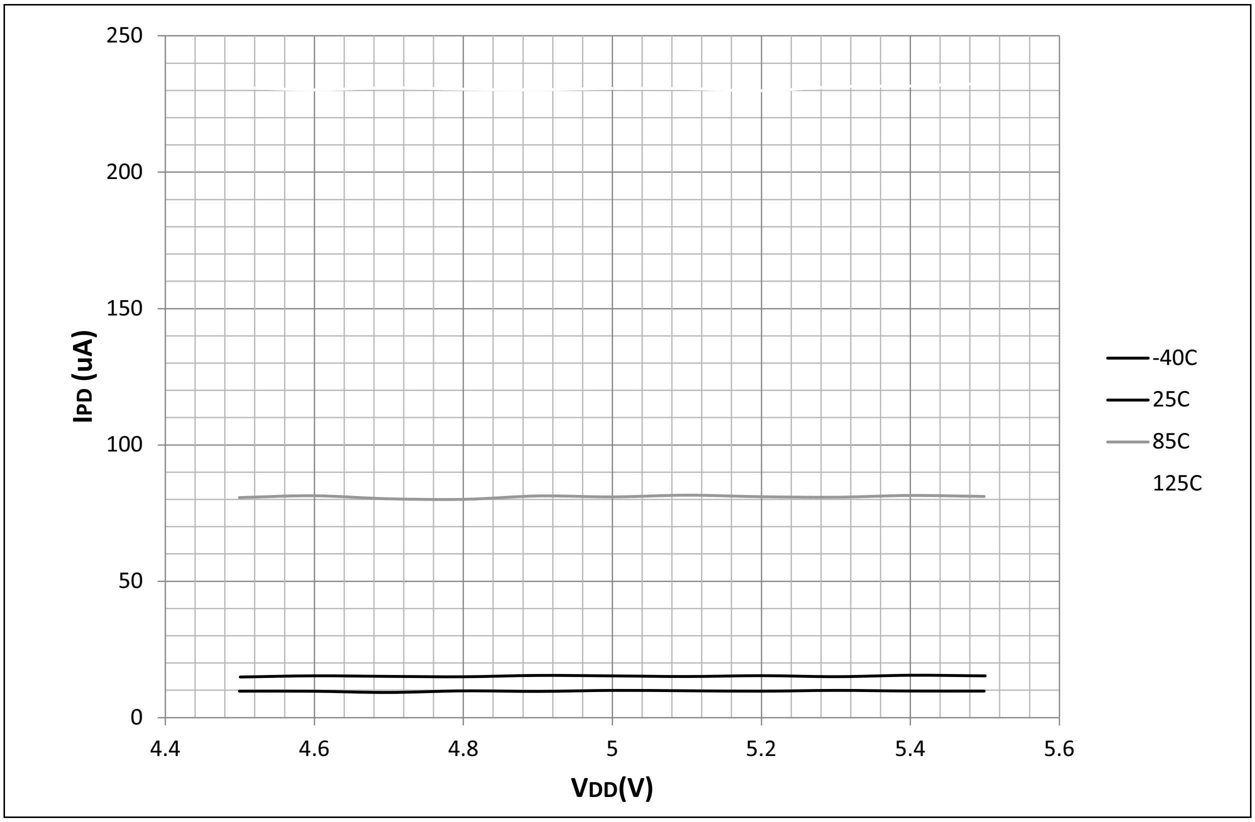



FIGURE 32-18: TYPICAL/MAXIMUM IPD vs. TEMPERATURE

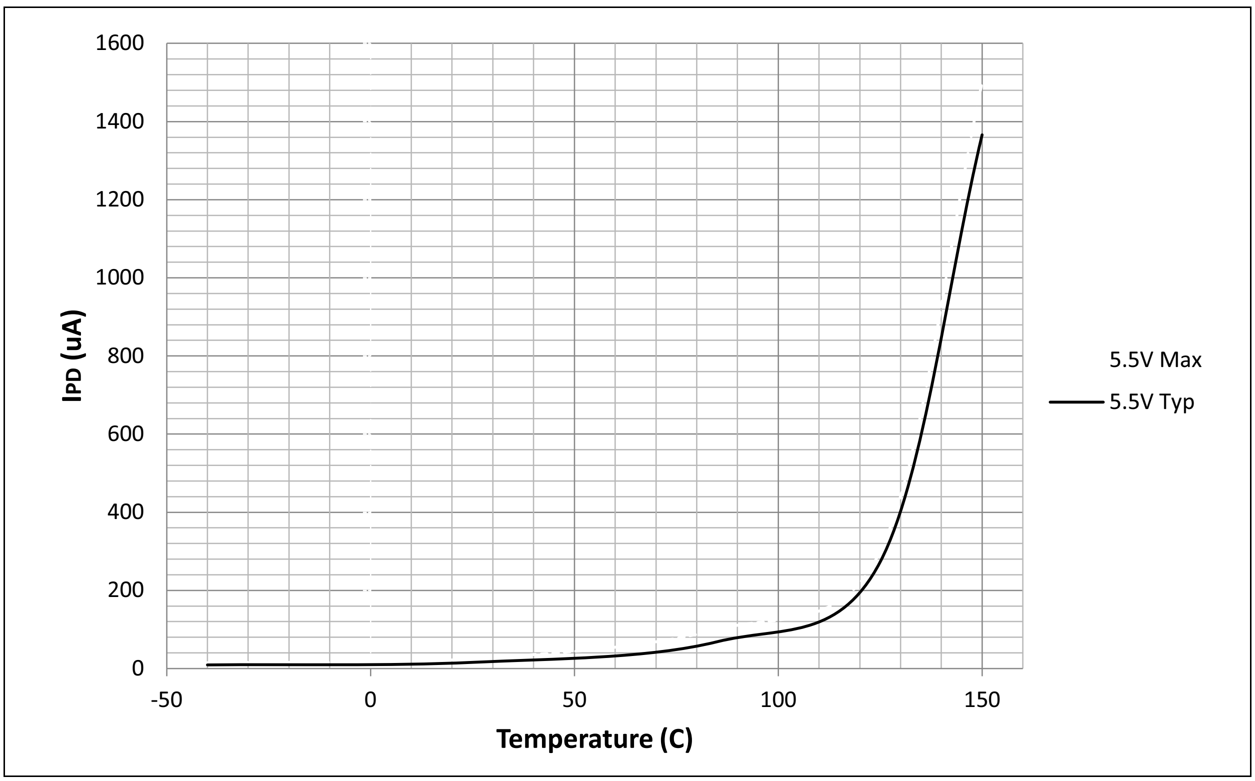
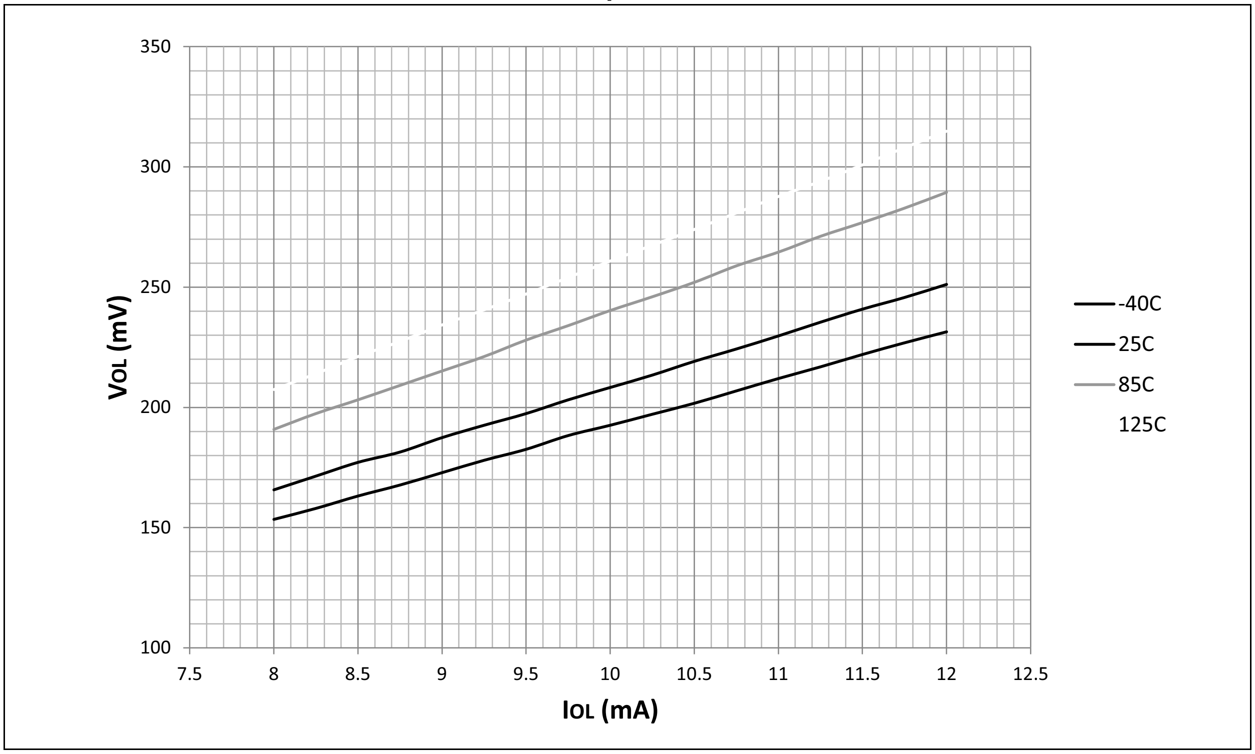
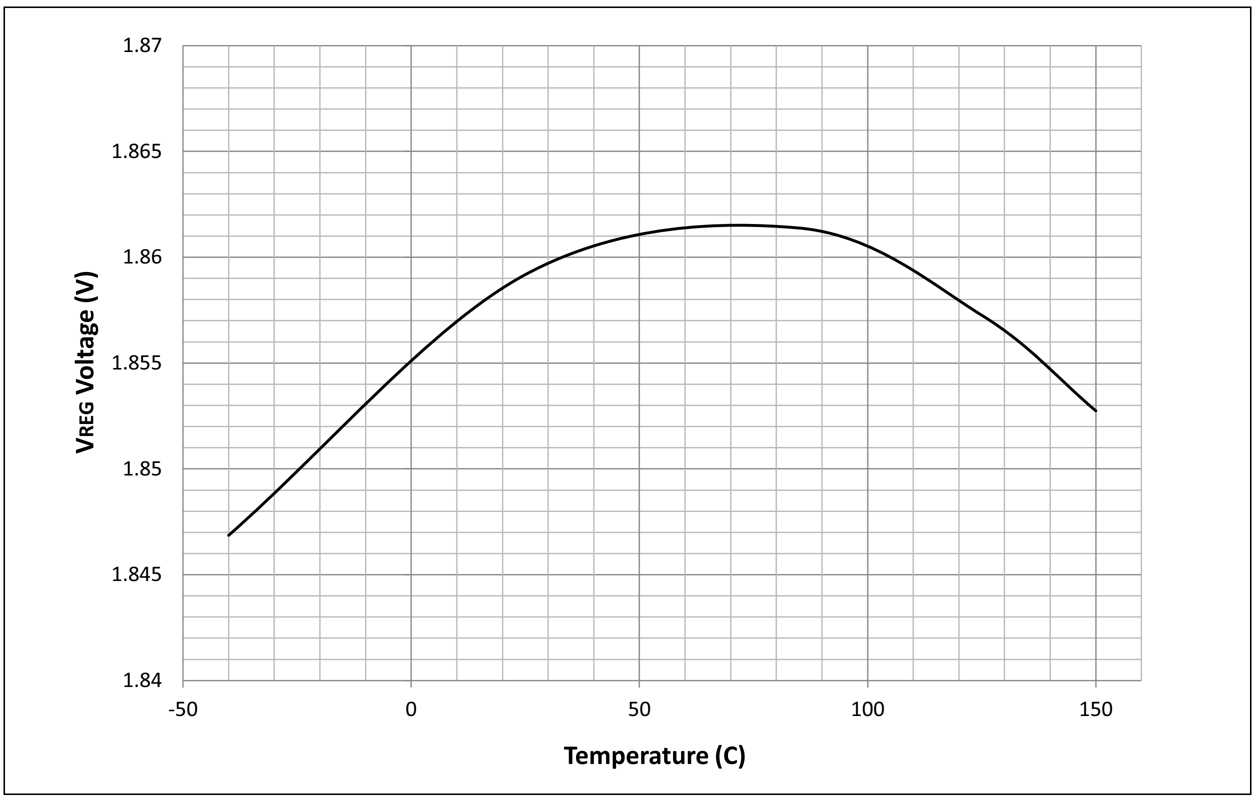


FIGURE 32-33: TYPICAL $V_{OL}$ 4x DRIVER PINS vs. $I_{OL}$ (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)




## 32.11 VREG

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE



## 33.2 IIDLE

**FIGURE 33-5: TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)**

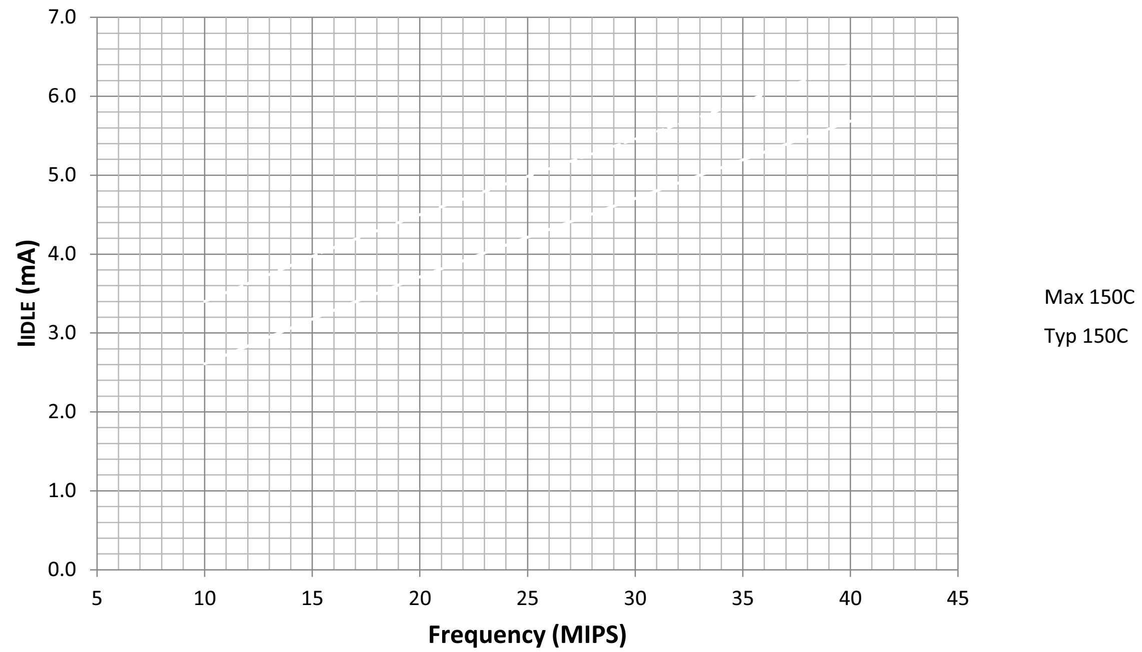



**FIGURE 33-6: TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)**