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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm102t-i-so">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm102t-i-so</a>

## Referenced Sources

This device data sheet is based on the following individual chapters of the *“dsPIC33/PIC24 Family Reference Manual”*, which are available from the Microchip web site ([www.microchip.com](http://www.microchip.com)). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- **“Introduction”** (DS70573)
- **“CPU”** (DS70359)
- **“Data Memory”** (DS70595)
- **“dsPIC33E/PIC24E Program Memory”** (DS70000613)
- **“Flash Programming”** (DS70609)
- **“Interrupts”** (DS70000600)
- **“Oscillator”** (DS70580)
- **“Reset”** (DS70602)
- **“Watchdog Timer and Power-Saving Modes”** (DS70615)
- **“I/O Ports”** (DS70000598)
- **“Timers”** (DS70362)
- **“CodeGuard™ Intermediate Security”** (DS70005182)
- **“Deadman Timer (DMT)”** (DS70005155)
- **“Input Capture”** (DS70000352)
- **“Output Compare”** (DS70005157)
- **“High-Speed PWM”** (DS70645)
- **“Analog-to-Digital Converter (ADC)”** (DS70621)
- **“Universal Asynchronous Receiver Transmitter (UART)”** (DS70000582)
- **“Serial Peripheral Interface (SPI)”** (DS70005185)
- **“Inter-Integrated Circuit™ (I<sup>2</sup>C™)”** (DS70000195)
- **“Enhanced Controller Area Network (ECAN™)”** (DS70353)
- **“Direct Memory Access (DMA)”** (DS70348)
- **“Programming and Diagnostics”** (DS70608)
- **“Op Amp/Comparator”** (DS70000357)
- **“Device Configuration”** (DS70000618)
- **“Charge Time Measurement Unit (CTMU)”** (DS70661)
- **“Single-Edge Nibble Transmission (SENT) Module”** (DS70005145)

# dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN19 AN24-AN32 AN48, AN49 AN51-AN56	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 to 4.
OCFA	I	ST	Yes	Compare Fault A input (for compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 to 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD5-RD6, RD8	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
U1CTS	I	ST	Yes	UART1 Clear-to-Send.
U1RTS	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.

**Legend:** CMOS = CMOS compatible input or output      Analog = Analog input      P = Power  
ST = Schmitt Trigger input with CMOS levels      O = Output      I = Input  
PPS = Peripheral Pin Select      TTL = TTL input buffer

## 9.0 OSCILLATOR CONFIGURATION

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Oscillator**” (DS70580) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

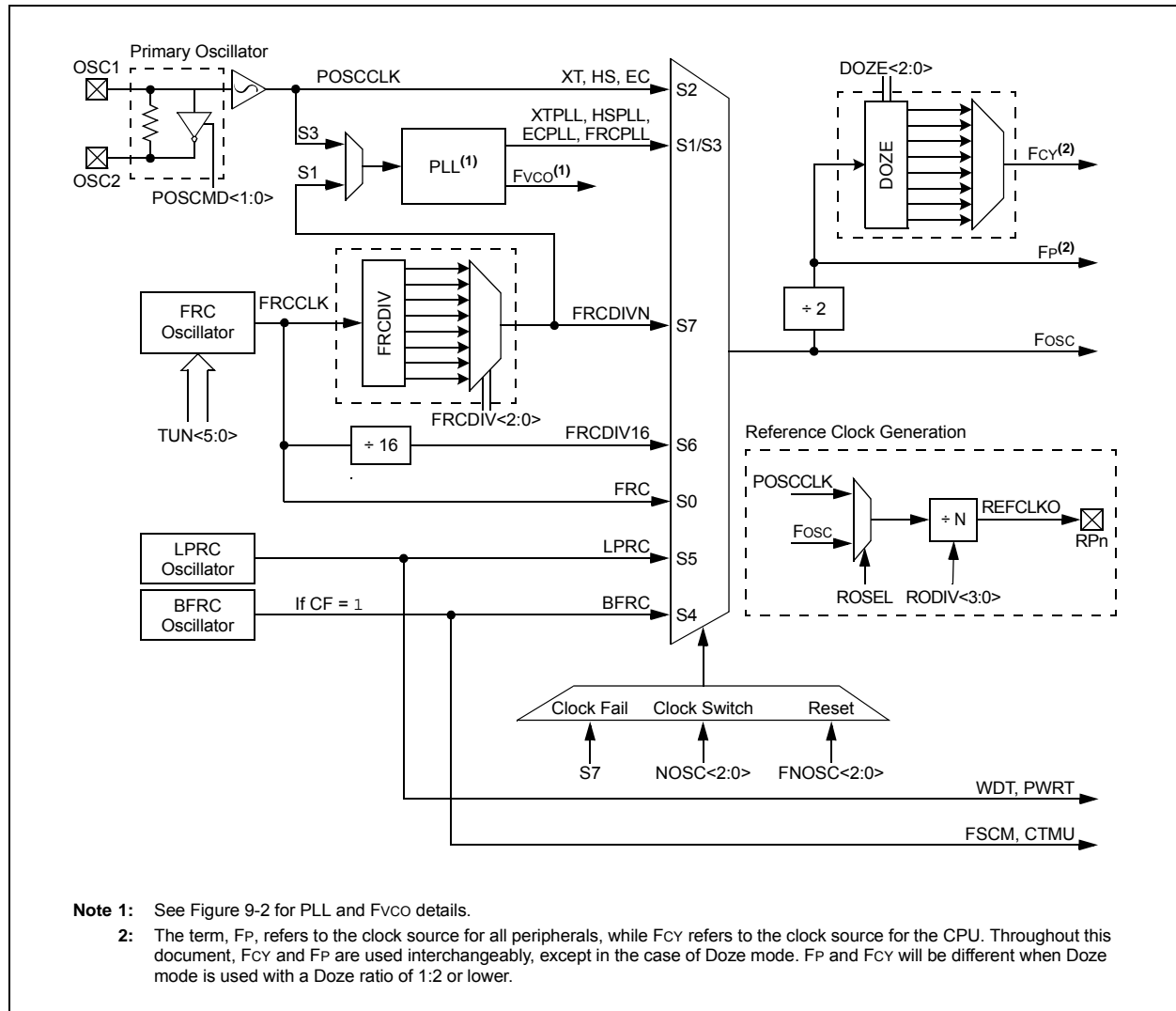
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family oscillator system provides:

- On-Chip Phase-Locked Loop (PLL) to Boost Internal Operating Frequency on Select Internal and External Oscillator Sources
- On-the-Fly Clock Switching between Various Clock Sources
- Doze mode for System Power Savings
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown.
- Backup FRC (BFRC) Function that Provides a System Clock when there is a Failure in the FRC Clock
- Configuration bits for Clock Source Selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

**FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM**



# dsPIC33EVXXXGM00X/10X FAMILY

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NOTES:

## 11.6 High-Voltage Detect (HVD)

dsPIC33EVXXXGM00X/10X devices contain High-Voltage Detection (HVD) which monitors the VCAP voltage. The HVD is used to monitor the VCAP supply voltage to ensure that an external connection does not raise the value above a safe level (~2.4V). If high core voltage is detected, all I/Os are disabled and put in a tri-state condition. The device remains in this I/O tri-state condition as long as the high-voltage condition is present.

## 11.7 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-10 under "Injection Current", have internal protection diodes to VDD and VSS. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

**Note:** Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention; for example, AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to  $\sim(V_{DD} - 0.8)$ , not VDD. This value is still above the minimum  $V_{IH}$  of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the  $V_{OH}/I_{OH}$  and  $V_{OL}/I_{OL}$  DC characteristic specifications. The respective  $I_{OH}$  and  $I_{OL}$  current rating only applies to maintaining the corresponding output at or above the  $V_{OH}$ , and at or below the  $V_{OL}$  levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum  $V_{IH}/V_{IL}$  levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

$$V_{OH} = 4.4V \text{ at } I_{OH} = -8 \text{ mA and } V_{DD} = 5V$$

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current, <12 mA, is technically permitted. For more information, refer to the  $V_{OH}/I_{OH}$  specifications in **Section 30.0 "Electrical Characteristics"**.

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## 18.2 SPI Control Registers

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER**

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0
bit 15						bit 8	

R/W-0	R/C-0, HS	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HS, HC	R-0, HS, HC
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7						bit 0	

<b>Legend:</b>	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		C = Clearable bit

- bit 15      **SPIEN:** SPIx Enable bit  
1 = Enables the SPIx module and configures SCKx, SDOx, SDIx and  $\overline{SSx}$  as serial port pins  
0 = Disables the SPIx module
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **SPISIDL:** SPIx Stop in Idle Mode bit  
1 = Discontinues the SPIx module operation when the device enters Idle mode  
0 = Continues the SPIx module operation in Idle mode
- bit 12-11      **Unimplemented:** Read as '0'
- bit 10-8      **SPIBEC<2:0>:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)  
Master mode:  
Number of SPIx transfers are pending.  
Slave mode:  
Number of SPIx transfers are unread.
- bit 7      **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)  
1 = The SPIx Shift register is empty and ready to send or receive the data  
0 = The SPIx Shift register is not empty
- bit 6      **SPIROV:** SPIx Receive Overflow Flag bit  
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register  
0 = Overflow has not occurred
- bit 5      **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)  
1 = RX FIFO is empty  
0 = RX FIFO is not empty
- bit 4-2      **SISEL<2:0>:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)  
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)  
110 = Interrupt when the last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty  
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete  
100 = Interrupt when one data is shifted into SPIxSR, and as a result, the TX FIFO has one open memory location  
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)  
010 = Interrupt when the SPIx receive buffer is 3/4 or more full  
001 = Interrupt when data is available in the SPIx receive buffer (SRMPT bit is set)  
000 = Interrupt when the last data in the SPIx receive buffer is read, and as a result, the buffer is empty (SRXMPT bit is set)

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## REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE <sup>(1)</sup>
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN <sup>(2)</sup>	CKP	MSTEN	SPRE2 <sup>(3)</sup>	SPRE1 <sup>(3)</sup>	SPRE0 <sup>(3)</sup>	PPRE1 <sup>(3)</sup>	PPRE0 <sup>(3)</sup>
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPI Master modes only)

1 = Internal SPI clock is disabled, pin functions as I/O

0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit

1 = SDOx pin is not used by the module; pin functions as I/O

0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit

1 = Communication is word-wide (16 bits)

0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit

Master mode:

1 = Input data is sampled at the end of data output time

0 = Input data is sampled at the middle of data output time

Slave mode:

SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** Clock Edge Select bit<sup>(1)</sup>

1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)

0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)<sup>(2)</sup>

1 =  $\overline{SS}$ x pin is used for Slave mode

0 =  $\overline{SS}$ x pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit

1 = Idle state for clock is a high level; active state is a low level

0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit

1 = Master mode

0 = Slave mode

**Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

**2:** This bit must be cleared when FRMEN = 1.

**3:** Do not set both primary and secondary prescalers to the value of 1:1.



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## REGISTER 22-13: CxBUFPNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-12      **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits  
                  1111 = Filter hits received in RX FIFO buffer  
                  1110 = Filter hits received in RX Buffer 14  
                  •  
                  •  
                  •  
                  0001 = Filter hits received in RX Buffer 1  
                  0000 = Filter hits received in RX Buffer 0
- bit 11-8      **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits 15-12)
- bit 7-4      **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits 15-12)
- bit 3-0      **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

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## REGISTER 22-15: CxBUFNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F15BP<3:0>**: RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>**: RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP<3:0>**: RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP<3:0>**: RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

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## REGISTER 22-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8
R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-5      **SID<10:0>**: Standard Identifier bits  
1 = Includes bit, SIDx, in filter comparison  
0 = Bit, SIDx, is a don't care in filter comparison
- bit 4      **Unimplemented**: Read as '0'
- bit 3      **MIDE**: Identifier Receive Mode bit  
1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter  
0 = Matches either standard or extended address message if filters match, i.e., if:  
(Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID)
- bit 2      **Unimplemented**: Read as '0'
- bit 1-0      **EID<17:16>**: Extended Identifier bits  
1 = Includes bit, EIDx, in filter comparison  
0 = Bit, EIDx, is a don't care in filter comparison

## REGISTER 22-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
-n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

- bit 15-0      **EID<15:0>**: Extended Identifier bits  
1 = Includes bit, EIDx, in filter comparison  
0 = Bit, EIDx, is a don't care in filter comparison

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## REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7						bit 0	

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bit  
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating  
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit  
1 = MCI is connected to OR gate  
0 = MCI is not connected to OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit  
1 = Inverted MCI is connected to OR gate  
0 = Inverted MCI is not connected to OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit  
1 = MBI is connected to OR gate  
0 = MBI is not connected to OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit  
1 = Inverted MBI is connected to OR gate  
0 = Inverted MBI is not connected to OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit  
1 = MAI is connected to OR gate  
0 = MAI is not connected to OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit  
1 = Inverted MAI is connected to OR gate  
0 = Inverted MAI is not connected to OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit  
1 = Inverted ANDI is connected to OR gate  
0 = Inverted ANDI is not connected to OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit  
1 = ANDI is connected to OR gate  
0 = ANDI is not connected to OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit  
1 = MCI is connected to AND gate  
0 = MCI is not connected to AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit  
1 = Inverted MCI is connected to AND gate  
0 = Inverted MCI is not connected to AND gate

# dsPIC33EVXXGM00X/10X FAMILY

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In

these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

**Note:** For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

**TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
$a \in \{b, c, d\}$	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register $\in \{W13, [W13]+ 2\}$
bit4	4-bit bit selection field (used in word-addressed instructions) $\in \{0...15\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address $\in \{0x0000...0x1FFF\}$
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal $\in \{0...15\}$
lit5	5-bit unsigned literal $\in \{0...31\}$
lit8	8-bit unsigned literal $\in \{0...255\}$
lit10	10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode
lit14	14-bit unsigned literal $\in \{0...16384\}$
lit16	16-bit unsigned literal $\in \{0...65535\}$
lit23	23-bit unsigned literal $\in \{0...8388608\}$ ; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal $\in \{-512...511\}$
Slit16	16-bit signed literal $\in \{-32768...32767\}$
Slit6	6-bit signed literal $\in \{-16...16\}$
Wb	Base W register $\in \{W0...W15\}$
Wd	Destination W register $\in \{Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd]\}$
Wdo	Destination W register $\in \{Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb]\}$
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

## 29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for  
Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICKit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards,  
Evaluation Kits and Starter Kits
- Third-party development tools

## 29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

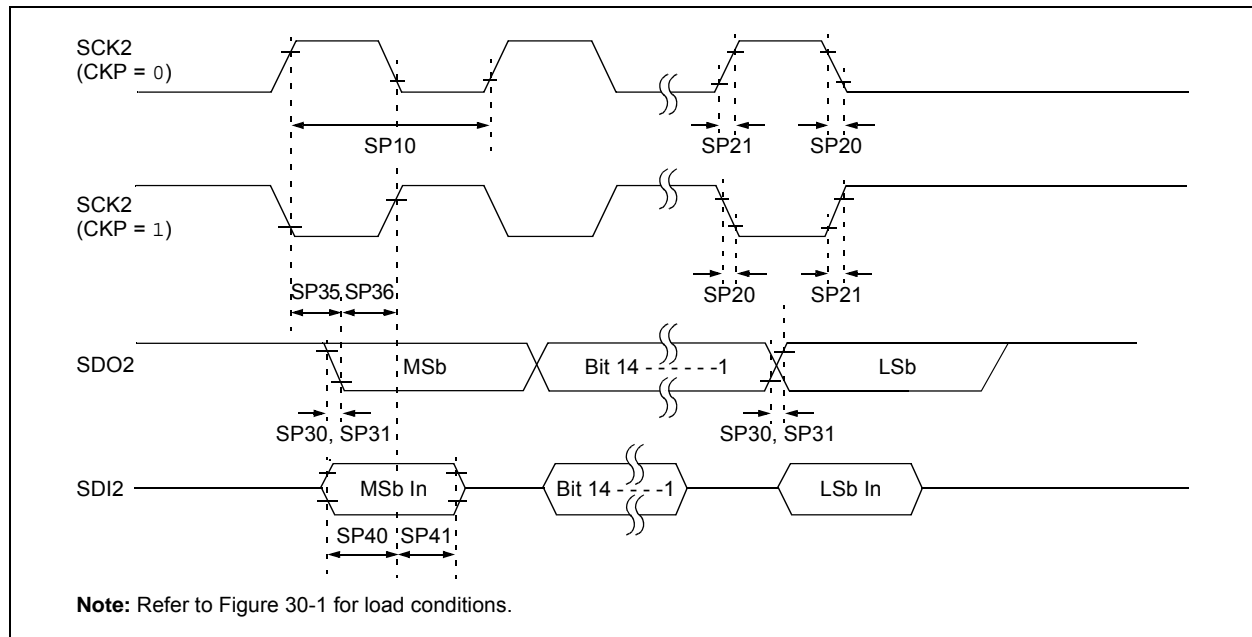
- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

# dsPIC33EVXXGM00X/10X FAMILY

**FIGURE 30-15: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**



**TABLE 30-33: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40°C to +125°C and see <b>Note 3</b>
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2sch, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

**Note 1:** These parameters are characterized but not tested in manufacturing.

**Note 2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**Note 3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

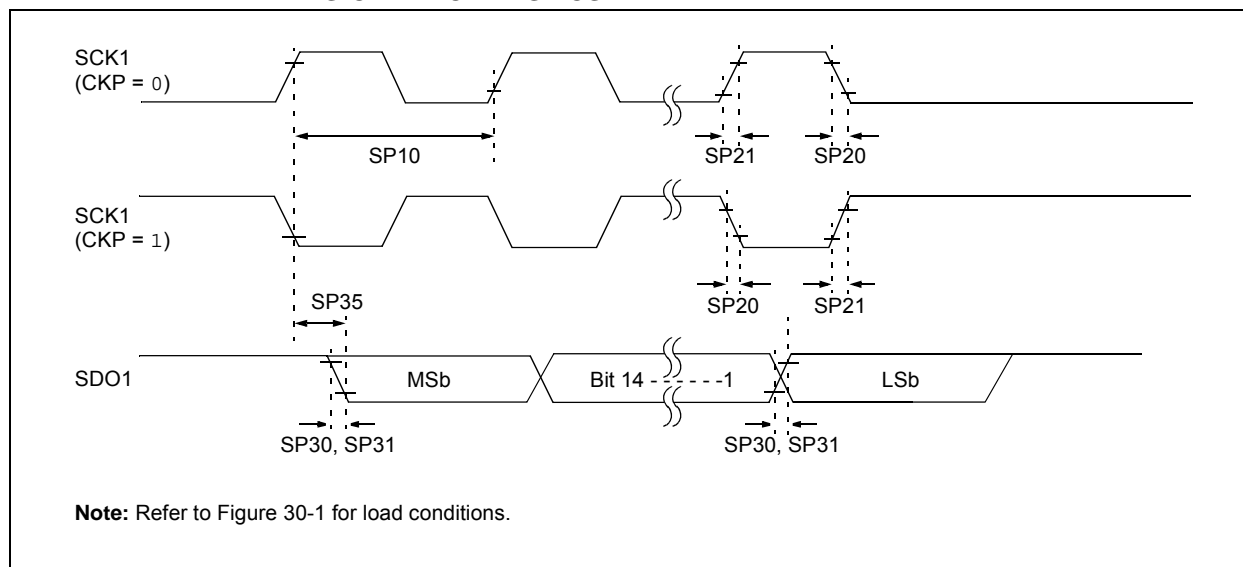
**Note 4:** Assumes 50 pF load on all SPI2 pins.

# dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 30-38: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY**

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended		
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
25 MHz	Table 30-39	—	—	0,1	0,1	0,1
25 MHz	—	Table 30-40	—	1	0,1	1
25 MHz	—	Table 30-41	—	0	0,1	1
25 MHz	—	—	Table 30-42	1	0	0
25 MHz	—	—	Table 30-43	1	1	0
25 MHz	—	—	Table 30-44	0	1	0
25 MHz	—	—	Table 30-45	0	0	0

**FIGURE 30-20: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**





# dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)  
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See <b>Note 3</b>
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and <b>Note 4</b>
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and <b>Note 4</b>
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	See <b>Note 4</b>
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See <b>Note 4</b>

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

## 31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EVXXXGM00X/10X family electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 “Electrical Characteristics”** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 “Electrical Characteristics”** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings<sup>(1)</sup>

Ambient temperature under bias <sup>(2)</sup>	-40°C to +150°C
Storage temperature	-65°C to +160°C
Voltage on VDD with respect to VSS	-0.3V to +6.0V
Maximum current out of VSS pin	350 mA
Maximum current into VDD pin <sup>(3)</sup>	350 mA
Maximum junction temperature	+155°C
Maximum current sunk by any I/O pin	20 mA
Maximum current sourced by I/O pin	18 mA
Maximum current sunk by all ports combined	200 mA
Maximum current sourced by all ports combined <sup>(3)</sup>	200 mA

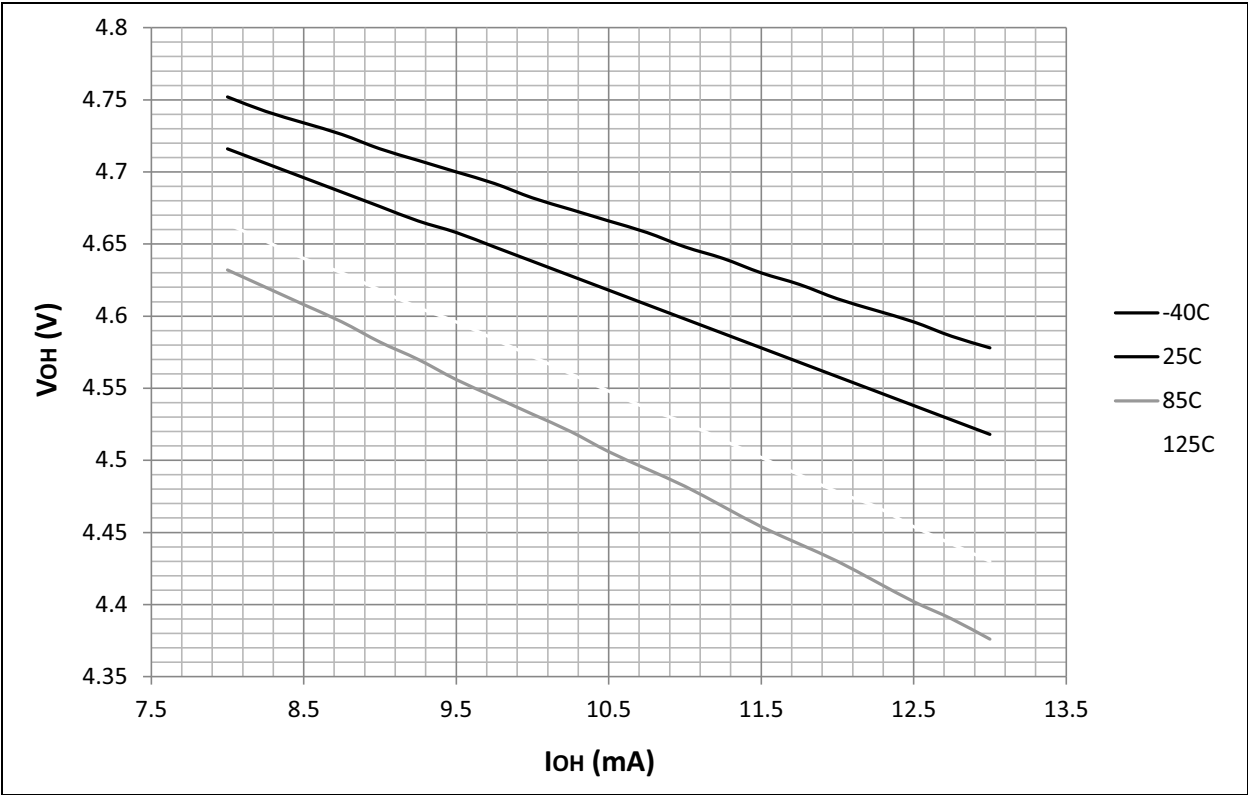
**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

**2:** AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

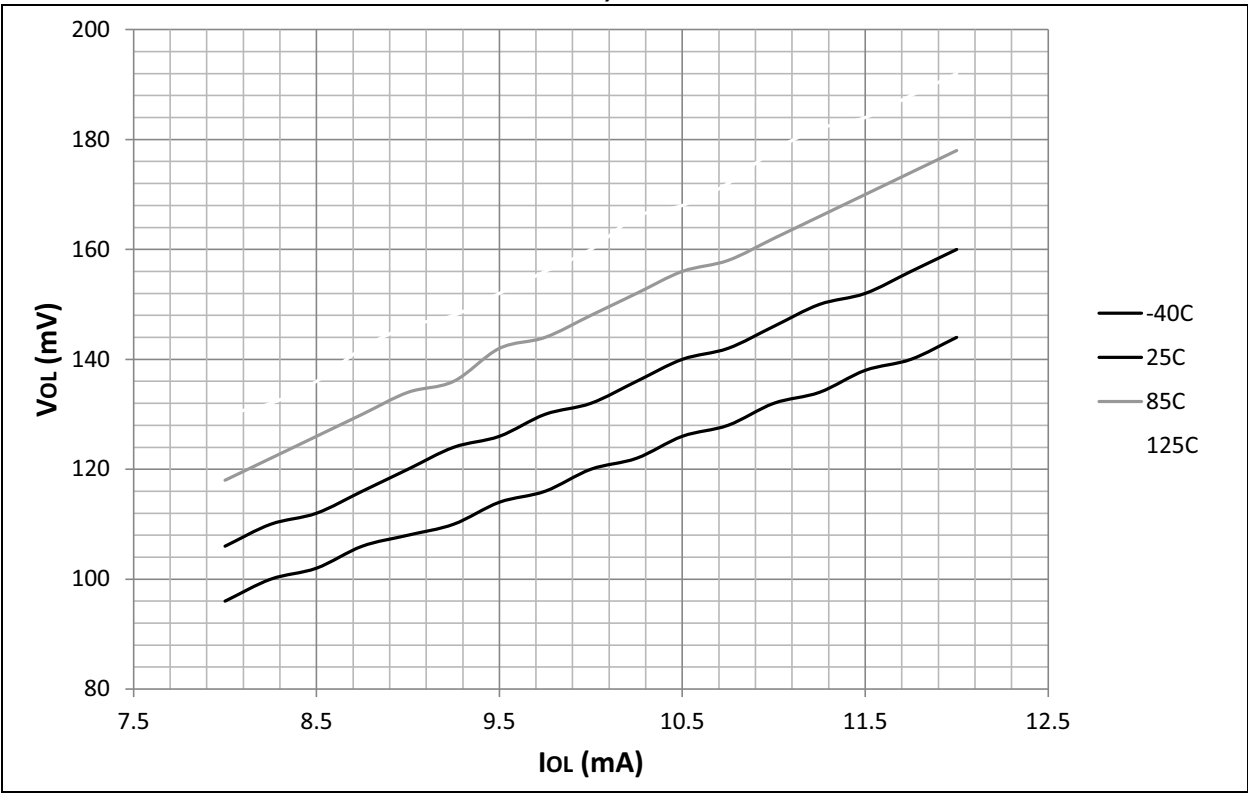
**3:** Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

# dsPIC33EVXXXGM00X/10X FAMILY

**FIGURE 32-31: TYPICAL  $V_{OH}$  4x DRIVER PINS vs.  $I_{OH}$  (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)**



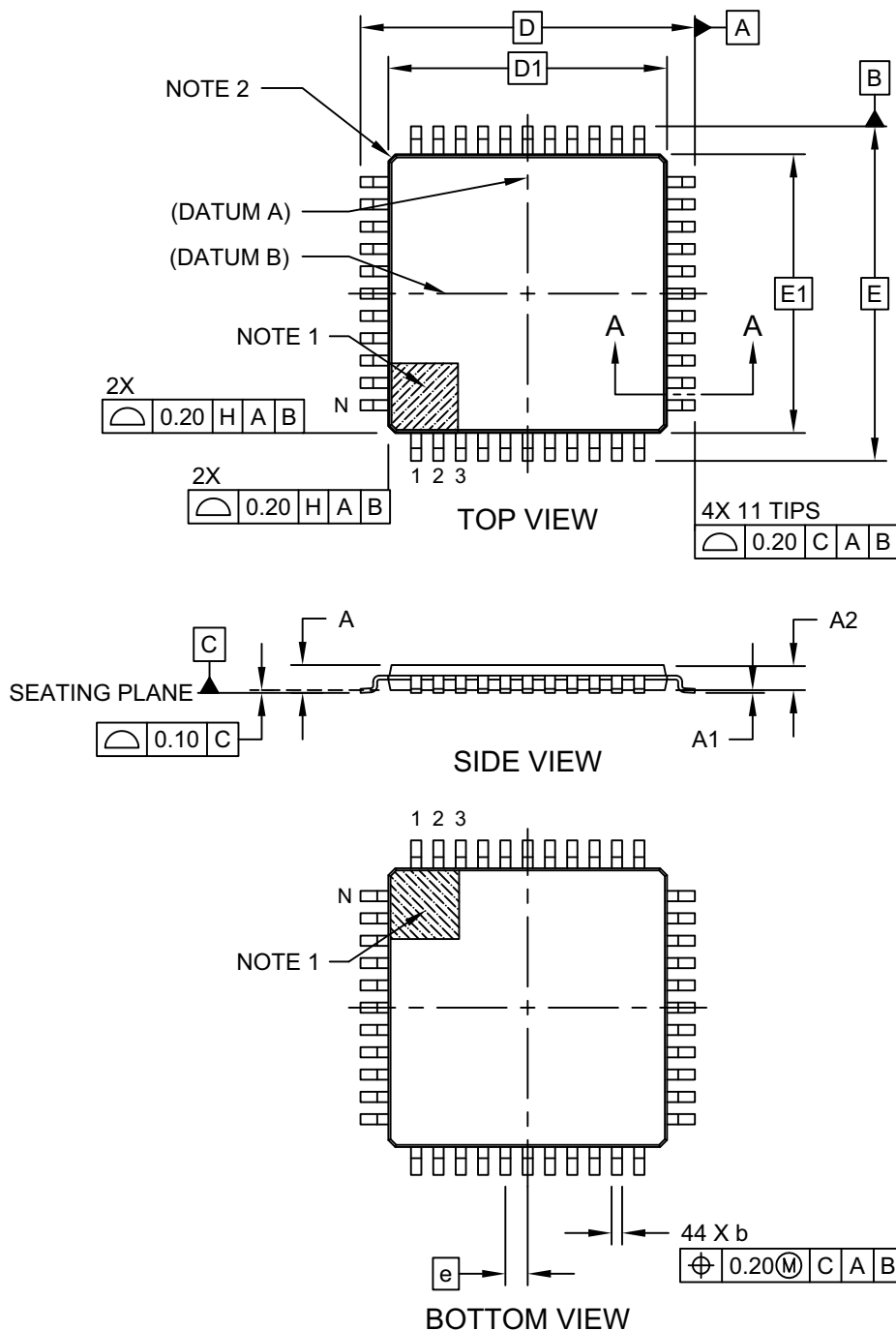
**FIGURE 32-32: TYPICAL  $V_{OL}$  8x DRIVER PINS vs.  $I_{OL}$  (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)**



# dsPIC33EVXXXGM00X/10X FAMILY

## 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

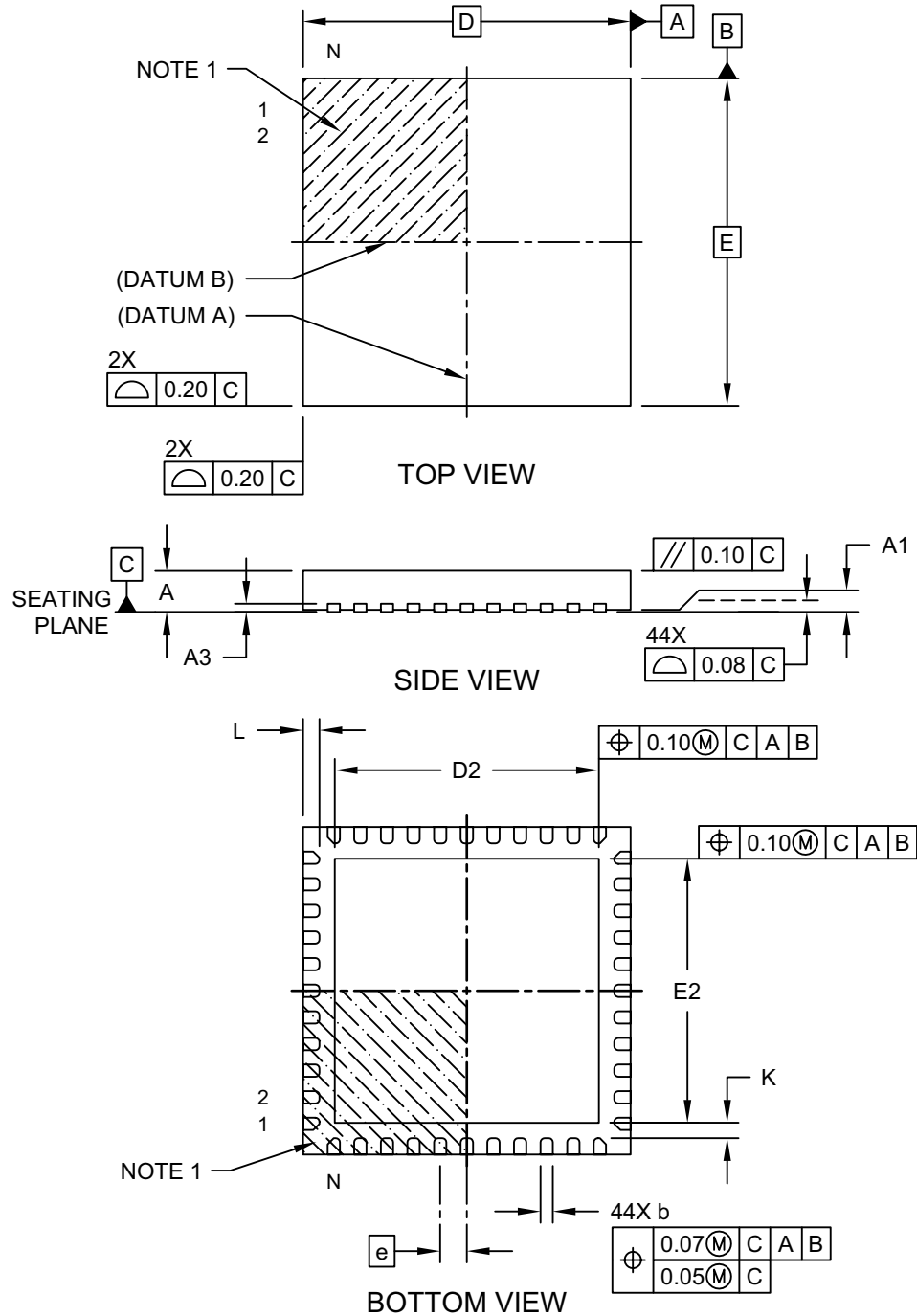


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# dsPIC33EVXXXGM00X/10X FAMILY

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-103D Sheet 1 of 2