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Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	25
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 13x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	36-UQFN (5x5)
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4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

IADLL 4	- • •			LOISIL														
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Reset s
W0	0000								W0 (W	REG)								0000
W1	0002								Ŵ									0000
W2	0004								W	2								0000
W3	0006								W	3								0000
W4	0008								W	4								0000
W5	000A		W5 0											0000				
W6	000C													0000				
W7	000E													0000				
W8	0010													0000				
W9	0012								W	9								0000
W10	0014								W1	0								0000
W11	0016											0000						
W12	0018											0000						
W13	001A								W1	3								0000
W14	001C								W1	4								0000
W15	001E								W1	5								0800
SPLIM	0020								SPL	IM								xxxx
ACCAL	0022								ACC	AL								xxxx
ACCAH	0024								ACC	AH								xxxx
ACCAU	0026			Sig	n Extension	of ACCA<3	9>						ACC	CAU				xxxx
ACCBL	0028								ACC	BL								xxxx
ACCBH	002A								ACC	BH								xxxx
ACCBU	002C			Sig	n Extension	of ACCB<3	9>						ACC	CBU				xxxx
PCL	002E						Pro	ogram Cou	nter Low We	ord Register	r						_	0000
PCH	0030	_	_	_	_	_	_	_	_	_		F	Program Cou	inter High W	ord Registe	r		0000
DSRPAG	0032	_	_	_	_	_	_				Dat	a Space Re	ad Page Reg	gister				0001
DSWPAG	0034	—	_			_	_	_				Data Spa	ce Write Pag	e Register				0001
RCOUNT	0036							REPEAT LC	op Counter	Register							0	xxxx
DCOUNT	0038							DC	OUNT<15:1	>							0	xxxx
DOSTARTL	003A	DOSTARTL<15:1> 0 x									xxxx							
DOSTARTH	003C								00xx									
DOENDL	003E							DO	ENDL<15:1	>							—	xxxx
Lanandi				- unimalar														

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: PMD REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	_	PWMMD	_	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD ⁽¹⁾	AD1MD	0000
PMD2	0762	_	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD		—		_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	_	_		—		_	—	—	_	—	0000
PMD4	0766	—	—	—	—	—	—	_	_		—		_	REFOMD	CTMUMD	_	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD		—		_	—	—	_	—	0000
PMD7	076C	_	—	—	—	-	—	—	_	-	—	-	DMA0MD	—	—		—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					
PMD8	076E	—	—	—	SENT2MD	SENT1MD	—	_	DMTMD		—		_	—	—	_	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

4.5 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing, since these two registers are used as the SFP and SSP, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.5.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.5.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit (MODCON<15>) is set

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit (MODCON<14>) is set.

Figure 4-15 shows an example of Modulo Addressing operation.

Note: Y Data Space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

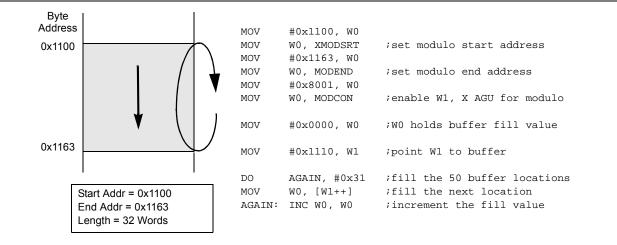


FIGURE 4-15: MODULO ADDRESSING OPERATION EXAMPLE

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0					
—		_	—	—	_		—					
bit 15							bit 8					
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0					
_	RQCOL3 RQCOL2 RQCOL1 RQ											
bit 7							bit 0					
Legend:												
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'												
-n = Value a	t POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown					
bit 15-4	Unimplemer	nted: Read as '	0'									
bit 3	RQCOL3: Cl	nannel 3 Transfe	er Request C	Collision Flag bit								
				est collision is d								
		•	•	est collision is n								
bit 2			•	Collision Flag bit								
				est collision is de								
L:1.4		•		est collision is no								
bit 1			•	Collision Flag bit								
		 1 = User force and interrupt-based request collision is detected 0 = User force and interrupt-based request collision is not detected 										
bit 0		•	•	collision Flag bit								
			•	est collision is d								
				est collision is n								

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—		—	—	-	—	—
bit 15							bit 8
U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-4	Unimplemented: Read as '0'
bit 3	PPST3: Channel 3 Ping-Pong Mode Status Flag bit
	1 = DMA3STB register is selected0 = DMA3STA register is selected
bit 2	PPST2: Channel 2 Ping-Pong Mode Status Flag bit
	1 = DMA2STB register is selected
	0 = DMA2STA register is selected
bit 1	PPST1: Channel 1 Ping-Pong Mode Status Flag bit
	1 = DMA1STB register is selected
	0 = DMA1STA register is selected
bit 0	PPST0: Channel 0 Ping-Pong mode Status Flag bit
	1 = DMA0STB register is selected
	0 = DMA0STA register is selected

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0

REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	t, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13-8	RP43R<5:0>: Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP42R<5:0>: Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5⁽¹⁾

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 Unimplemented: Read as '0'

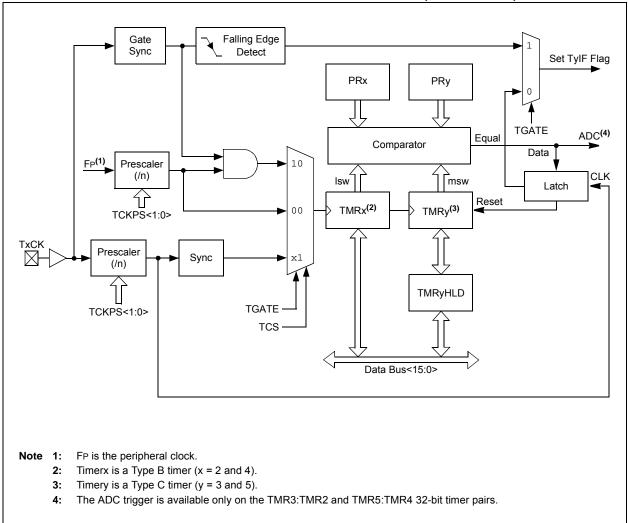
bit 13-8**RP49R<5:0>:** Peripheral Output Function is Assigned to RP49 Output Pin bits
(see Table 11-3 for peripheral function numbers)bit 7-6**Unimplemented:** Read as '0'

bit 5-0 **RP48R<5:0>:** Peripheral Output Function is Assigned to RP48 Output Pin bits

(see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.





REGISTER 14-9: DMTPSINTVL: DMT POST CONFIGURE INTERVAL STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PSIN	FV<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PSIN	TV<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'			ad as '0'				
-n = Value at POR '1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown		

bit 15-0 **PSINTV<15:0>:** Lower DMT Window Interval Configuration Status bits This is always the value of the FDMTINTVL Configuration register.

REGISTER 14-10: DMTPSINTVH: DMT POST CONFIGURE INTERVAL STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PSINT	V<31:24>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PSINT	V<23:16>			
bit 7							bit C
Legend:							
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'		id as '0'		
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is		x = Bit is unk	nown

bit 15-0 **PSINTV<31:16>:** Higher DMT Window Interval Configuration Status bits This is always the value of the FDMTINTVH Configuration register.

REGISTER 17-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	—	—	CHOPCLK9	CHOPCLK8
bit 15							bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| CHOPCLK7 | CHOPCLK6 | CHOPCLK5 | CHOPCLK4 | CHOPCLK3 | CHOPCLK2 | CHOPCLK1 | CHOPCLK0 |
| bit 7 | | | | | | | bit 0 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit	, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	CHPCLKEN: Enable Chop Clock Generator bit
	1 = Chop clock generator is enabled
	0 = Chop clock generator is disabled
bit 14-10	Unimplemented: Read as '0'
bit 9-0	CHOPCLK<9:0>: Chop Clock Divider bits
	The frequency of the chop clock signal is given by the following expression: Chop Frequency = (FP/PCLKDIV<2:0>)/(CHOPCLK<9:0> + 1)

REGISTER 17-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			MDC	<15:8>				
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
			MD	C<7:0>				
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set			'0' = Bit is cleared x = Bit is unknown			nown		

bit 15-0 MDC<15:0>: PWMx Master Duty Cycle Value bits

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
PENH	PENL	POLH	POLL	PMOD1 ⁽¹⁾	PMOD0 ⁽¹⁾	OVRENH	OVRENL			
bit 15							bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'				
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkr	nown			
bit 15	PENH: PWM	xH Output Pin	Ownership bit							
		odule controls								
		dule controls th	•	ו						
bit 14		L Output Pin	•							
		odule controls dule controls th								
bit 13		xH Output Pin	•	I						
DIL 13		bin is active-low	•							
		pin is active-hig								
bit 12		<l f<="" output="" pin="" td=""><td></td><td></td><td></td><td></td><td></td></l>								
		1 = PWMxL pin is active-low								
	0 = PWMxL p	in is active-hig	h							
bit 11-10	PMOD<1:0>:	PWMx I/O Pin	Mode bits ⁽¹⁾							
	11 = Reserve									
		/O pin pair is ir /O pin pair is ir								
		O pin pair is in O pin pair is ir		•						
bit 9		verride Enable	•							
	1 = OVRDAT	1 controls the o	output on the I	PWMxH pin						
		enerator contro								
bit 8	OVRENL: Ov	erride Enable	for PWMxL Pi	n bit						
		0 controls the o	•							
	•	nerator contro		•						
bit 7-6					ide is Enabled b	its				
		•			d by OVRDAT1. by OVRDAT0.					
bit 5-4				•	TMOD is Enable	d hits				
		ve, PWMxH is								
		ve, PWMxL is								
bit 3-2				•	/IOD is Enabled	bits				
	If current limit	is active, PWI	MxH is driven	to the state sp	ecified by CLDA	T1.				
	If current limit	is active, PWI	MxL is driven t	o the state spe	ecified by CLDA	ГО.				
Note 1: The	ese bits should	not be change	d after the PW	/Mx module is	enabled (PTEN	= 1).				

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1). **2:** If the PWMI OCK Configuration bit (EDEVOPT<0>) is a '1' the IOCONy register can only be

2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70005185) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with the Motorola[®] SPI and SIOP interfaces.

The dsPIC33EVXXXGM00X/10X device family offers two SPI modules on a single device, SPI1 and SPI2, that are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of this module, but results in a lower maximum speed. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of the following four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- · SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

Note: All of the 4 pins of the SPIx serial interface must be configured as digital in the ANSELx registers.

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1 (CONTINUED)

bit 7	GCEN: General Call Enable bit (I ² C Slave mode only)
	 1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception 0 = General call address is disabled.
bit 6	STREN: SCLx Clock Stretch Enable bit
	In I ² C Slave mode only, used in conjunction with the SCLREL bit. 1 = Enables clock stretching 0 = Disables clock stretching
bit 5	ACKDT: Acknowledge Data bit
	In I ² C Master mode, during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive. In I ² C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception. 1 = NACK is sent 0 = ACK is sent
bit 4	ACKEN: Acknowledge Sequence Enable bit
	In I ² C Master mode only; applicable during Master Receive mode. 1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit 0 = Acknowledge sequence is Idle
bit 3	RCEN: Receive Enable bit (I ² C Master mode only)
	1 = Enables Receive mode for I^2C , automatically cleared by hardware at the end of 8-bit receive data byte 0 = Receive sequence is not in progress
bit 2	PEN: Stop Condition Enable bit (I ² C Master mode only)
	 1 = Initiates Stop condition on SDAx and SCLx pins 0 = Stop condition is Idle
bit 1	RSEN: Restart Condition Enable bit (I ² C Master mode only)
	 1 = Initiates Restart condition on SDAx and SCLx pins 0 = Restart condition is Idle
bit 0	SEN: Start Condition Enable bit (I ² C Master mode only)
	 1 = Initiates Start condition on SDAx and SCLx pins 0 = Start condition is Idle
Note 1:	Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EVXXXGM00X/10X family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings⁽¹⁾

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +160°C
Voltage on VDD with respect to Vss	0.3V to +6.0V
Voltage on VCAP with respect to Vss	1.62V to 1.98V
Maximum current out of Vss pin	350 mA
Maximum current into Vod pin ⁽²⁾	350 mA
Maximum current sunk by any I/O pin	20 mA
Maximum current sourced by I/O pin	18 mA
Maximum current sourced/sunk by all ports ⁽²⁾	200 mA

- **Note 1:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
 - 2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

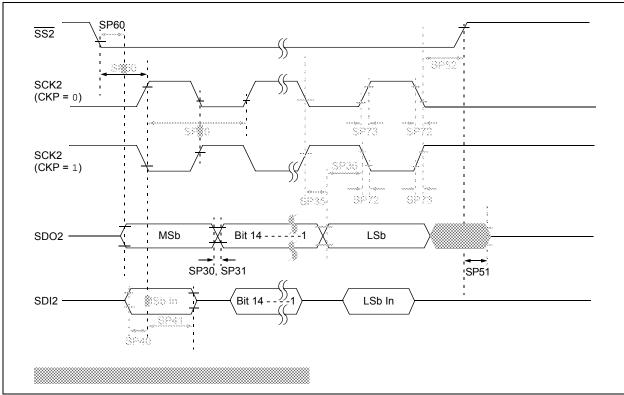


FIGURE 30-16: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

TABLE 30-41:SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 4.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCK1 Output Fall Time	—		—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCK1 Output Rise Time	—	—	_	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—		ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	_	ns	See Parameter DO31 and Note 4
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	_	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	20	—		ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

dsPIC33EVXXXGM00X/10X FAMILY

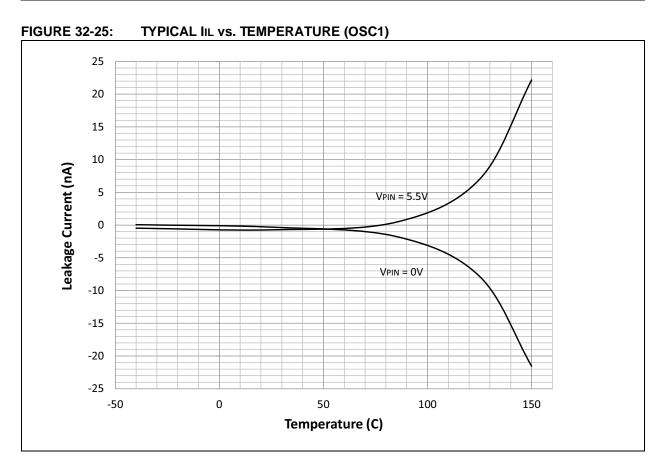
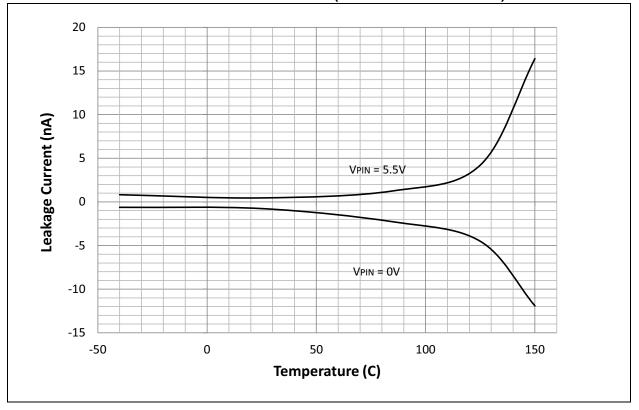
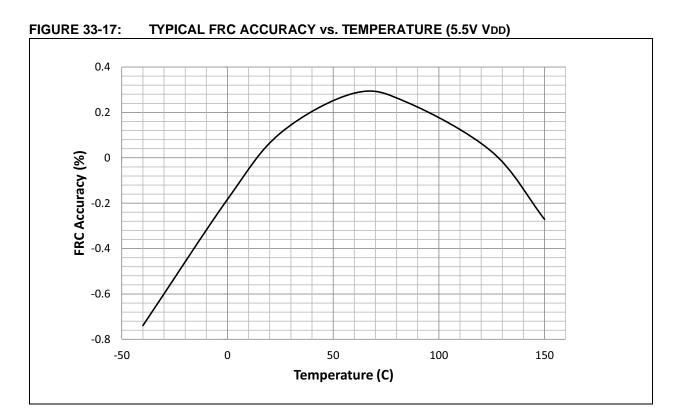


FIGURE 32-26: TYPICAL IIL vs. TEMPERATURE (GENERAL PURPOSE I/Os)



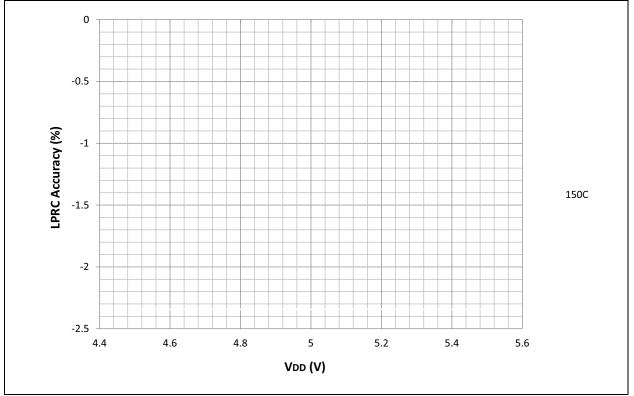
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NOTES:

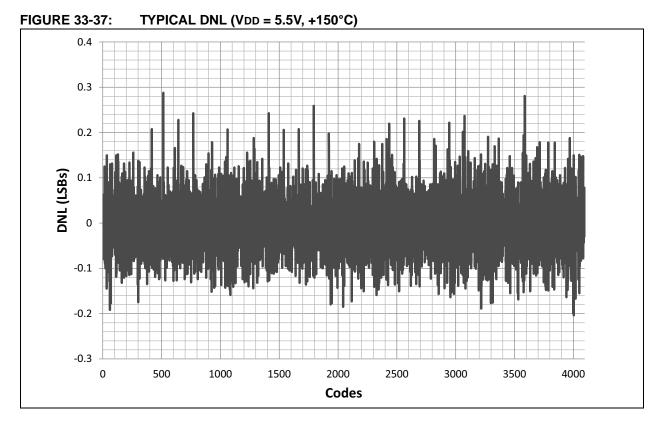








33.17 ADC DNL



33.18 ADC INL

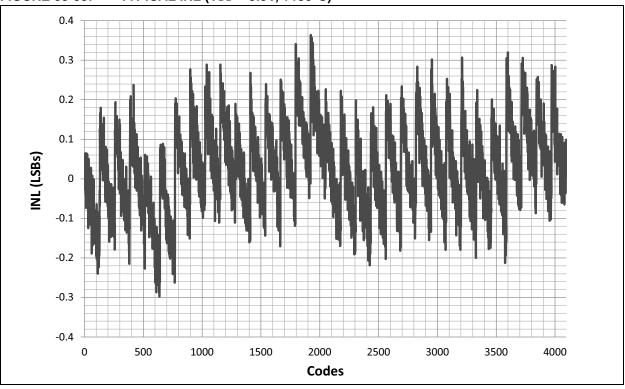


FIGURE 33-38: TYPICAL INL (VDD = 5.5V, +150°C)

Peripheral Pin Select (PPS)	
Control Registers 1	53
Input Sources, Maps Input to Function1	
Output Selection for Remappable Pins 1	
Pinout I/O Descriptions (table)	
Power-Saving Features1	
Clock Frequency and Switching1	
Instruction-Based Modes1	
Idle1	
Sleep1	34
Interrupts Coincident with Power Save	24
Instructions1	
Program Address Space Construction	
Data Access from Program Memory Using	19
Table Instructions	81
Memory Map for dsPIC33EV128GM00X/10X	01
Devices	33
Memory Map for dsPIC33EV256GM00X/10X	00
Devices	34
Memory Map for dsPIC33EV32GM00X/10X	
Devices	31
Memory Map for dsPIC33EV64GM00X/10X	
Devices	32
Table Read Instructions	
TBLRDH	81
TBLRDL	81
Program Memory	
Interrupt/Trap Vectors	
Organization	
Reset Vector	35
Programmer's Model	
Register Descriptions	23
	-0
R	20
Referenced Sources	
Referenced Sources Register Maps	12
Referenced Sources Register Maps ADC1	12 46
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1)	12 46 47
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0)	12 46 47 47
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1)	12 46 47 47 48
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0)	12 46 47 47 48 18
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 47 48 18 41
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 48 18 41 46
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 47 48 18 41 46 59
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 48 18 41 46 59 52
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 47 48 18 41 46 59 52 44
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1	12 46 47 47 48 18 41 46 59 52 44 44
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 48 18 41 46 59 52 44 45 53
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator	12 46 47 48 18 41 46 59 52 44 45 53 53 53
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 48 41 46 59 52 44 45 53 55 53 57
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words	12 46 47 48 18 41 46 59 52 44 45 53 58 57 52
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD	12 46 47 48 47 48 41 46 52 44 45 53 58 57 52 54
Referenced Sources	12 46 47 48 8 41 46 52 44 45 53 85 52 53 85 52 46
Referenced Sources	12 46 47 47 48 8 41 46 55 53 57 52 44 55 58 57 52 46 63 62
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXXGMX04 Devices	12 46 47 48 8 41 46 55 53 57 52 44 55 58 57 52 46 62 62
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices PORTA for dsPIC33EVXXXGMX04 Devices	12 46 47 48 18 46 52 44 45 53 57 52 46 62 62 64
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTA for dsPIC33EVXXXGMX02 Devices PORTB for dsPIC33EVXXXGMX02 Devices PORTB for dsPIC33EVXXXGMX04 Devices	12 46 47 48 18 46 52 44 45 53 57 52 43 62 62 64 64
Referenced Sources Register Maps ADC1 CAN1 (WIN (C1CTRL) = 0 or 1) CAN1 (WIN (C1CTRL) = 0) CAN1 (WIN (C1CTRL) = 1) Configuration Words 3 CPU Core CTMU DMAC DMT I2C1 Input Capture 1 through Input Capture 4 Interrupt Controller NVM Op Amp/Comparator Output Compare Peripheral Input Remap PMD PORTA for dsPIC33EVXXXGMX02 Devices PORTA for dsPIC33EVXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices PORTB for dsPIC33EVXXXGMX04 Devices	$\begin{array}{cccccccccccccccccccccccccccccccccccc$
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Devices 50 PPS Output for dsPIC33EVXXXGM004/104 50 PPS Output for dsPIC33EVXXXGM006/106 51 Devices 51 PVM Generator 1 60 PVM Generator 3 61 PVM Generator 3 61 PWM Generator 3 61 PWM Generator 3 61 PWM Generator 3 61 PWT Receiver 49 SENT1 Receiver 49 SENT2 Receiver 49 SP11 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCCN3 (ADCx Control 1) 289 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON3 (ADCx Input Scan Select Liow) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 ADxCON2 (PWMx Alternate Dead-Time) 211 ADxCON3 (ADCx Control 3) 293 ADxCON	PPS Output for dsPIC33EVXXXGM002/102	
Devices 50 PPS Output for dsPIC33EVXXXGM006/106 51 Devices 51 PWM 60 PWM Generator 1 60 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCCN3 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 1) 289 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Input Scan Select Ligh) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON (Comparator 4 Control) 306 CMACON (Comparator X Control) 306 CMXTON (Comparator x Control) 306 CMXCON (Comparator X Mask Source	Devices	50
Devices 51 PVMM 60 PVMM Generator 1 60 PVMM Generator 2 61 PVMM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPH1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCX control 1) 289 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 3) 293 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PMMx Alternate Dead-Time) 211 AUXCONK (PWMx Auxiliary Control) 219 CHOP (PWMx Athernate Dead-Time) 211 AUXCON (Comparator X Control) 303 <		50
PWM 60 PWM Generator 1 60 PWM Generator 2 61 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCX Input Channel 0 Select) 296 ADXCHS123 (ADCx Input 295 ADXCON1 (ADCX Control 1) 289 ADXCON3 (ADCx Control 3) 293 ADXCON3 (ADCx Control 3) 293 ADXCON4 (ADCx Control 4) 294 ADXCSSL (ADCx Input Scan Select High) 298 ADXCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Status) 303 CMXCON (Comparator X Mask Source Select Control) Select Control) 308 CO		- 4
PWM Generator 1 60 PWM Generator 2 61 PWM Generator 3 61 Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCx Input Channel 0 Select) 296 ADXCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCx Control 2) 291 ADXCON3 (ADCx Control 3) 293 ADXCON4 (ADCx Control 4) 294 ADXCSSH (ADCx Input Scan Select High) 298 ADXCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Atuxiliary Control) 219 CM4CON (Comparator 2 Control) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Filter Control) 310 CMxKCON (Comparator x Mask Gating Control) 312 CMMKON (Comparator x Kliter Sold 308 CORCON (Core Control) 271 </td <td></td> <td></td>		
PWM Generator 2. 61 PWM Generator 3. 61 Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADXCSSL (ADCx Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Atternate Dead-Time) 211 AUXCON4 (Comparator X Control) 206 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Mask Source		
PWM Generator 3. 61 Reference Clock 53 SENT1 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers. 43 UART1 and UART2 45 Registers ADXCHS0 (ADCX Input Channel 0 Select) 296 ADXCHS123 (ADCx Input Channel 0 Select) 296 ADXCON2 (ADCX Control 1) 289 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCx Control 3) 293 ADXCON3 (ADCx Control 4) 294 ADXCSSH (ADCx Input Scan Select High) 298 ADXCSS (ADCx Input Scan Select Low) 300 ALTDTSK (PWMx Atternate Dead-Time) 211 AUXCON1 (Comparator 4 Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Comparator x Control) 303 CMXCON (Comparator X Control) 312 CMMCON (Comparator x Filter Control) 312 CMMSKSCO (Comparator x Mask Source Select Control) Select Control) 308 CORCON (Core Control) 271 C		
Reference Clock 53 SENT1 Receiver 49 SENT2 Receiver 49 SP11 and SP12 45 System Control 53 Timers 43 UART1 and UART2 45 Registers 43 ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCONS (ADCx Control 1) 289 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 1) 293 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSL (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON4 (CMC Comparator X Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 306 CMXCON (Comparator X Mask 310 CMXMSKSCN (Comparator X Mask 310 CMxMSKSRC (Comparator X Mask 308	PWM Generator 2	61
SENT1 Receiver 49 SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADXCHS0 (ADCx Input Channels 1, 2, 3 Select) 296 ADXCON1 (ADCx Control 1) 289 ADXCON2 (ADCx Control 2) 291 ADXCON3 (ADCx Control 2) 291 ADXCON4 (ADCx Control 2) 293 ADXCON4 (ADCx Control 3) 293 ADXCOSSH (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Autiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) CMXCKSCON (Comparator x Control, x = 1, 2, 3 or 5) CMXMSKCON (Comparator x Mask 303 Gating Control) 310 CMXMSKSCN (Comparator x Mask 308 CORCON (Core Control) 27 CTMU	PWM Generator 3	61
SENT2 Receiver 49 SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Control) 304 CMxLETR (Comparator X Filter Control) 312 CMXMSKCON (Comparator X Mask Gating Control) X = 1, 2, 3 or 5) 304 CMXELTR (Comparator X Kask Source Select Control) CTMUCON1 (CTMU Control 1) 281	Reference Clock	53
SPI1 and SPI2 45 System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channel 0 Select) 296 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 1) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHACON (Comparator Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHACON (Comparator X Control) 218 CM4CON (Comparator X Control) 303 CMXCON (Comparator X Control) 312 CMxMSKSRC (Comparator x Mask 303 Gating Control) 308 CORCON (Core Control) 27 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282	SENT1 Receiver	49
System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Aiternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CMACON (Comparator 4 Control) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMXFLTR (Comparator x Klask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON2 (CTMU Control 2) 282 CTMUCON3 (COMparator Voltage Refere	SENT2 Receiver	49
System Control 53 Timers 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 2) 291 ADxCON4 (ADCx Control 3) 293 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCX Input Scan Select Low) 300 ALTDTRx (PWMx Aiternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CMACON (Comparator 4 Control) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMXFLTR (Comparator x Klask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON2 (CTMU Control 2) 282 CTMUCON3 (COMparator Voltage Refere	SPI1 and SPI2	45
Timers. 43 UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Control 4) 294 ADxCON4 (ADCx Input Scan Select High) 298 ADxCON4 (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) X = 1, 2, 3 or 5) 304 CMxMSKSRC (Comparator x Mask Gating Control) MXMSKSRC (Comparator x Mask Source Select Control) X = 1, 2, 3 or 5) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Current Control) 284 CTMUCON2 (CTMU Control 1) 281 CTMUC		
UART1 and UART2 45 Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) CMXCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 310 CMXMSKSCO (Comparator x Mask Source 388 Gating Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 1) 282 CTMUCON1 (CTMU Control 1) 281 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) <td></td> <td></td>		
Registers ADxCHS0 (ADCx Input Channel 0 Select) 296 ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxMSKCON (Comparator x Mask Gating Control) CMXMSKSRC (Comparator x Mask Source Select Control) Select Control) 308 CORCON (Core Control 1) 281 CTMUCON1 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Vo		
ADxCHS0 (ADCx Input 296 ADxCHS123 (ADCx Input 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSL (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON4 (Conparator Select Low) 300 ALTDTRx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMXCON (Comparator x Control, x = 1, 2, 3 or 5) 304 CMXMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control		
ADxCHS123 (ADCx Input Channels 1, 2, 3 Select) 295 ADxCON1 (ADCx Control 1) 289 ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 4) 294 ADxCOSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCON2 (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMTACON (Comparator X Control) 303 CMXCON (Comparator X Control) 303 CMXCON (Comparator x Control) 312 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Comparator x Mask 310 CMXMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 27 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315		200
ADxCON1 (ADCx Control 1)	ADxCHS123 (ADCx Input	
ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 311 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Corparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 271 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 8-11	Channels 1, 2, 3 Select)	295
ADxCON2 (ADCx Control 2) 291 ADxCON3 (ADCx Control 3) 293 ADxCON4 (ADCx Control 4) 294 ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONX (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 311 CMXMSKCON (Comparator x Mask 310 CMXMSKCON (Corparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 271 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 8-11	ADxCON1 (ADCx Control 1)	289
ADxCON3 (ADCx Control 3)		
ADxCON4 (ADCx Control 4)	ADxCON3 (ADCx Control 3)	293
ADxCSSH (ADCx Input Scan Select High) 298 ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) 312 CMxMSKCON (Comparator x Mask 310 CMXMSKCON (Comparator x Mask 310 CMXMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CXBUFPNT1 (CANx Filters 0-3 316 CXBUFPNT3 (CANx Filters 4-7 316 CXBUFPNT3 (CANx Filters 8-11 30 Buffer Pointer 3)		
ADxCSSL (ADCx Input Scan Select Low) 300 ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Control) 312 CMxMSKCON (Comparator x Mask Gating Control) Gating Control) 310 CMXMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Control 2) 282 CTMUICON (CTMU Control 2) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CXBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 1) 264 CXBUFPNT3 (CANx Filters 8-11 <		
ALTDTRx (PWMx Alternate Dead-Time) 211 AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxKLTR (Comparator x Kliter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) Gating Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON1 (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) Control 2) 316 CxBUFPNT2 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 3) 266 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) Buffer Pointer 4) 267 CxCFG1 (CANx Ba		
AUXCONx (PWMx Auxiliary Control) 219 CHOP (PWMx Chop Clock Generator) 207 CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control) x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Kontrol) 312 CMxMSKCON (Comparator x Mask Gating Control) CMxMSKSRC (Comparator x Mask Saling Control) Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) Buffer Pointer 3) 266 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) Buffer Pointer 4) 267 CxCFG1 (CANx Bau		
CHOP (PWMx Chop Clock Generator)207CLKDIV (Clock Divisor)128CM4CON (Comparator 4 Control)306CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKCON (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15316Buffer Pointer 3)266CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL2 (CANx Control 1)255CxCTRL2 (CANx FIFO Control)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		
CLKDIV (Clock Divisor) 128 CM4CON (Comparator 4 Control) 306 CMSTAT (Op Amp/Comparator Status) 303 CMxCON (Comparator x Control, x = 1, 2, 3 or 5) x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) CMxMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON1 (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 30 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 30 Buffer Pointer 4) 267		219
CM4CON (Comparator 4 Control)306CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKSRC (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 3)266CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		
CMSTAT (Op Amp/Comparator Status)303CMxCON (Comparator x Control,x = 1, 2, 3 or 5)x = 1, 2, 3 or 5)304CMxFLTR (Comparator x Filter Control)312CMxMSKCON (Comparator x Mask310CMxMSKSRC (Comparator x Mask Source308Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Control 2)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 3)266CxCFG2 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		
CMxCON (Comparator x Control, x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask Gating Control) 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFEN1 (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264		
x = 1, 2, 3 or 5) 304 CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source 308 Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 316 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 316 CxCFG2 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 <		303
CMxFLTR (Comparator x Filter Control) 312 CMxMSKCON (Comparator x Mask 310 CMxMSKSRC (Comparator x Mask Source 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUCON2 (CTMU Control 2) 282 CTMUCON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 316 Buffer Pointer 1) 264 CxBUFPNT3 (CANx Filters 8-11 316 CxBUFPNT3 (CANx Filters 8-11 316 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 316 CxCFG2 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) <		
CMxMSKCON (Comparator x Mask Gating Control) 310 CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG2 (CANx Baud Rate Configuration 1) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264	x = 1, 2, 3 or 5)	304
Gating Control)310CMxMSKSRC (Comparator x Mask Source Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264	CMxFLTR (Comparator x Filter Control)	312
Gating Control)310CMxMSKSRC (Comparator x Mask Source Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264	CMxMSKCON (Comparator x Mask	
CMxMSKSRC (Comparator x Mask Source Select Control) 308 CORCON (Core Control) 27, 102 CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference Control 1) 315 CVR2CON (Comparator Voltage Reference Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG2 (CANx Baud Rate Configuration 1) 263 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264		310
Select Control)308CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-38Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265CxBUFPNT3 (CANx Filters 8-118Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		
CORCON (Core Control)27, 102CTMUCON1 (CTMU Control 1)281CTMUCON2 (CTMU Control 2)282CTMUICON (CTMU Current Control)284CTXTSTAT (CPU W Register Context Status)29CVR1CON (Comparator Voltage Reference20Control 1)315CVR2CON (Comparator Voltage Reference316CxBUFPNT1 (CANx Filters 0-3316Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		308
CTMUCON1 (CTMU Control 1) 281 CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 316 CxBUFPNT1 (CANx Filters 0-3 8 Buffer Pointer 1) 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 8 Buffer Pointer 2) 265 CxBUFPNT4 (CANx Filters 12-15 8 Buffer Pointer 3) 266 CxBUFPNT4 (CANx Filters 12-15 8 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 1) 255 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264	,	
CTMUCON2 (CTMU Control 2) 282 CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 20 Control 1) 315 CVR2CON (Comparator Voltage Reference 20 Control 2) 316 CxBUFPNT1 (CANx Filters 0-3 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 265 CxBUFPNT4 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264		
CTMUICON (CTMU Current Control) 284 CTXTSTAT (CPU W Register Context Status) 29 CVR1CON (Comparator Voltage Reference 315 CVR2CON (Comparator Voltage Reference 316 CxBUFPNT1 (CANx Filters 0-3 316 CxBUFPNT2 (CANx Filters 4-7 264 CxBUFPNT2 (CANx Filters 4-7 265 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264		
CTXTSTAT (CPU W Register Context Status)		
CVR1CON (Comparator Voltage Reference Control 1)		
Control 1)315CVR2CON (Comparator Voltage Reference Control 2)316CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		
Control 2)316CxBUFPNT1 (CANx Filters 0-39Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7265Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264	Control 1)	315
CxBUFPNT1 (CANx Filters 0-3 Buffer Pointer 1)264CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11 Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		316
CxBUFPNT2 (CANx Filters 4-7 Buffer Pointer 2) 265 CxBUFPNT3 (CANx Filters 8-11 266 CxBUFPNT4 (CANx Filters 12-15 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264	CxBUFPNT1 (CANx Filters 0-3	
Buffer Pointer 2)265CxBUFPNT3 (CANx Filters 8-11266Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		264
CxBUFPNT3 (CANx Filters 8-11Buffer Pointer 3)CxBUFPNT4 (CANx Filters 12-15Buffer Pointer 4)CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)	·	<i>.</i>
Buffer Pointer 3)266CxBUFPNT4 (CANx Filters 12-15267Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		265
CxBUFPNT4 (CANx Filters 12-15 Buffer Pointer 4) 267 CxCFG1 (CANx Baud Rate Configuration 1) 262 CxCFG2 (CANx Baud Rate Configuration 2) 263 CxCTRL1 (CANx Control 1) 255 CxCTRL2 (CANx Control 2) 256 CxEC (CANx Transmit/Receive Error Count) 262 CxFCTRL (CANx FIFO Control) 258 CxFEN1 (CANx Acceptance Filter Enable 1) 264	CxBUFPNT3 (CANx Filters 8-11	
Buffer Pointer 4)267CxCFG1 (CANx Baud Rate Configuration 1)262CxCFG2 (CANx Baud Rate Configuration 2)263CxCTRL1 (CANx Control 1)255CxCTRL2 (CANx Control 2)256CxEC (CANx Transmit/Receive Error Count)262CxFCTRL (CANx FIFO Control)258CxFEN1 (CANx Acceptance Filter Enable 1)264		266
CxCFG1 (CANx Baud Rate Configuration 1)		
CxCFG1 (CANx Baud Rate Configuration 1)	Buffer Pointer 4)	267
CxCFG2 (CANx Baud Rate Configuration 2)	CxCFG1 (CANx Baud Rate Configuration 1)	262
CxCTRL1 (CANx Control 1)		
CxCTRL2 (CANx Control 2)		
CxEC (CANx Transmit/Receive Error Count)	CxCTRI 2 (CANx Control 2)	256
CxFCTRL (CANx FIFO Control)		
CxFEN1 (CANx Acceptance Filter Enable 1)		
GXFIFU (GANX FIFU Status)259		
	UXFIFU (UAINX FIFU STATUS)	259