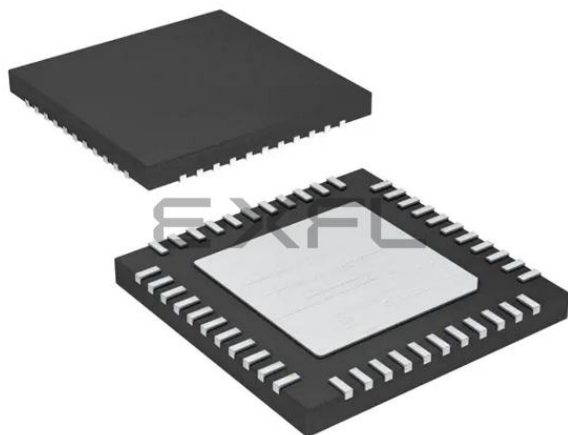




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm104-i-ml

dsPIC33EVXXXGM00X/10X FAMILY

Timers/Output Compare/Input Capture

- Nine General Purpose Timers:
 - Five 16-bit and up to two 32-bit timers/counters; Timer3 can provide ADC trigger
- Four Output Compare modules Configurable as Timers/Counters
- Four Input Capture modules

Communication Interfaces

- Two Enhanced Addressable Universal Asynchronous Receiver/Transmitter (UART) modules (6.25 Mbps):
 - With support for LIN/J2602 bus and IrDA®
 - High and low speed (SCI)
- Two SPI modules (15 Mbps):
 - 25 Mbps data rate without using PPS
- One I²C module (up to 1 Mbaud) with SMBus Support
- Two SENT J2716 (Single-Edge Nibble Transmission-Transmit/Receive) module for Automotive Applications
- One CAN module:
 - 32 buffers, 16 filters and three masks

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, Serial Peripheral Interface (SPI), ADC, Input Capture, Output Compare and Controller Area Network (CAN)

Input/Output

- GPIO Registers to Support Selectable Slew Rate I/Os
- Peripheral Pin Select (PPS) to allow Function Remap
- Sink/Source: 8 mA or 12 mA, Pin-Specific for Standard VOH/VOL
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Change Notice Interrupts on All I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: -40°C to +125°C) Compliant
- AEC-Q100 REVG (Grade 0: -40°C to +150°C) Compliant
- Class B Safety Library, IEC 60730

Class B Fault Handling Support

- Backup FRC
- Windowed WDT uses LPRC
- Windowed Deadman Timer (DMT) uses System Clock (System Windowed Watchdog Timer)
- H/W Clock Monitor Circuit
- Oscillator Frequency Monitoring through CTMU (OSCI, SYSCLK, FRC, BFRC, LPRC)
- Dedicated PWM Fault Pin
- Lockable Clock Configuration

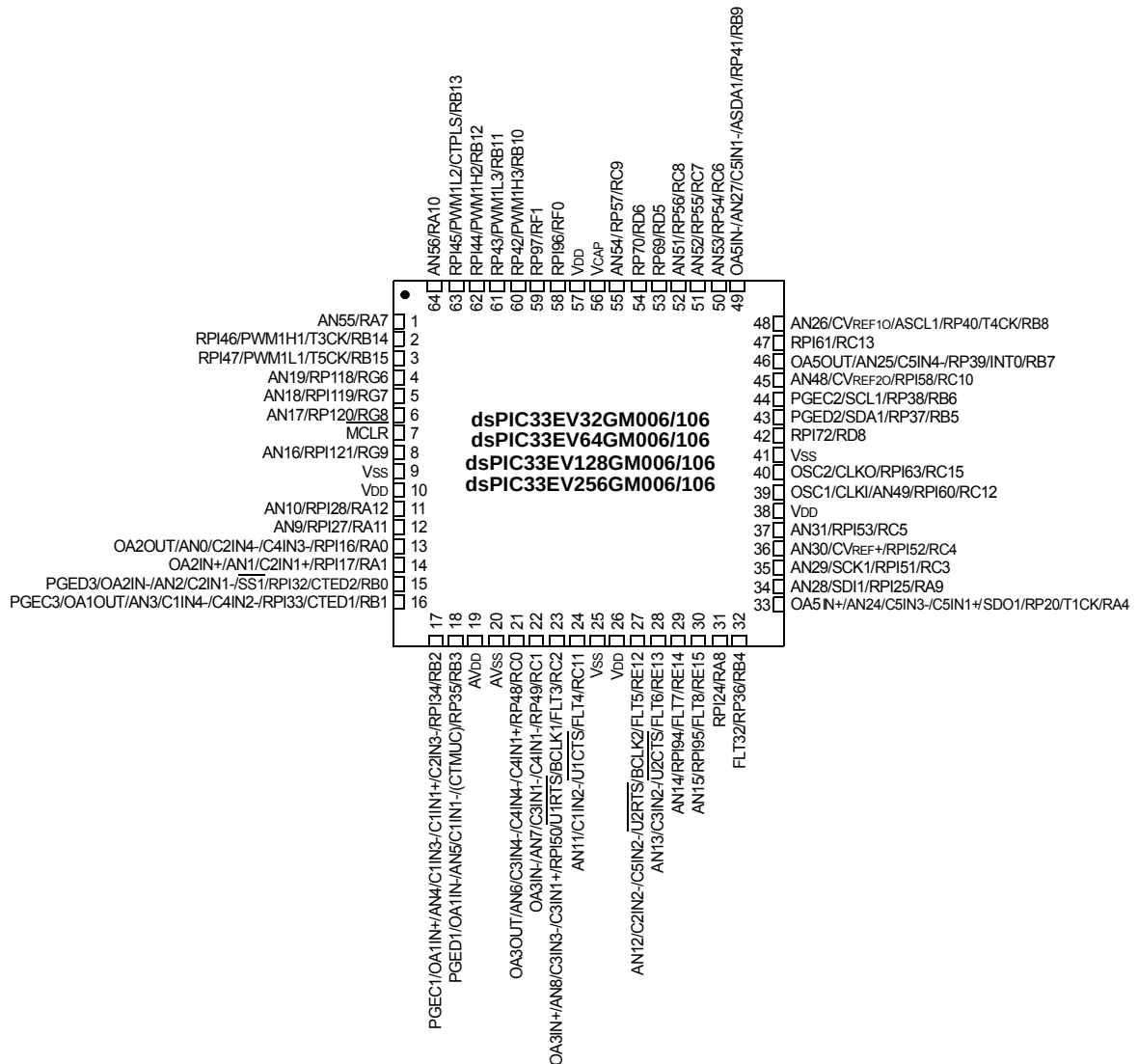
Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- Trace and Run-Time Watch

dsPIC33EVXXXGM00X/10X FAMILY

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.5 “Peripheral Pin Select (PPS)”** for available peripherals and information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

TABLE 4-7: ADC1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
ADC1BUF0	0300	ADC1 Data Buffer 0																	xxxx
ADC1BUF1	0302	ADC1 Data Buffer 1																	xxxx
ADC1BUF2	0304	ADC1 Data Buffer 2																	xxxx
ADC1BUF3	0306	ADC1 Data Buffer 3																	xxxx
ADC1BUF4	0308	ADC1 Data Buffer 4																	xxxx
ADC1BUF5	030A	ADC1 Data Buffer 5																	xxxx
ADC1BUF6	030C	ADC1 Data Buffer 6																	xxxx
ADC1BUF7	030E	ADC1 Data Buffer 7																	xxxx
ADC1BUF8	0310	ADC1 Data Buffer 8																	xxxx
ADC1BUF9	0312	ADC1 Data Buffer 9																	xxxx
ADC1BUFA	0314	ADC1 Data Buffer 10																	xxxx
ADC1BUFB	0316	ADC1 Data Buffer 11																	xxxx
ADC1BUFC	0318	ADC1 Data Buffer 12																	xxxx
ADC1BUFD	031A	ADC1 Data Buffer 13																	xxxx
ADC1BUFE	031C	ADC1 Data Buffer 14																	xxxx
ADC1BUFF	031E	ADC1 Data Buffer 15																	xxxx
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000	
AD1CON2	0322	VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0	BUFS	SMP14	SMP13	SMP12	SMP11	SMP10	BUFM	ALTS	0000	
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000	
AD1CHS123	0326	—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000	
AD1CHS0	0328	CH0NB	—	CH0SB5	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000	
AD1CSSH	032E	CSS<31:24>									—	—	—	—	CSS<19:16>				0000
AD1CSSL	0330	CSS<15:0>																	0000
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL2	DMABL1	DMABL0	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: CTMU REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUICON	033E	ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	—	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	—	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
TRISB	0E14	TRISB<15:0>																	FFFF
PORTB	0E16	RB<15:0>																	xxxx
LATB	0E18	LATB<15:0>																	xxxx
ODCB	0E1A	ODCB<15:0>																	0000
CNENB	0E1C	CNIEB<15:0>																	0000
CNPUB	0E1E	CNPUB<15:0>																	0000
CNPDB	0E20	CNPDB<15:0>																	0000
ANSELB	0E22	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				038F	
SR1B	0E24	—	—	—	—	—	—	SR1B<9:7>			—	—	SR1B4	—	—	—	—	0000	
SR0B	0E26	—	—	—	—	—	—	SR0B<9:7>			—	—	SR0B4	—	—	—	—	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel or channels are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA Channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode

- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
External Interrupt 0 (INT0)	00000000	—	—
Input Capture 1 (IC1)	00000001	0x0144 (IC1BUF)	—
Input Capture 2 (IC2)	00000101	0x014C (IC2BUF)	—
Input Capture 3 (IC3)	00100101	0x0154 (IC3BUF)	—
Input Capture 4 (IC4)	00100110	0x015C (IC4BUF)	—
Output Compare 1 (OC1)	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
Output Compare 2 (OC2)	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
Output Compare 3 (OC3)	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
Output Compare 4 (OC4)	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
Timer2 (TMR2)	00000111	—	—
Timer3 (TMR3)	00001000	—	—
Timer4 (TMR4)	00011011	—	—
Timer5 (TMR5)	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1 Receiver (UART1RX)	00001011	0x0226 (U1RXREG)	—
UART1 Transmitter (UART1TX)	00001100	—	0x0224 (U1TXREG)
UART2 Receiver (UART2RX)	00011110	0x0236 (U2RXREG)	—
UART2 Transmitter (UART2TX)	00011111	—	0x0234 (U2TXREG)
RX Data Ready (CAN1)	00100010	0x0440 (C1RXD)	—
TX Data Request (CAN1)	01000110	—	0x0442 (C1TXD)
ADC1 Convert Done (ADC1)	00001101	0x0300 (ADC1BUF0)	—

dsPIC33EVXXXGM00X/10X FAMILY

11.5.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings

across any or all of the RPn pins is possible. This includes both many-to-one, and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
C1TX	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
REFCKLO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5
SENT1	111001	RPn tied to SENT Out 1
SENT2	111010	RPn tied to SENT Out 2

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/S-1	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL ⁽¹⁾	STRICT	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit (writable from SW only)
1 = Enables the I²C module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I²C module and all I²C pins are controlled by port functions
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (I²C Slave mode only)⁽¹⁾
Module resets and (I2CEN = 0) sets SCLREL = 1.
If STREN = 0:⁽²⁾
1 = Releases clock
0 = Forces clock low (clock stretch)
If STREN = 1:
1 = Releases clock
0 = Holds clock low (clock stretch); user may program this bit to '0', clock stretch at the next SCLx low
- bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced
In Slave mode, the device does not respond to reserved address space and addresses falling in that category are NACKed.
0 = Reserved addressing would be Acknowledged
In Slave mode, the device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK.
- bit 10 **A10M:** 10-Bit Slave Address Flag bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Slew Rate Control Disable bit
1 = Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)
- bit 8 **SMEN:** SMBus Input Levels Enable bit
1 = Enables the input logic so thresholds are compliant with the SMBus specification
0 = Disables the SMBus-specific inputs

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

23.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Charge Time Measurement Unit (CTMU)**” (DS70661) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Nine Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Time Measurement Resolution Down to 200 ps
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode
- Pulse Generation Generates a Pulse using the C1INB Comparator Input and Outputs the Pulse onto the CTPLS Remappable Output

25.1 Op Amp/Comparator Control Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
PSIDL	—	—	C5EVT ⁽¹⁾	C4EVT ⁽¹⁾	C3EVT ⁽¹⁾	C2EVT ⁽¹⁾	C1EVT ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	C5OUT ⁽²⁾	C4OUT ⁽²⁾	C3OUT ⁽²⁾	C2OUT ⁽²⁾	C1OUT ⁽²⁾
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **PSIDL:** Op Amp/Comparator Stop in Idle Mode bit
 1 = Discontinues operation of all op amps/comparators when device enters Idle mode
 0 = Continues operation of all op amps/comparators in Idle mode

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **C5EVT:C1EVT:** Op Amp/Comparator 1-5 Event Status bits⁽¹⁾
 1 = Op amp/comparator event occurred
 0 = Op amp/comparator event did not occur

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op Amp/Comparator 1-5 Output Status bits⁽²⁾

When CPOL = 0:

1 = VIN+ > VIN-

0 = VIN+ < VIN-

When CPOL = 1:

1 = VIN+ < VIN-

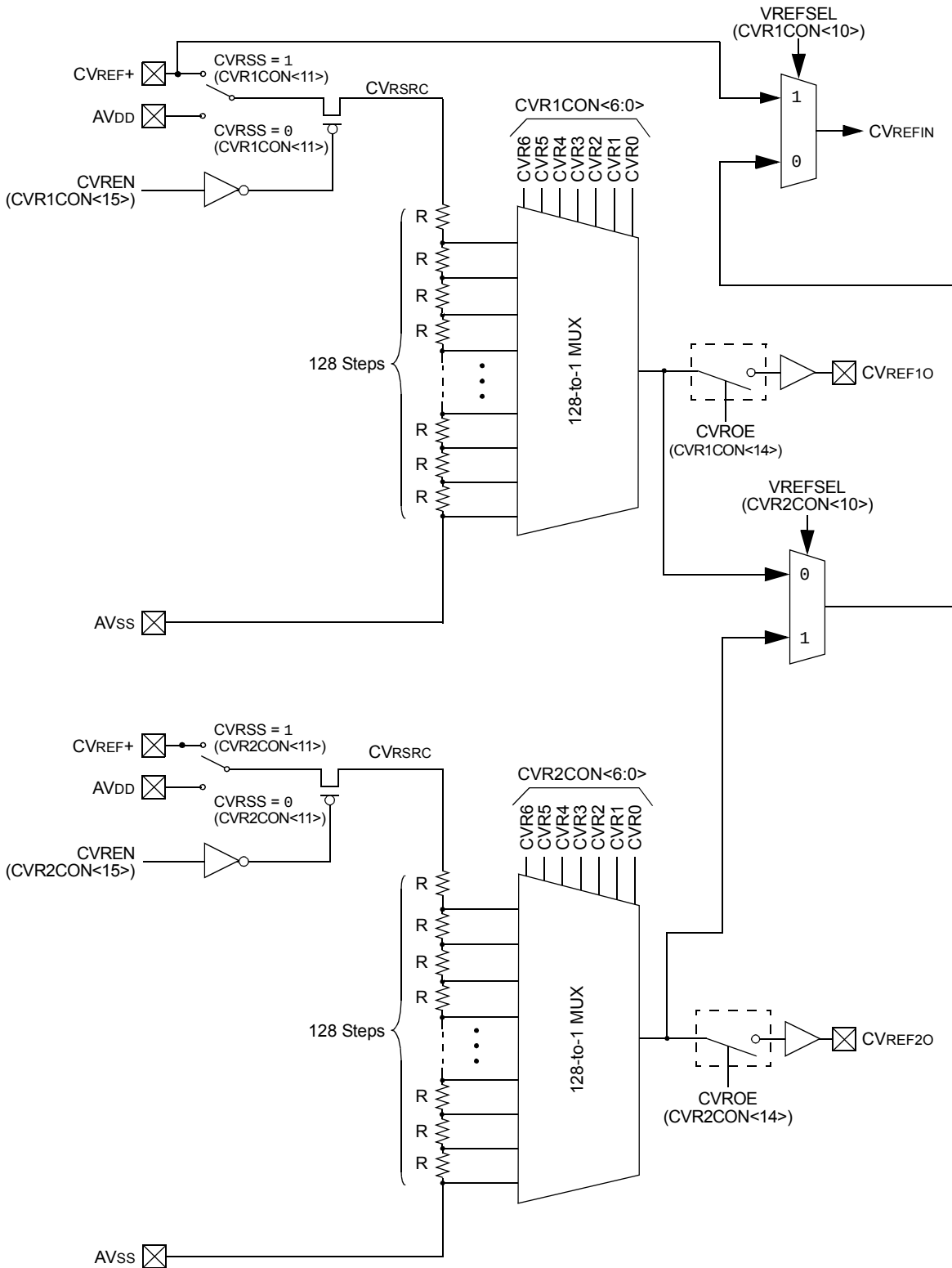
0 = VIN+ > VIN-

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: CVREF20 and CVROE (CVR2CON<14>) is not available on the 28-pin devices.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be ‘1111 1111 1111 1111’. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ‘1’s to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See Note 3
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 32-25: TYPICAL I_{IL} vs. TEMPERATURE (OSC1)

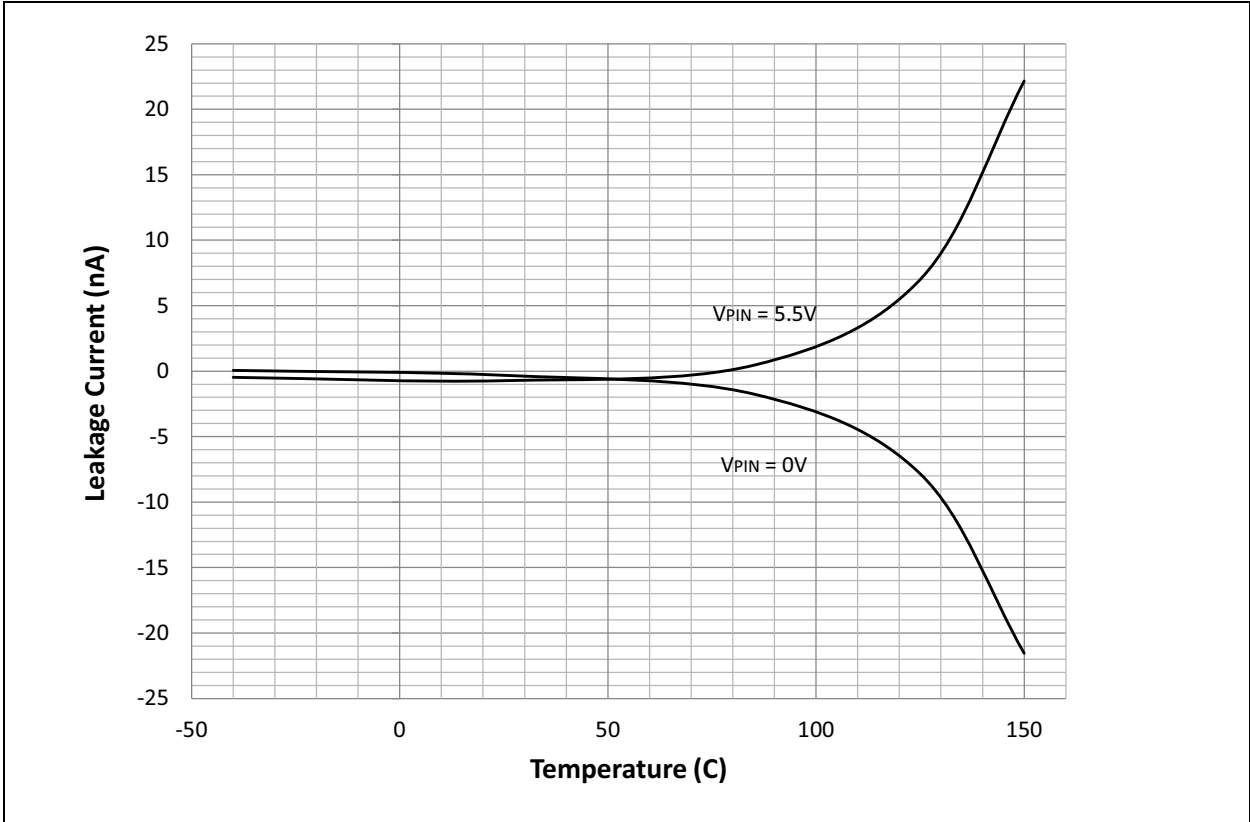
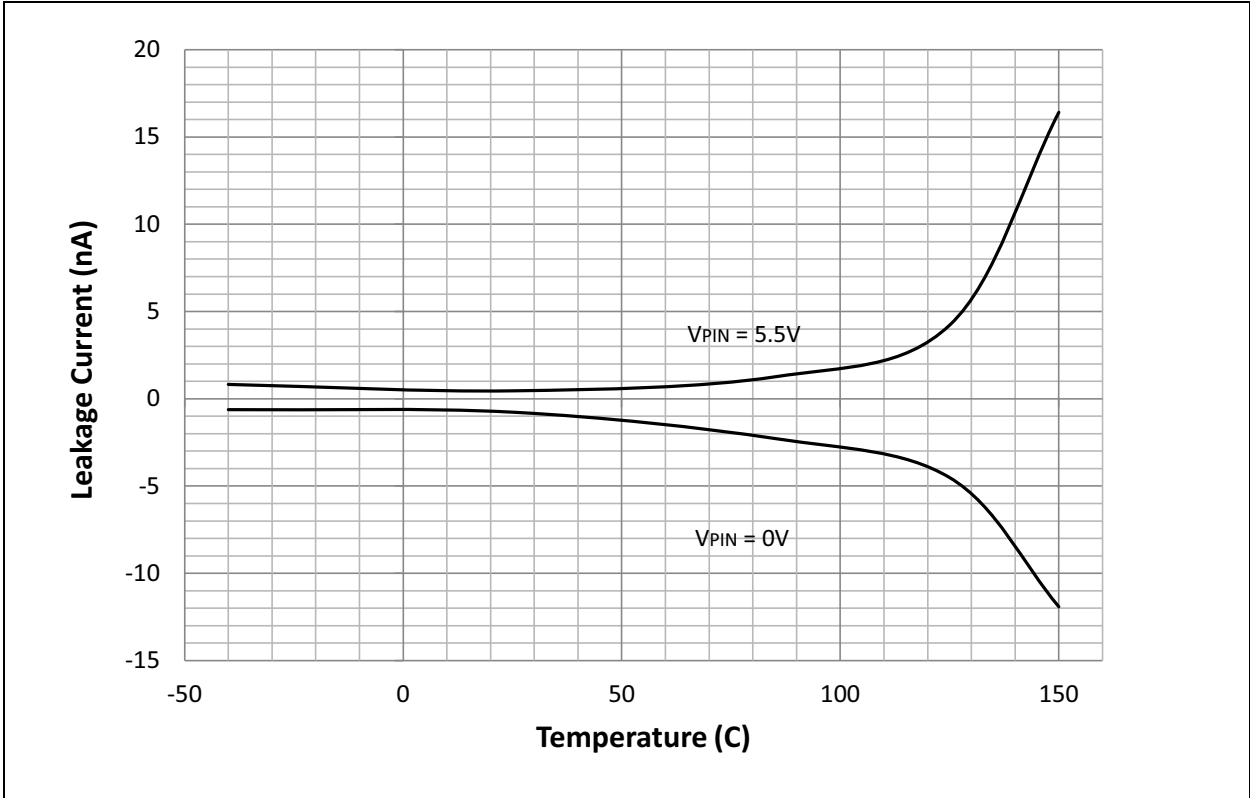
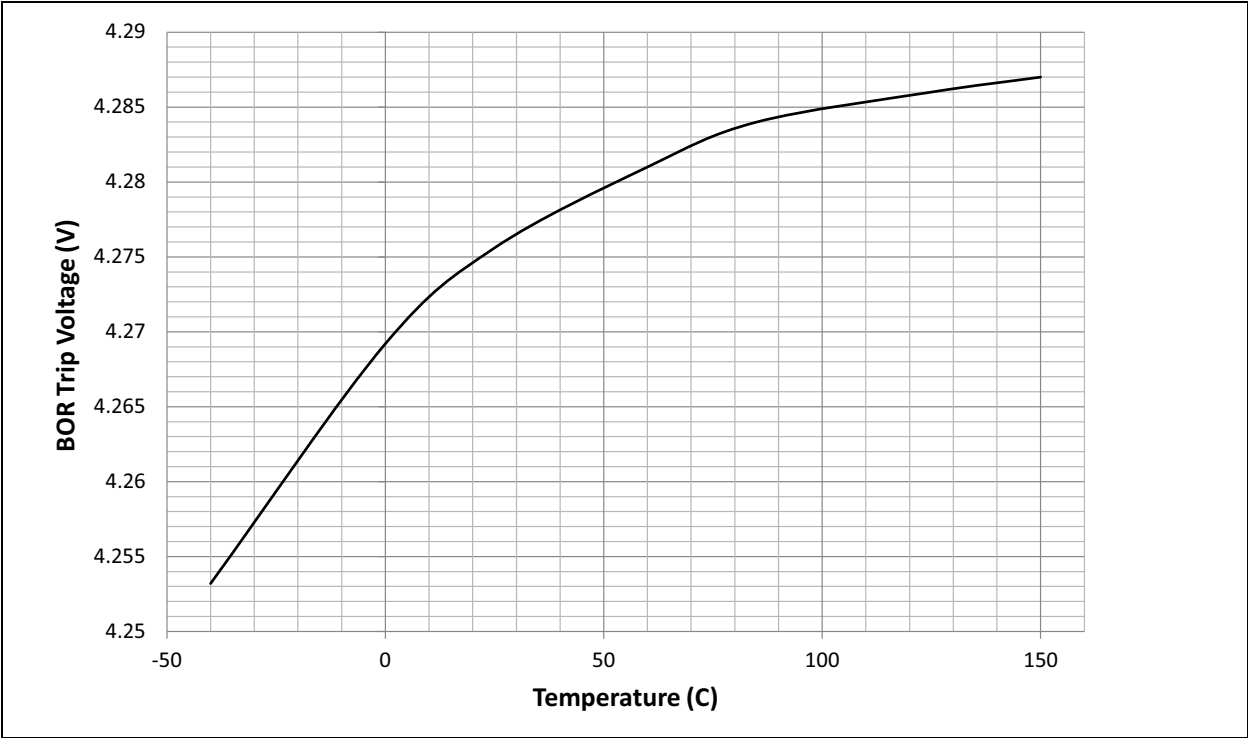


FIGURE 32-26: TYPICAL I_{IL} vs. TEMPERATURE (GENERAL PURPOSE I/Os)



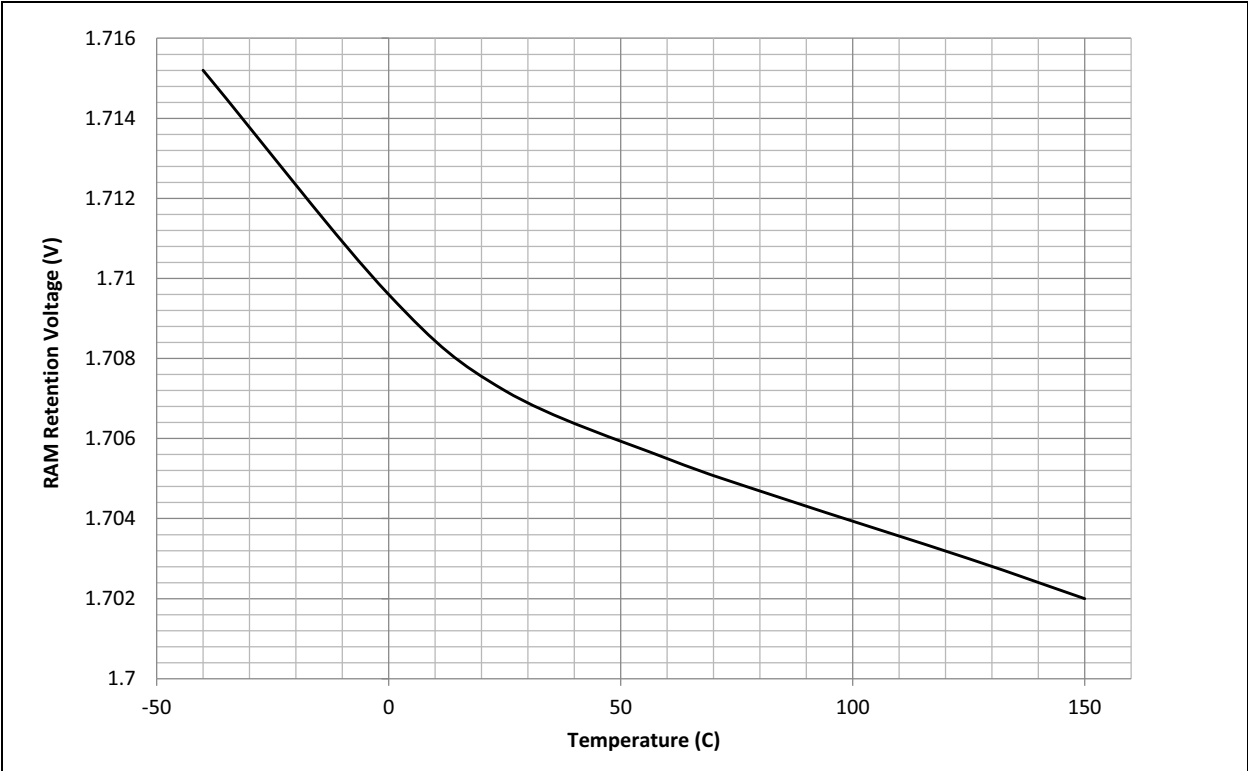
32.12 V_{BOR}

FIGURE 32-35: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



32.13 RAM Retention

FIGURE 32-36: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE



32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. V_{CM}

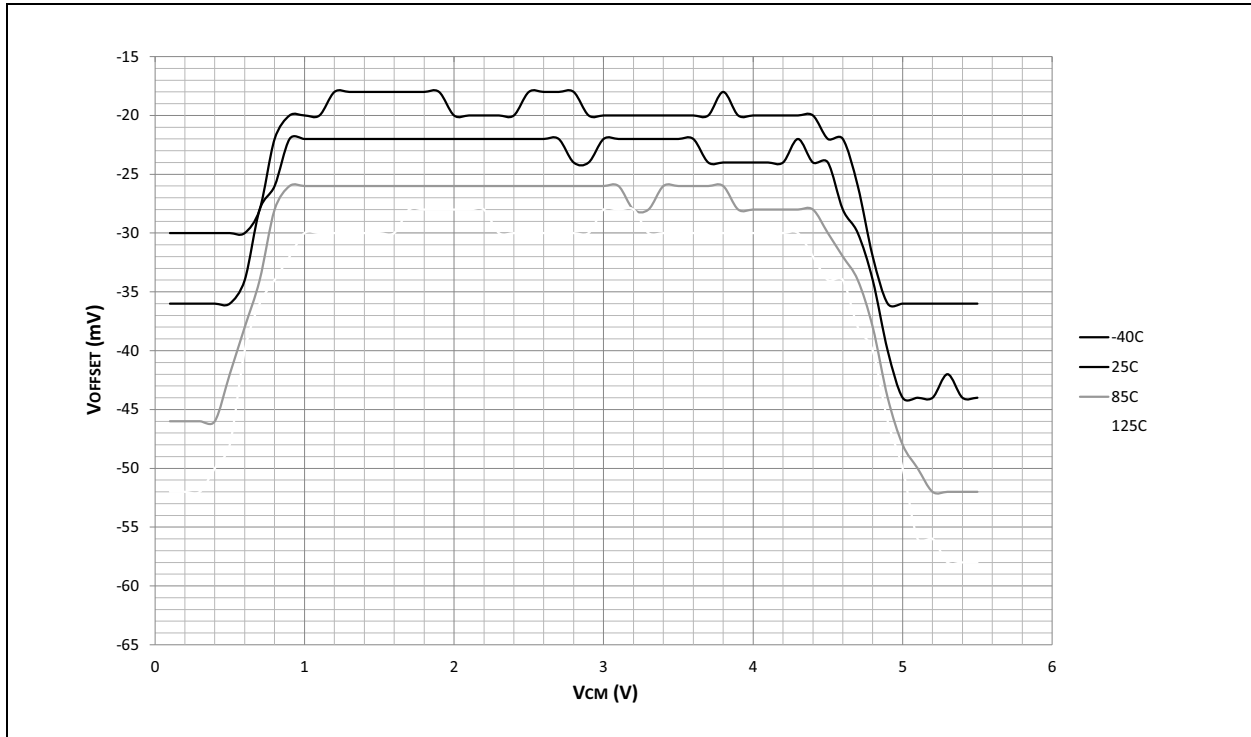
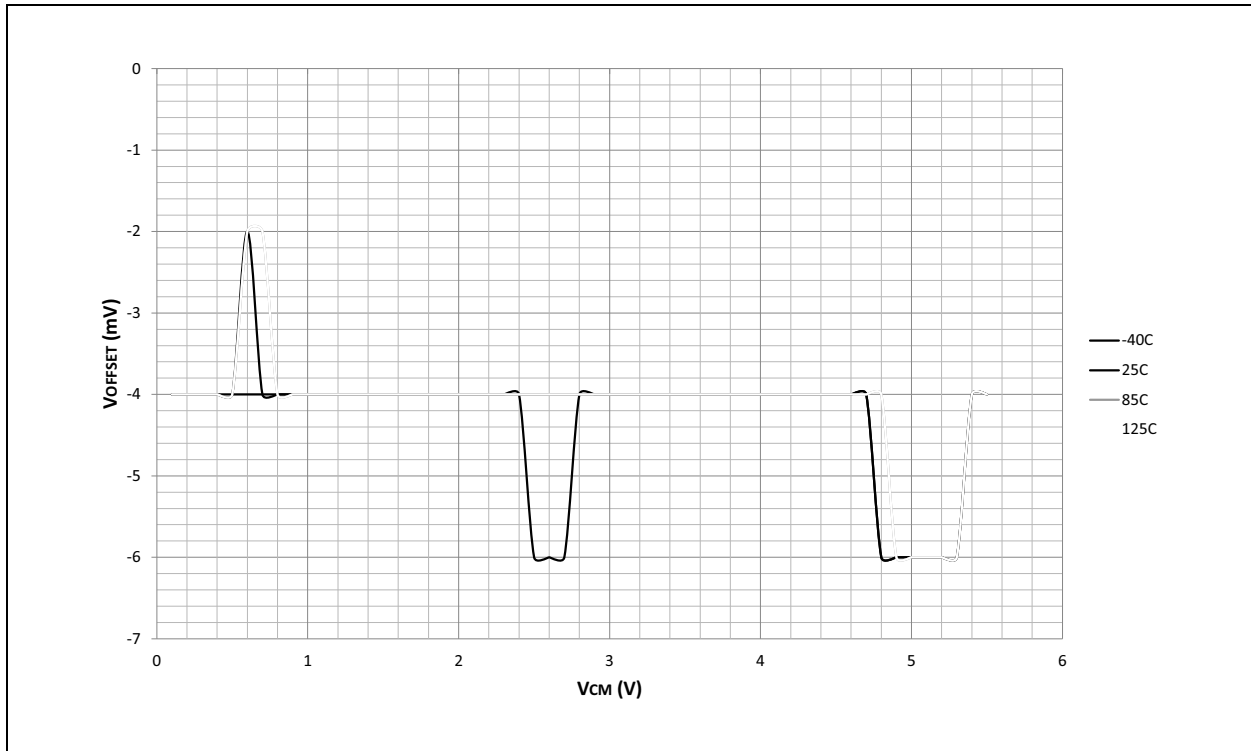


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. V_{CM} OP AMP OFFSET



32.17 ADC DNL

FIGURE 32-41: TYPICAL DNL ($V_{DD} = 5.5V$, $-40^{\circ}C$)

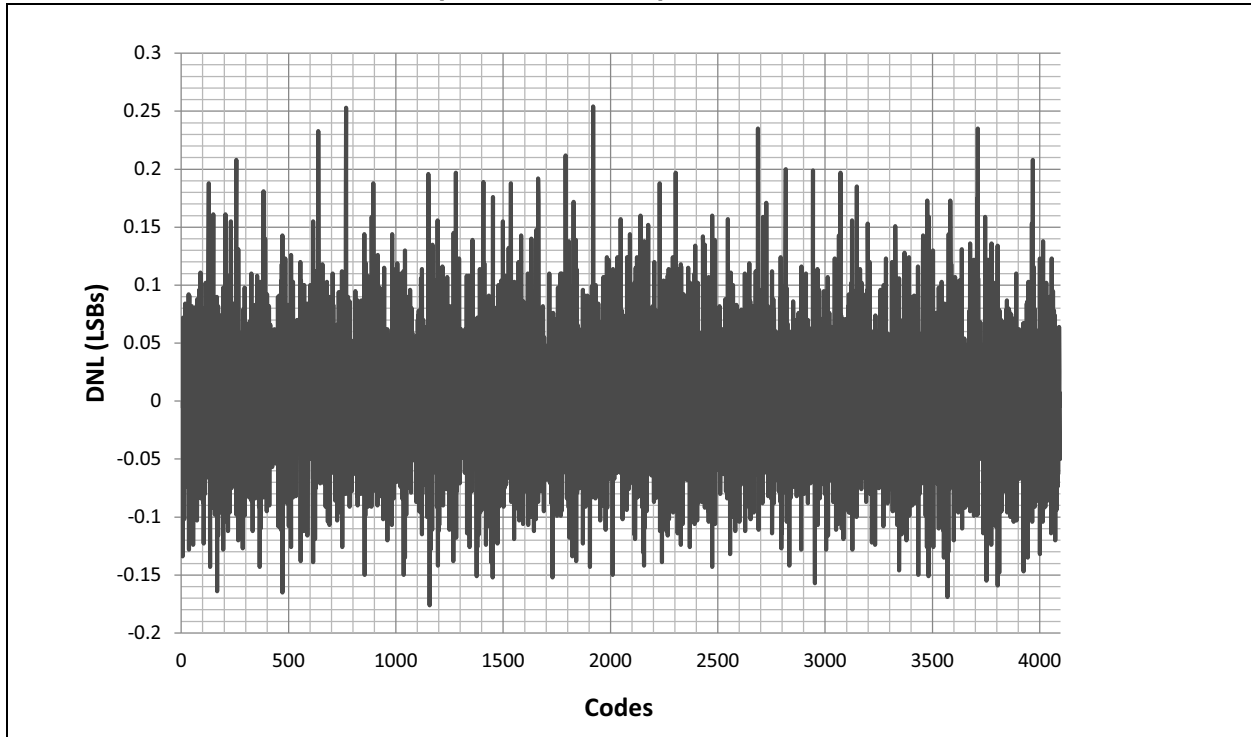
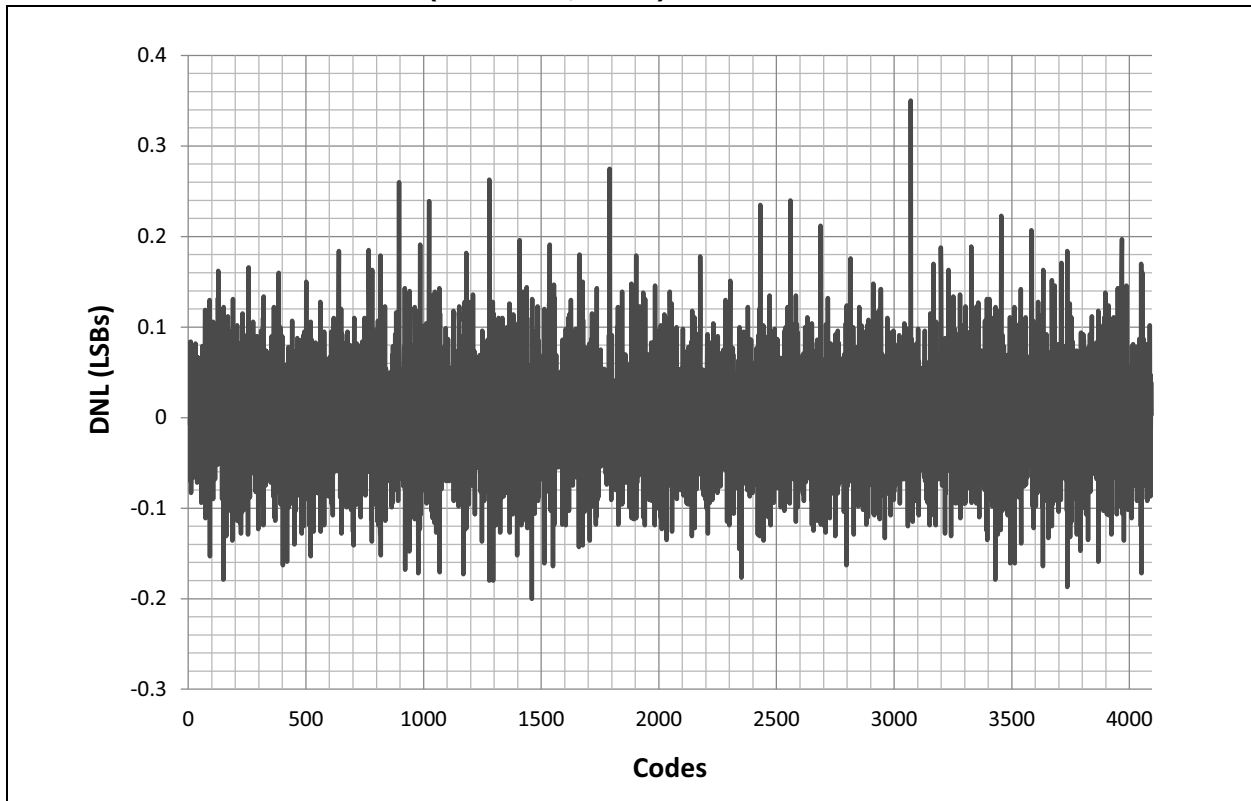


FIGURE 32-42: TYPICAL DNL ($V_{DD} = 5.5V$, $+25^{\circ}C$)



33.2 IDLE

FIGURE 33-5: TYPICAL/MAXIMUM I_{IDLE} vs. F_{OSC} (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)

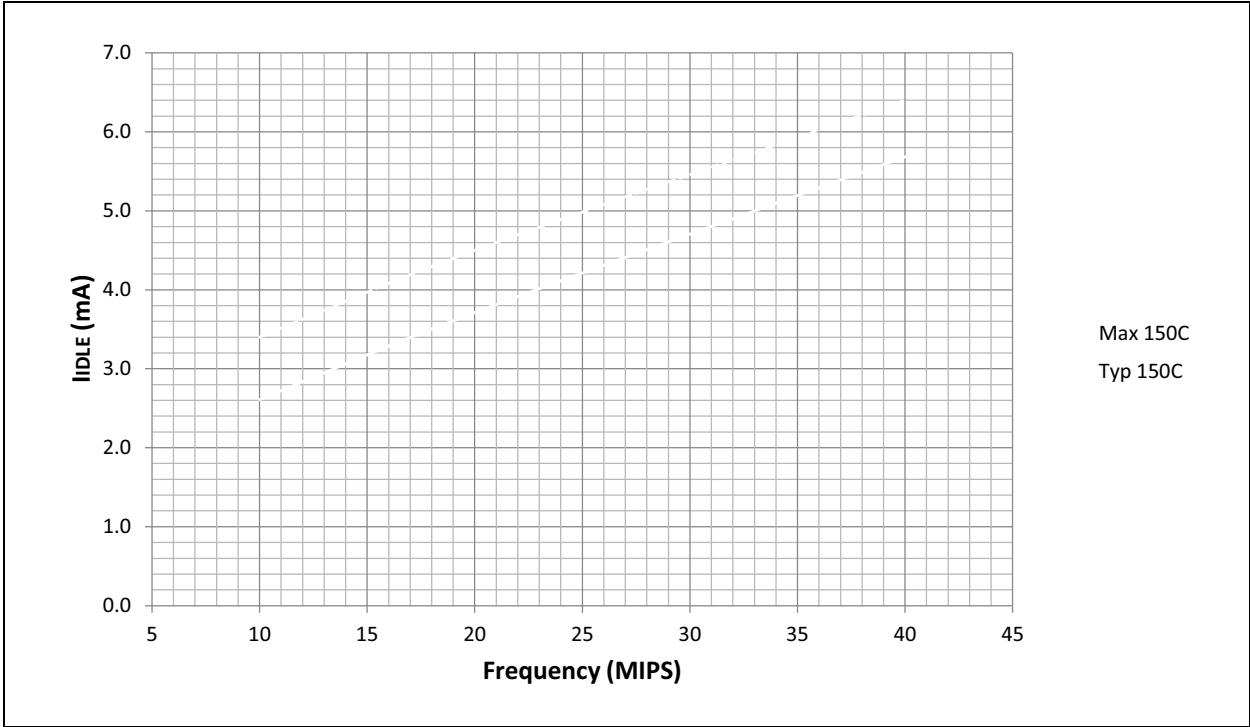
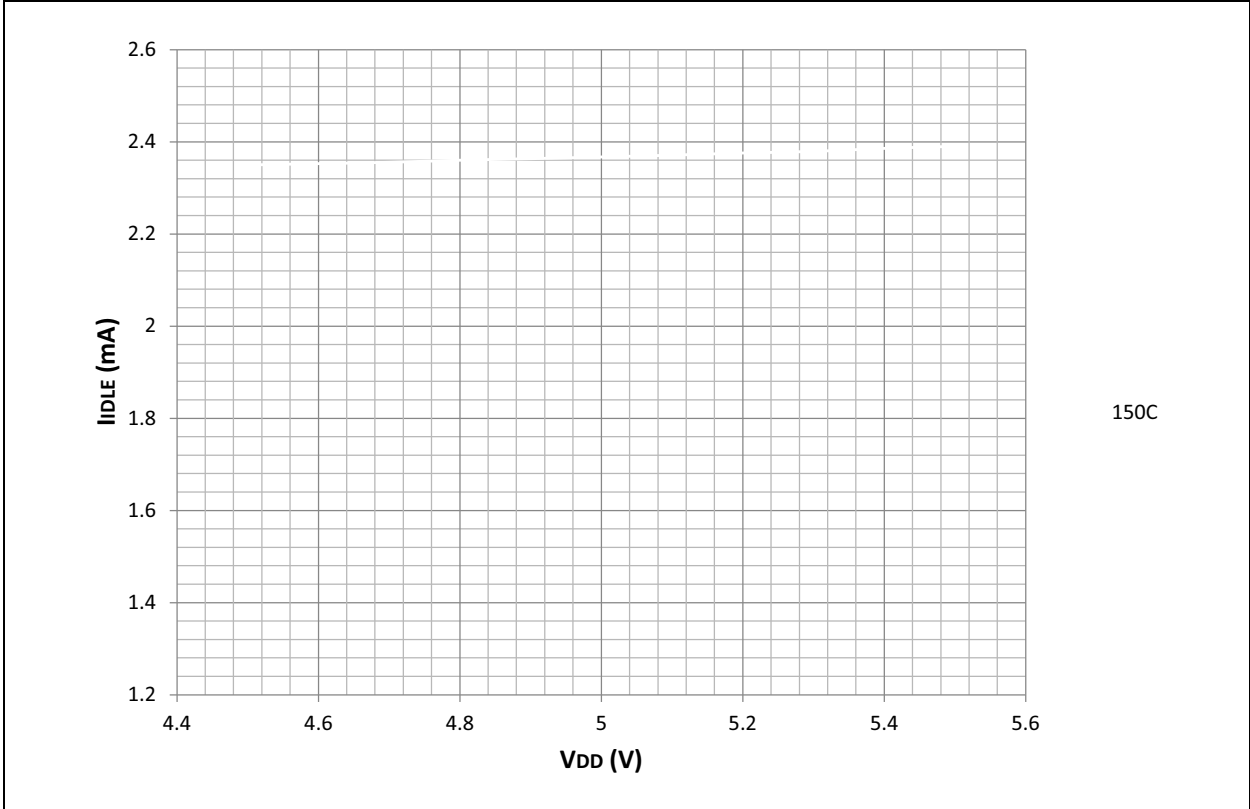
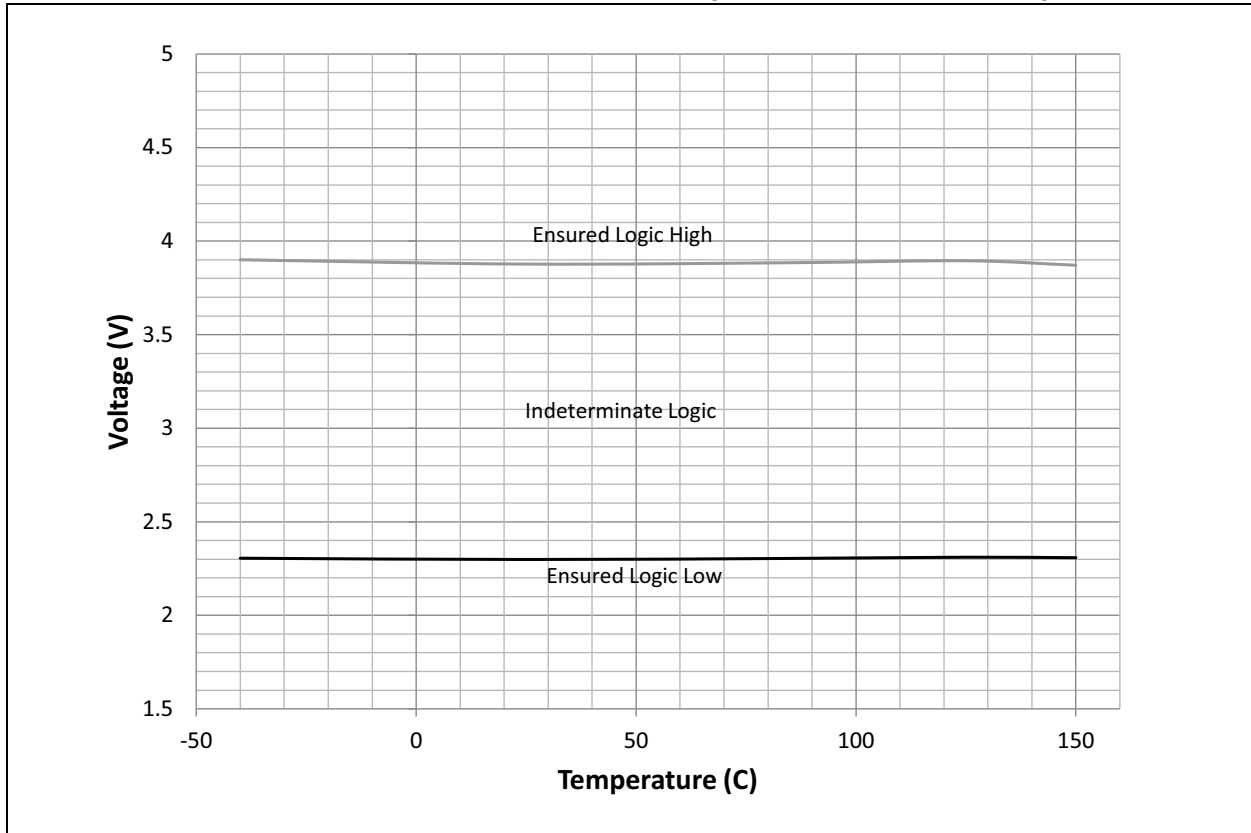


FIGURE 33-6: TYPICAL I_{IDLE} vs. V_{DD} (EC MODE, 10 MIPS)



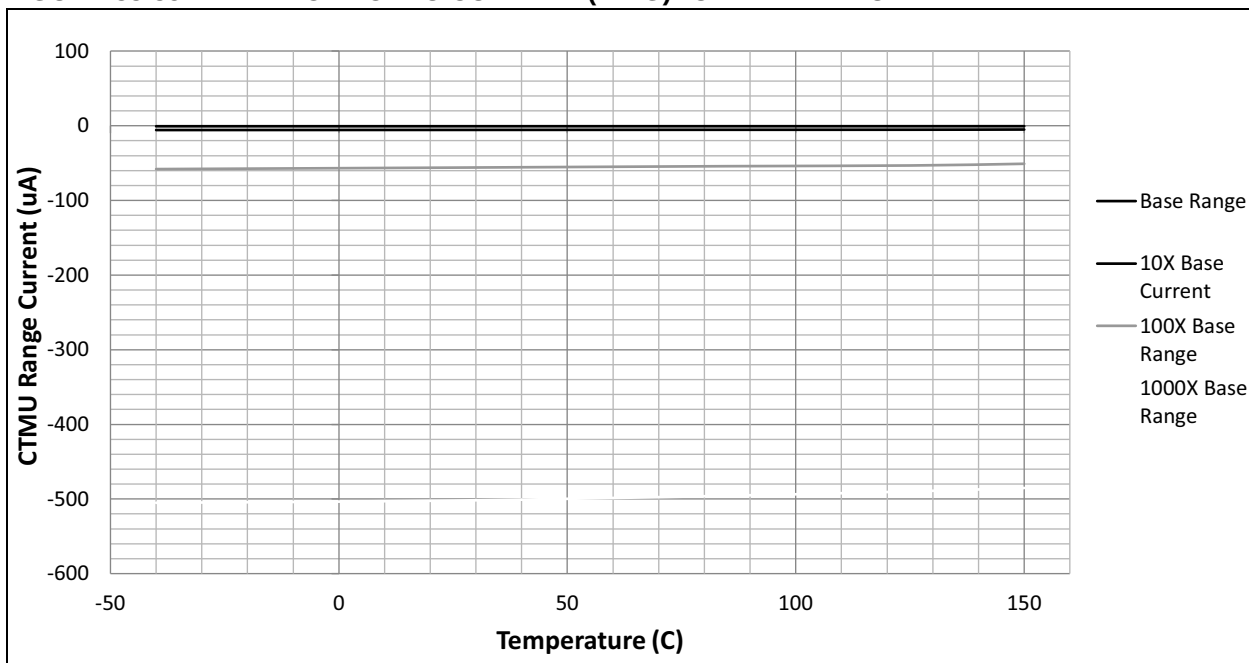
33.9 Voltage Input High (V_{IH}) – Voltage Input Low (V_{IL})

FIGURE 33-25: TYPICAL V_{IH}/V_{IL} vs. TEMPERATURE (GENERAL PURPOSE I/Os)



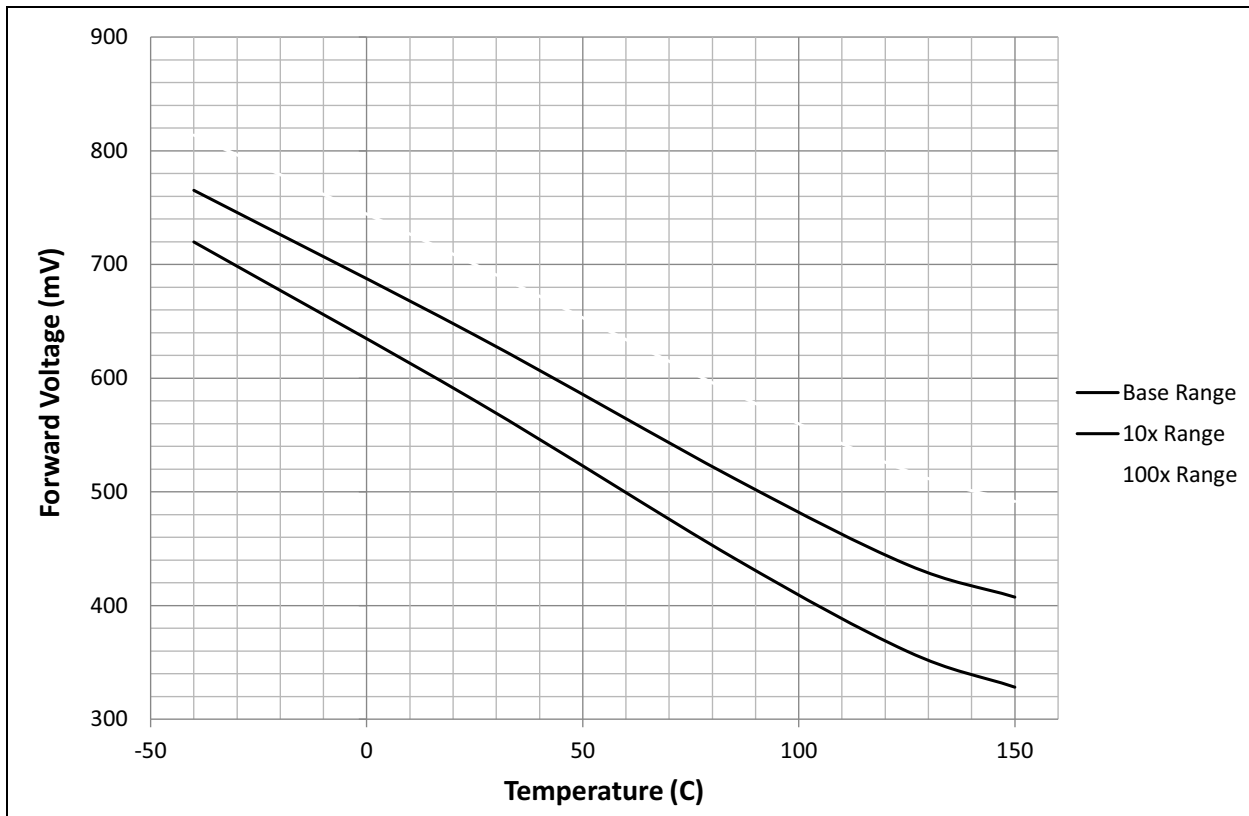
33.15 CTMU Current V/S Temperature

FIGURE 33-35: TYPICAL CTMU CURRENT (IRNG) vs. TEMPERATURE



33.16 CTMU Temperature Forward Diode (V)

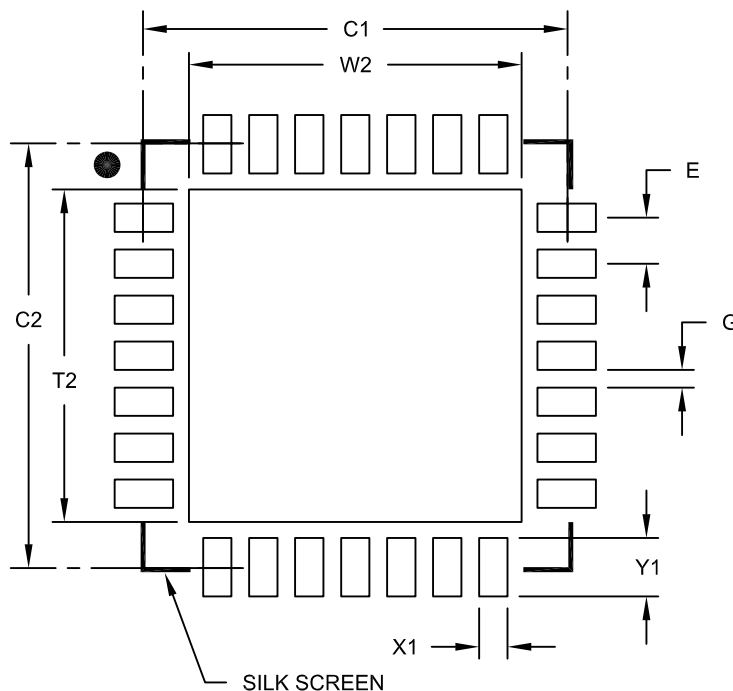
FIGURE 33-36: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE vs. TEMPERATURE



dsPIC33EVXXXGM00X/10X FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A