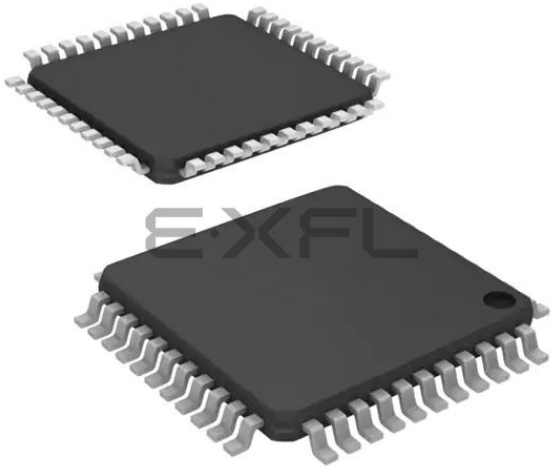
Microchip Technology - DSPIC33EV256GM104T-I/PT Datasheet



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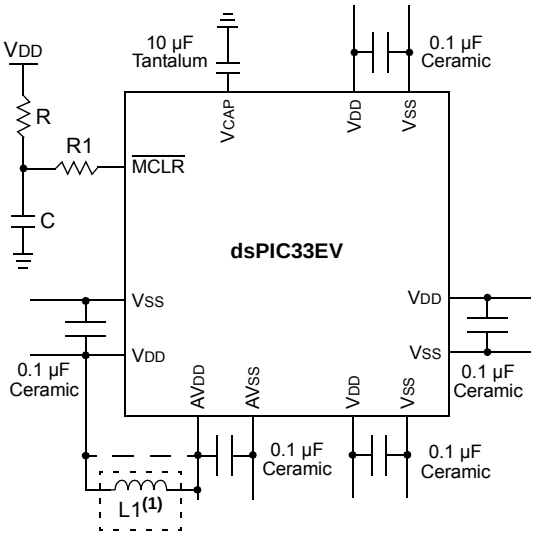
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm104t-i-pt

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC Conversion Rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (<1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 µF (10 µF is recommended), with at least a 16V rating connected to the ground. The type can be ceramic or tantalum. See **Section 30.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length should not exceed one-quarter inch (6 mm).

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

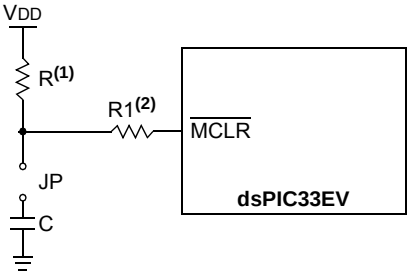
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-1, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

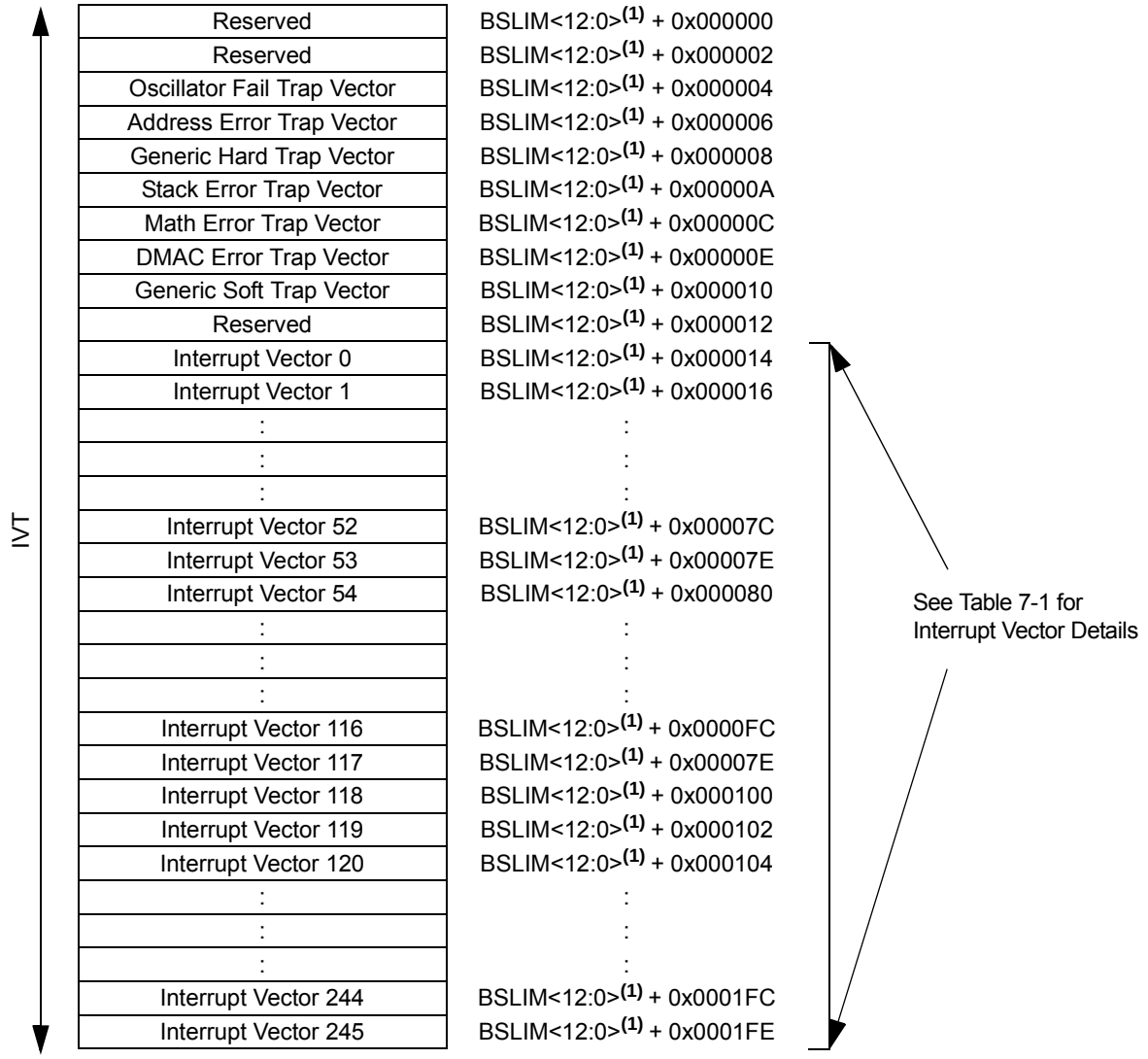
FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flow into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

FIGURE 7-1: dsPIC33EVXXXGM00X/10X FAMILY ALTERNATE INTERRUPT VECTOR TABLE



Note 1: The address depends on the size of the Boot Segment defined by BSLIM<12:0>: [(BSLIM<12:0> – 1) x 0x400] + Offset.

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMT	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **DMT:** Deadman Timer (Soft) Trap Status bit
1 = Deadman Timer trap has occurred
0 = Deadman Timer trap has not occurred

bit 14-6 **Unimplemented:** Read as ‘0’

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as ‘0’

8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access (DMA)"** (DS70348) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM. For the simplified DMA block diagram, refer to Figure 8-1.

In addition, DMA can access the entire data memory space. The data memory bus arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. The peripherals supported by the DMA Controller include:

- CAN
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: PERIPHERAL TO DMA CONTROLLER

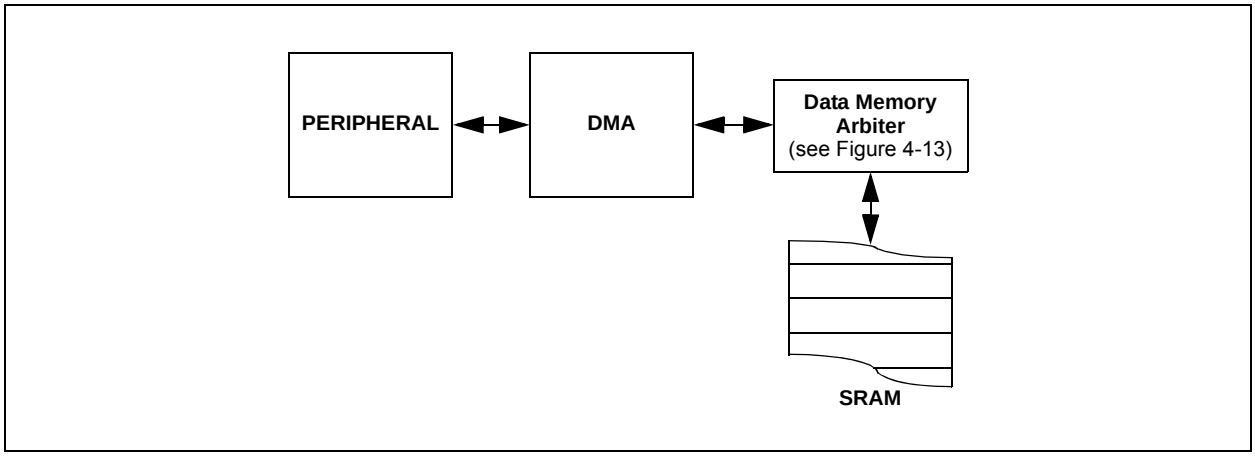


TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss
000 0001	I	CMP1(1)
000 0010	I	CMP2(1)
000 0011	I	CMP3(1)
000 0100	I	CMP4(1)
000 0101	—	—
000 1100	I	CMP5(1)
000 1101	—	—
000 1110	—	—
000 1111	—	—
001 0000	I	RPI16
001 0001	I	RPI17
001 0010	I	RPI18
001 0011	I	RPI19
001 0100	I/O	RP20
001 0101	—	—
001 0110	—	—
001 0111	—	—
001 1000	I	RPI24
001 1001	I	RPI25
001 1010	—	—
001 1011	I	RPI27
001 1100	I	RPI28
001 1101	—	—
001 1110	—	—
001 1111	—	—
010 0000	I	RPI32
010 0001	I	RPI33
010 0010	I	RPI34
010 0011	I/O	RP35
010 0100	I/O	RP36
010 0101	I/O	RP37
010 0110	I/O	RP38
010 0111	I/O	RP39
010 1000	I/O	RP40
010 1100	I	RPI44
010 1101	I	RPI45
010 1110	I	RPI46
010 1111	I	RPI47
011 0000	I/O	RP48
011 0010	I	RPI50
011 0011	I	RPI51
011 0100	I	RPI52
011 0101	I	RPI53
011 0110	I/O	RP54
011 0111	I/O	RP55
011 1000	I/O	RP56
011 1001	I/O	RP57
011 1010	I	RPI58
011 1011	—	—
011 1100	I	RPI60
011 1101	I	RPI61
011 1110	—	—
011 1111	I	RPI 63
100 0000	—	—
100 0001	—	—
100 0010	—	—
100 0011	—	—
100 0100	—	—
100 0101	I/O	RP69
100 0110	I/O	RP70
100 0111	—	—
100 1000	I	RPI72
100 1001	—	—
100 1010	—	—
100 1011	—	—
100 1110	—	—
100 1111	—	—
101 0010	—	—
101 0011	—	—
101 0100	—	—
010 1001	I/O	RP41
010 1010	I/O	RP42
010 1011	I/O	RP43
101 1000	—	—
101 1001	—	—
101 1010	—	—
101 1011	—	—
101 1100	—	—
101 1101	—	—

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

Note 1: These are virtual pins. See **Section 11.5.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When Set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When Set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWMx time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
3: DTC<1:0> = 11 for DTCP to be effective; else, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA® encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or has completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register (TSR) Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for transmit operation.

REGISTER 22-19: CxFMSKSEL2: CANx FILTERS 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK‘	F13MSK0	F12MSK1	F12MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK<1:0>:** Mask Source for Filter 15 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain the mask
01 = Acceptance Mask 1 registers contain the mask
00 = Acceptance Mask 0 registers contain the mask

bit 13-12 **F14MSK<1:0>:** Mask Source for Filter 14 bit (same values as bits 15-14)

bit 11-10 **F13MSK<1:0>:** Mask Source for Filter 13 bit (same values as bits 15-14)

bit 9-8 **F12MSK<1:0>:** Mask Source for Filter 12 bit (same values as bits 15-14)

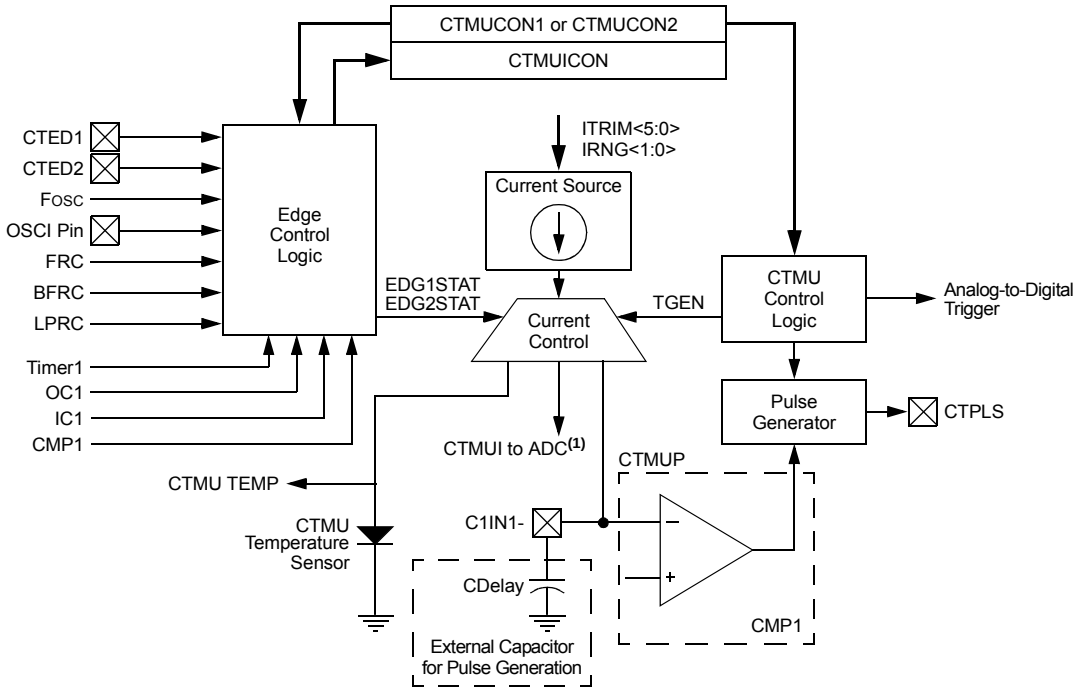
bit 7-6 **F11MSK<1:0>:** Mask Source for Filter 11 bit (same values as bits 15-14)

bit 5-4 **F10MSK<1:0>:** Mask Source for Filter 10 bit (same values as bits 15-14)

bit 3-2 **F9MSK<1:0>:** Mask Source for Filter 9 bit (same values as bits 15-14)

bit 1-0 **F8MSK<1:0>:** Mask Source for Filter 8 bit (same values as bits 15-14)

FIGURE 23-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMU TEMP	0	EDG1STAT = EDG2STAT
CTMUI to ADC	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

Note 1: Current source to particular ANx pins is provided only when 10-Bit ADC mode is chosen.

REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	CH0SB5(1,3)	CH0SB4(1,3)	CH0SB3(1,3)	CH0SB2(1,3)	CH0SB1(1,3)	CH0SB0(1,3)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	CH0SA5(1,3)	CH0SA4(1,3)	CH0SA3(1,3)	CH0SA2(1,3)	CH0SA1(1,3)	CH0SA0(1,3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUX B bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CH0SB<5:0>:** Channel 0 Positive Input Select for Sample MUX B bits(1,3)
111111 = Channel 0 positive input is AN63
111110 = Channel 0 positive input is AN62
111101 = Channel 0 positive input is AN61 (internal band gap voltage)
•
•
•
011111 = Channel 0 positive input is AN31
011110 = Channel 0 positive input is AN30
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 (Op Amp 2)(2)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUX A bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6 **Unimplemented:** Read as '0'

Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2) (CONTINUED)

bit 1 **CSS17:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 0 **CSS16:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

25.1 Op Amp/Comparator Control Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
PSIDL	—	—	C5EVT(1)	C4EVT(1)	C3EVT(1)	C2EVT(1)	C1EVT(1)
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	C5OUT(2)	C4OUT(2)	C3OUT(2)	C2OUT(2)	C1OUT(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PSIDL:** Op Amp/Comparator Stop in Idle Mode bit
1 = Discontinues operation of all op amps/comparators when device enters Idle mode
0 = Continues operation of all op amps/comparators in Idle mode

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **C5EVT:C1EVT:** Op Amp/Comparator 1-5 Event Status bits(1)
1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **C5OUT:C1OUT:** Op Amp/Comparator 1-5 Output Status bits(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON<9>.

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON<8>.

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(2)

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator 4 Reference Select bit (VIN+ input)(1)

1 = VIN+ input connects to the internal CVREFIN voltage
0 = VIN+ input connects to the C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Comparator 4 Channel Select bits(1)

11 = VIN- input of comparator connects to the C4IN4- pin
10 = VIN- input of comparator connects to the C4IN3- pin
01 = VIN- input of comparator connects to the C4IN2- pin
00 = VIN- input of comparator connects to the C4IN1- pin

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

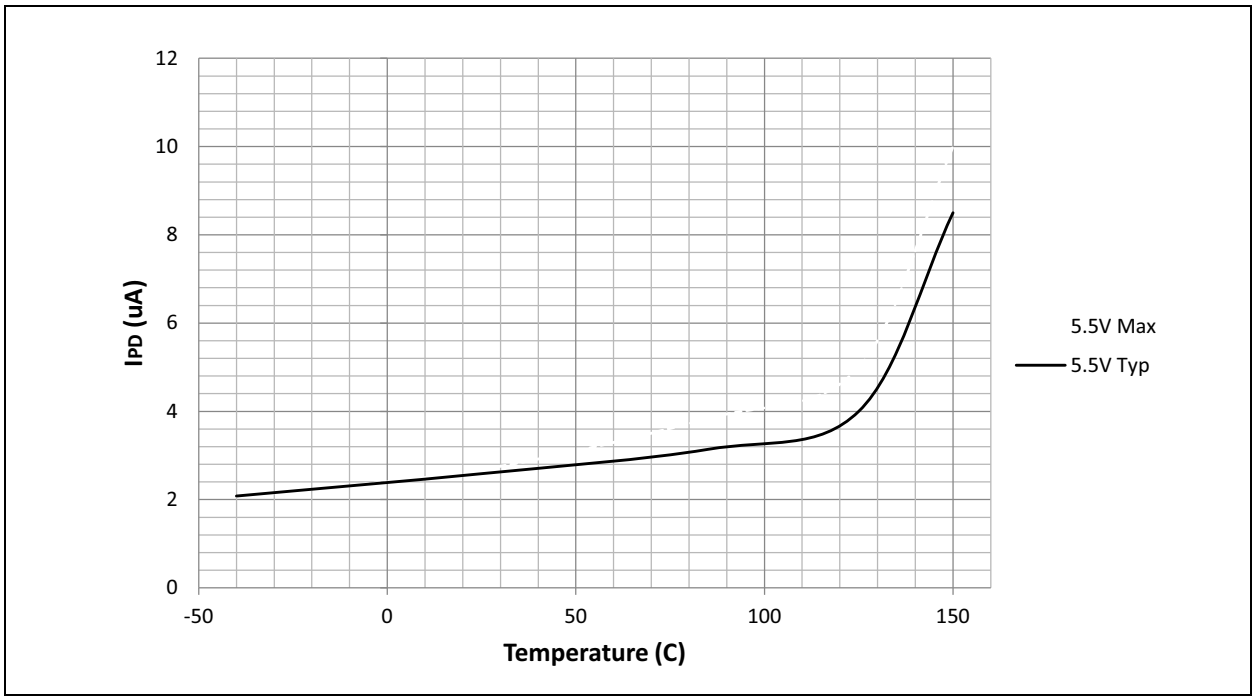
Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
8	BSW	BSW.C Ws,Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z Ws,Wb	Write Z bit to Ws<Wb>	1	1	None
9	BTG	BTG f,#bit4	Bit Toggle f	1	1	None
		BTG Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f,#bit4	Bit Test f	1	1	Z
		BTST.C Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C Ws,Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z Ws,Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call subroutine	2	4	SFA
		CALL Wn	Call indirect subroutine	1	4	SFA
		CALL.L Wn	Call indirect subroutine (long address)	1	4	SFA
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR Ws	Ws = 0x0000	1	1	None
		CLR Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA, SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM f	$f = \overline{f}$	1	1	N,Z
		COM f,WREG	$WREG = \overline{f}$	1	1	N,Z
		COM Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,Ws	Compare Wb with Ws, with Borrow ($Wb – Ws – \overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb,Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ Wb,Wn,Expr	Compare Wb with Wn, branch if =	1	1 (5)	None
22	CPSGT	CPSGT Wb,Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT Wb,Wn,Expr	Compare Wb with Wn, branch if >	1	1 (5)	None
23	CPSLT	CPSLT Wb,Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT Wb,Wn,Expr	Compare Wb with Wn, branch if <	1	1 (5)	None
24	CPSNE	CPSNE Wb,Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE Wb,Wn,Expr	Compare Wb with Wn, branch if ≠	1	1 (5)	None

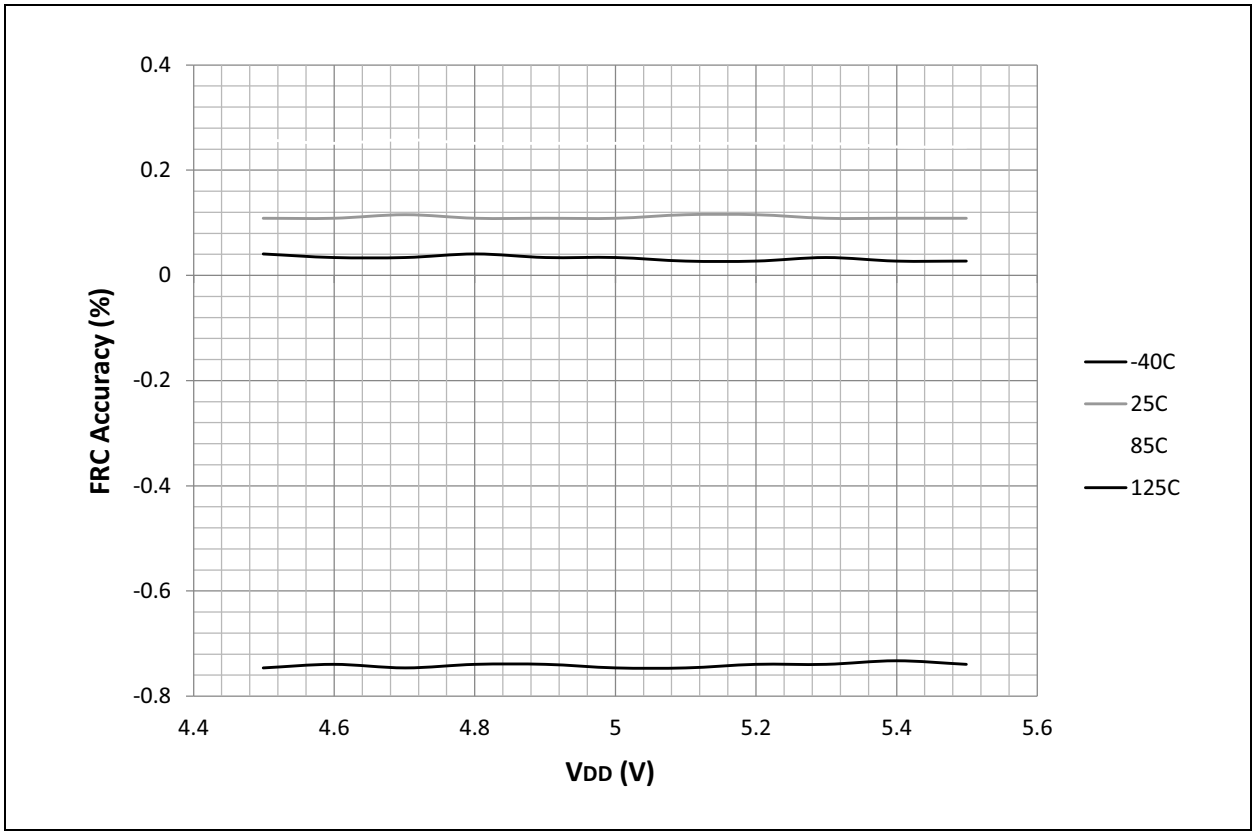
Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 32-19: TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE



32.5 FRC

FIGURE 32-20: TYPICAL FRC ACCURACY vs. VDD



NOTES: