Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm106-e-mr

dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.

TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES

Device	Program Memory Bytes	SRAM Bytes	CAN	DMA Channels	16-Bit Timers (T1)	32-Bit Timers	Input Capture	Output Compare	PWM	UART	SPI	I²C	SENT	10/12-Bit ADC	ADC Inputs	Op Amp/Comparators	CTMU	Security	Peripheral Pin Select (PPS)	General Purpose I/O (GPIO)	External Interrupts	Pins	Packages
dsPIC33EV32GM002	32K	4K	0																				
dsPIC33EV32GM102			1																				
dsPIC33EV64GM002	64K	8K	0																				
dsPIC33EV64GM102			1	4	5	2	4	4	3x2	2	2	1	2	1	11	3/4	1	Intermediate	Y	21	3	28	SPDIP, SOIC, SSOP, QFN-S
dsPIC33EV128GM002	128K	8K	0																				
dsPIC33EV128GM102			1																				
dsPIC33EV256GM002	256K	16K	0																				
dsPIC33EV256GM102			1																				
dsPIC33EV32GM004	32K	4K	0																				
dsPIC33EV32GM104			1																				
dsPIC33EV64GM004	64K	8K	0																				
dsPIC33EV64GM104			1	4	5	2	4	4	3x2	2	2	1	2	1	24	4/5	1	Intermediate	Y	35	3	44	TQFP, QFN
dsPIC33EV128GM004	128K	8K	0																				
dsPIC33EV128GM104			1																				
dsPIC33EV256GM004	256K	16K	0																				
dsPIC33EV256GM104			1																				
dsPIC33EV32GM006	32K	4K	0																				
dsPIC33EV32GM106			1																				
dsPIC33EV64GM006	64K	8K	0																				
dsPIC33EV64GM106			1	4	5	2	4	4	3x2	2	2	1	2	1	36	4/5	1	Intermediate	Y	53	3	64	TQFP, QFN
dsPIC33EV128GM006	128K	8K	0																				
dsPIC33EV128GM106			1																				
dsPIC33EV256GM006	256K	16K	0																				
dsPIC33EV256GM106			1																				

dsPIC33EVXXXGM00X/10X FAMILY

Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip web site (www.microchip.com). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- **"Introduction"** (DS70573)
- **"CPU"** (DS70359)
- **"Data Memory"** (DS70595)
- **"dsPIC33E/PIC24E Program Memory"** (DS70000613)
- **"Flash Programming"** (DS70609)
- **"Interrupts"** (DS70000600)
- **"Oscillator"** (DS70580)
- **"Reset"** (DS70602)
- **"Watchdog Timer and Power-Saving Modes"** (DS70615)
- **"I/O Ports"** (DS70000598)
- **"Timers"** (DS70362)
- **"CodeGuard™ Intermediate Security"** (DS70005182)
- **"Deadman Timer (DMT)"** (DS70005155)
- **"Input Capture"** (DS70000352)
- **"Output Compare"** (DS70005157)
- **"High-Speed PWM"**(DS70645)
- **"Analog-to-Digital Converter (ADC)"** (DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582)
- **"Serial Peripheral Interface (SPI)"** (DS70005185)
- **"Inter-Integrated Circuit™ (I^{2}C™)"** (DS70000195)
- **"Enhanced Controller Area Network (ECAN™)"**(DS70353)
- **"Direct Memory Access (DMA)"** (DS70348)
- **"Programming and Diagnostics"** (DS70608)
- **"Op Amp/Comparator"** (DS70000357)
- **"Device Configuration"** (DS70000618)
- **"Charge Time Measurement Unit (CTMU)"** (DS70661)
- **"Single-Edge Nibble Transmission (SENT) Module"** (DS70005145)

1.0   DEVICE OVERVIEW

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EVXXXGM00X/10X family Digital Signal Controller (DSC) devices.

dsPIC33EVXXXGM00X/10X family devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.
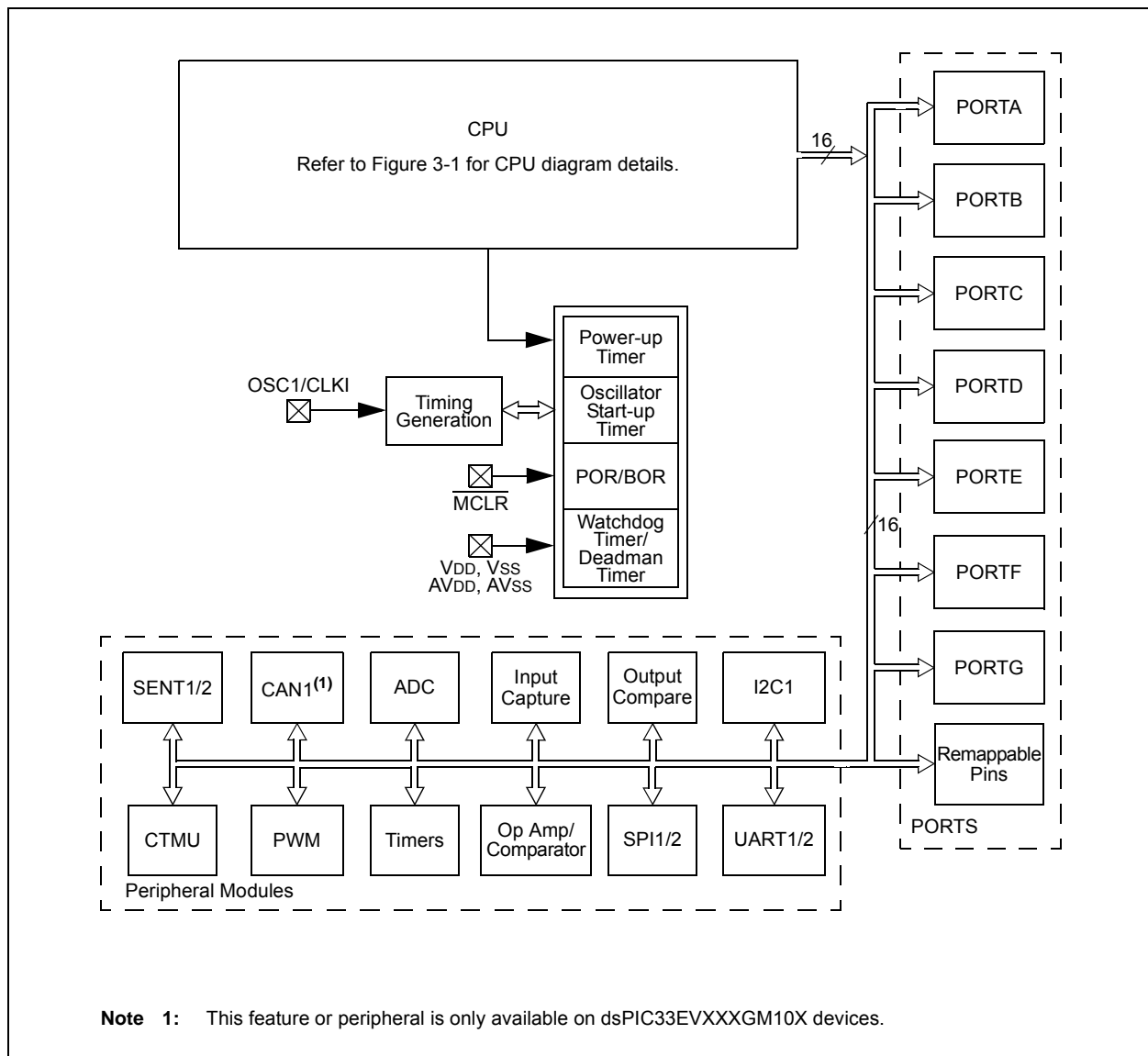
FIGURE 1-1:   **dsPIC33EVXXXGM00X/10X FAMILY BLOCK DIAGRAM**

Note 1: This feature or peripheral is only available on dsPIC33EVXXXGM10X devices.

TABLE 4-2: **TIMERS REGISTER MAP**

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register															0000
PR1	0102	Period Register 1															FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register															0000
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)															0000
TMR3	010A	Timer3 Register															0000
PR2	010C	Period Register 2															FFFF
PR3	010E	Period Register 3															FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register															0000
TMR5HLD	0116	Timer5 Holding Register (For 32-bit operations only)															0000
TMR5	0118	Timer5 Register															0000
PR4	011A	Period Register 4															FFFF
PR5	011C	Period Register 5															FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 5-4: **NVMKEY: NONVOLATILE MEMORY KEY REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

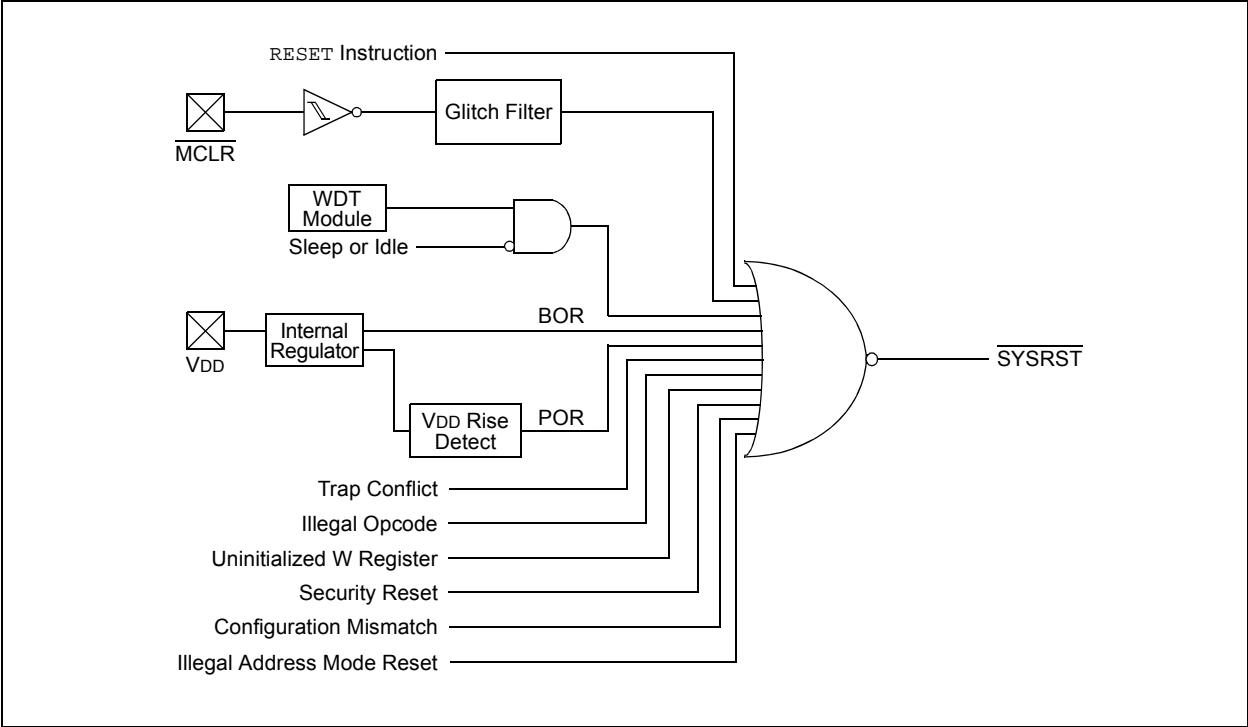| W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** NVM Key Register bits (write-only)

FIGURE 6-1: **RESET SYSTEM BLOCK DIAGRAM**

7.0 INTERRUPT CONTROLLER

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EVXXXGM00X/10X CPU. The Interrupt Vector Table (IVT) provides 246 interrupt sources (unused sources are reserved for future use) that can be programmed with different priority levels.

The interrupt controller has the following features:

- Interrupt Vector Table with up to 246 Vectors
- Alternate Interrupt Vector Table (AIVT)
- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Software can Generate any Peripheral Interrupt
- Alternate Interrupt Vector Table (AIVT) is available if Boot Security is Enabled and AIVTEN = 1

7.1 Interrupt Vector Table

The dsPIC33EVXXXGM00X/10X family IVT, shown in Figure 7-2, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 187 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-1, is available if the Boot Segment (BS) is defined, the AIVTEN bit is set in the INTCON2 register and if the AIVTDIS Configuration bit is set to '1'. The AIVT begins at the start of the last page of the Boot Segment.

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			T2CKR<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7-0   **T2CKR<7:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
-
-
-
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT1R<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SENT1R<7:0>:** Assign SENT Module Input 1 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT2R<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **SENT2R<7:0>:** Assign SENT Module Input 2 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000= Input tied to Vss

REGISTER 14-3: **DMTCLR: DEADMAN TIMER CLEAR REGISTER**

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STEP2<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2<7:0>:** DMT Clear Timer bits

00001000 = Clears STEP1<7:0>, STEP2<7:0> and the Deadman Timer if preceded by the correct loading of the STEP1<7:0> bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H register and observing the counter being reset.

All Other

Write Patterns = Sets the BAD2 bit; the value of STEP1<7:0> will remain unchanged and the new value being written to STEP2<7:0> will be captured. These bits are cleared when a DMT Reset event occurs.

REGISTER 17-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPER<15:8>				
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
			PTPER<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

REGISTER 17-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTCMP<15:8>				
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTCMP<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SEVTCMP<15:0>:** Special Event Compare Count Value bits

REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 **S:** I2Cx Start bit

Updated when Start, Reset or Stop is detected; cleared when the I²C module is disabled, I2CEN = 0.

1 = Indicates that a Start (or Repeated Start) bit has been detected last

0 = Indicates that a Start bit was not detected last

bit 2 **R_W:** Read/Write Information bit (when operating as I²C slave)

1 = Read: Indicates that the data transfer is output from the slave

0 = Write: Indicates that the data transfer is input to the slave

bit 1 **RBF:** Receive Buffer Full Status bit

1 = Receive is complete, the I2CxRCV bit is full

0 = Receive is not complete, the I2CxRCV bit is empty

bit 0 **TBF:** Transmit Buffer Full Status bit

1 = Transmit is in progress, I2CxTRN is full (8 bits of data)

0 = Transmit is complete, I2CxTRN is empty

REGISTER 19-4: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	MSK<9:8>	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSK<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **MSK<9:0>:** I2Cx Mask for Address Bit x Select bits

1 = Enables masking for bit x of the incoming message address; bit match is not required in this position

0 = Disables masking for bit x; bit match is required in this position

20.2 Transmit Mode

By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME<15:0> (SENTxCON2<15:0>) bits. The tick period calculations are shown in Equation 20-1.

EQUATION 20-1: TICK PERIOD CALCULATION

$$TICKTIME\text{<}15:0\text{>} = \frac{T_{TICK}}{T_{CLK}} - 1$$

An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing a value to the FRAMETIME<15:0> (SENTxCON3<15:0>) bits. The formulas used to calculate the value of frame time are shown in Equation 20-2.

EQUATION 20-2: FRAME TIME CALCULATIONS

$$FRAMETIME\text{<}15:0\text{>} = T_{TICK}/T_{FRAME}$$

$$FRAMETIME\text{<}15:0\text{>} \geq 122 + 27N$$

$$FRAMETIME\text{<}15:0\text{>} \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME<15:0> value. FRAMETIME<15:0> values beyond 2047 will have no effect on the length of a data frame.

20.2.1 TRANSMIT MODE CONFIGURATION

20.2.1.1 Initializing the SENTx Module:

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1<11>) = 0 for Transmit mode.
2. Write TXM (SENTxCON1<10>) = 0 for Asynchronous Transmit mode or TXM = 1 for Synchronous mode.
3. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
4. Write CRCEN (SENTxCON1<8>) for hardware or software CRC calculation.
5. Write PPP (SENTxCON1<7>) for optional pause pulse.
6. If PPP = 1, write T_FRAME to SENTxCON3.
7. Write SENTxCON2 with the appropriate value for desired tick period.
8. Enable interrupts and set interrupt priority.
9. Write initial status and data values to SENTxDATH/L.
10. If CRCEN = 0, calculate CRC and write the value to CRC<3:0> (SENTxDATL<3:0>).
11. Set the SNTEN (SENTxCON1<15>) bit to enable the module.

User software updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

REGISTER 20-2:   SENTxSTAT: SENTx STATUS REGISTER (CONTINUED)

bit 0   **SYNCTXEN:** SENTx Synchronization Period Status/Transmit Enable bit**(1)**

Module in Receive Mode (RCVEN = 1):

1 = A valid synchronization period was detected; the module is receiving nibble data

0 = No synchronization period has been detected; the module is not receiving nibble data

Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):

The bit always reads as '1' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads '0' when the module is disabled.

Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):

1 = The module is transmitting a SENTx data frame

0 = The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission

Note 1:   In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER (CONTINUED)

bit 1   **RBIF:** RX Buffer Interrupt Flag bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0   **TBIF:** TX Buffer Interrupt Flag bit

1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 22-7: CxINTE: CANx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8   **Unimplemented:** Read as '0'

bit 7   **IVRIE:** Invalid Message Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6   **WAKIE:** Bus Wake-up Activity Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5   **ERRIE:** Error Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4   **Unimplemented:** Read as '0'

bit 3   **FIFOIE:** FIFO Almost Full Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2   **RBOVIE:** RX Buffer Overflow Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1   **RBIE:** RX Buffer Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0   **TBIE:** TX Buffer Interrupt Enable bit

1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 23-3: CTMUICON: CTMU CURRENT CONTROL REGISTER[3]

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1[2]	IRNG0[2]
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM<5:0>:** Current Source Trim bits

011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%
•
•
•
000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%
•
•
•
100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG<1:0>:** Current Source Range Select bits[2]

11 = 100 × Base Current
10 = 10 × Base Current
01 = Base Current Level
00 = 1000 × Base Current[1]

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This current range is not available for use with the internal temperature measurement diode.

2: Refer to the CTMU Current Source Specifications (Table 30-53) in **Section 30.0 "Electrical Characteristics"** for the current range selection values.

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

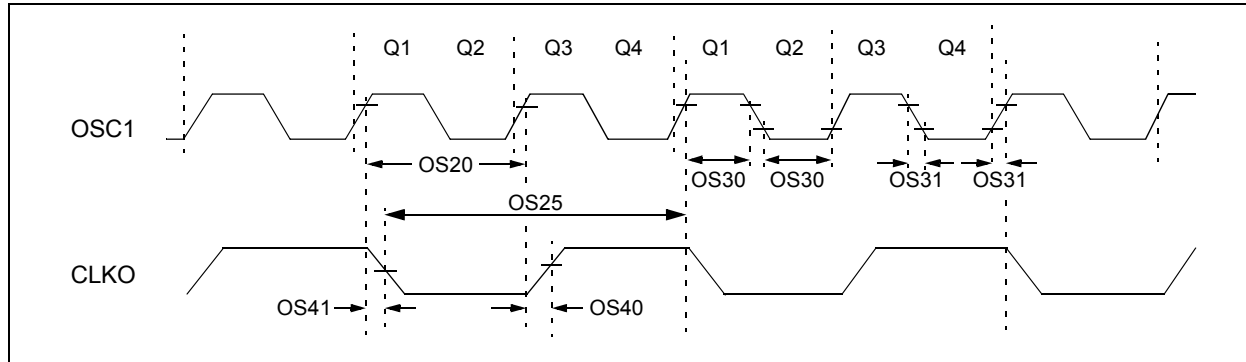**FIGURE 30-2:** **EXTERNAL CLOCK TIMING**

TABLE 30-17: **EXTERNAL CLOCK TIMING REQUIREMENTS**

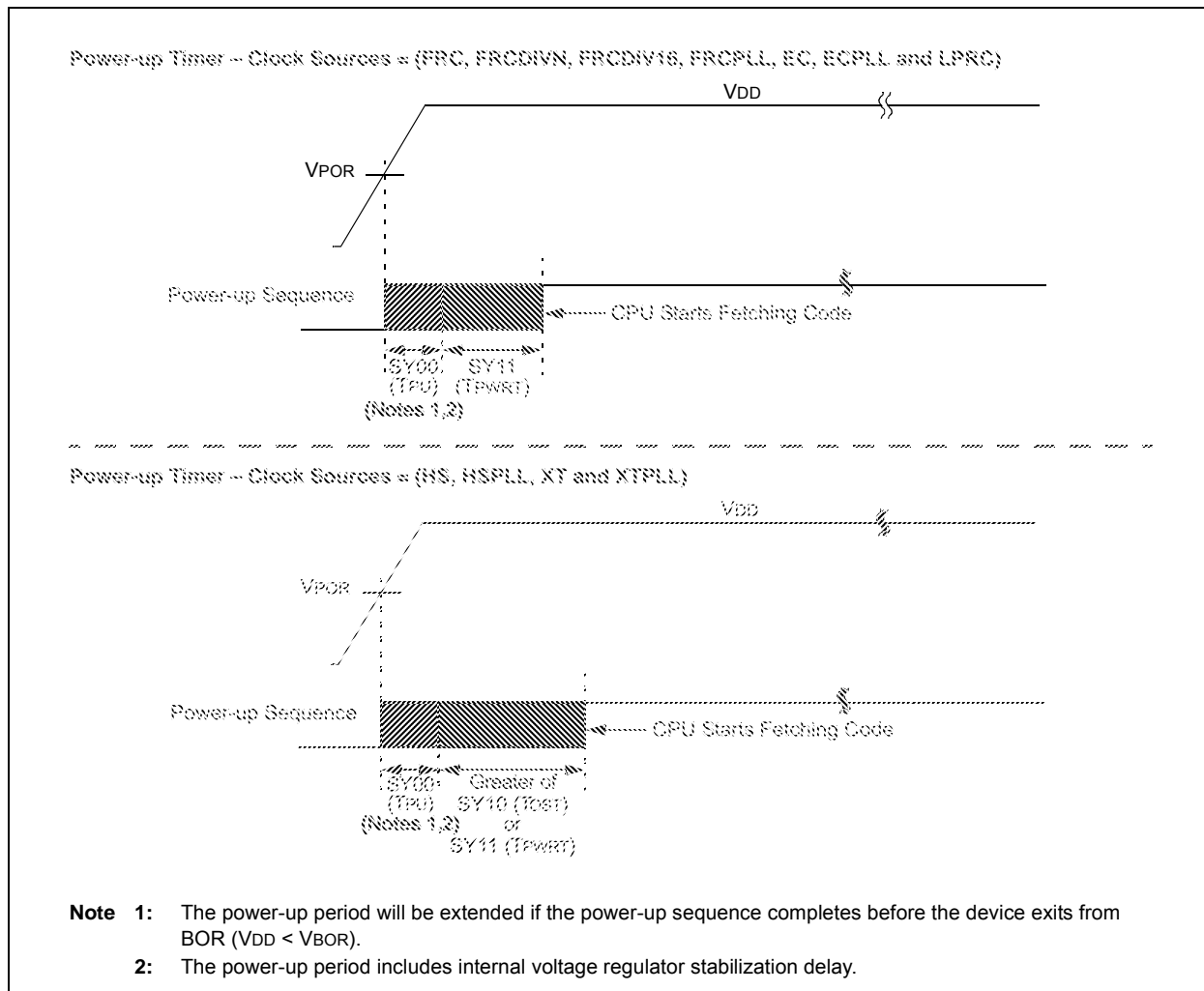| AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Sym	Characteristic	Min.	Typ.[1]	Max.	Units	Conditions
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	40	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 25	MHz MHz	XT HS
OS20	TOSC	TOSC = 1/FOSC	12.5	—	DC	ns	TA = +125°C
OS25	TCY	Instruction Cycle Time[2]	25	—	DC	ns	TA = +125°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x TOSC	—	0.625 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time[3]	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time[3]	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance[4]	—	12	—	mA/V	HS, VDD = 5.0V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 5.0V, TA = +25°C

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: This parameter is characterized but not tested in manufacturing.

FIGURE 30-5: **POWER-ON RESET TIMING CHARACTERISTICS**

Power-up Timer – Clock Sources = (FRC, FRCDIVN, FRCDIV16, FRCPLL, EC, ECPLL and LPRC)

VDD

VPOR

Power-up Sequence

CPU Starts Fetching Code

SY00 SY11
(TPU) (TPWRT)
(Notes 1,2)

Power-up Timer – Clock Sources = (HS, HSPLL, XT and XTPLL)

VDD

VPOR

Power-up Sequence

CPU Starts Fetching Code

SY00 Greater of
(TPU) SY10 (TOST)
(Notes 1,2) or
SY11 (TPWRT)

Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR (VDD < VBOR).

2: The power-up period includes internal voltage regulator stabilization delay.

32.8   Pull-up and Pull-Down Current

FIGURE 32-27:   TYPICAL PULL-UP CURRENT (V_{PIN} = V_{SS}) vs. TEMPERATURE
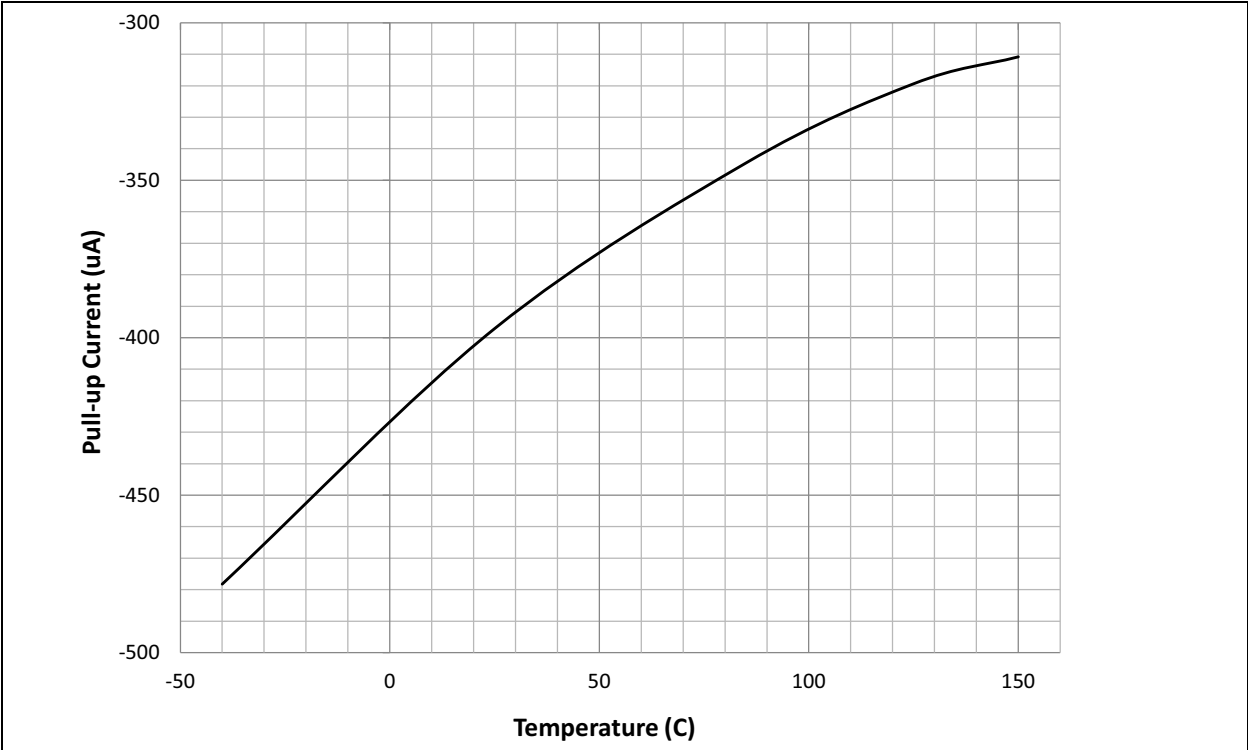
FIGURE 32-28:   TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE
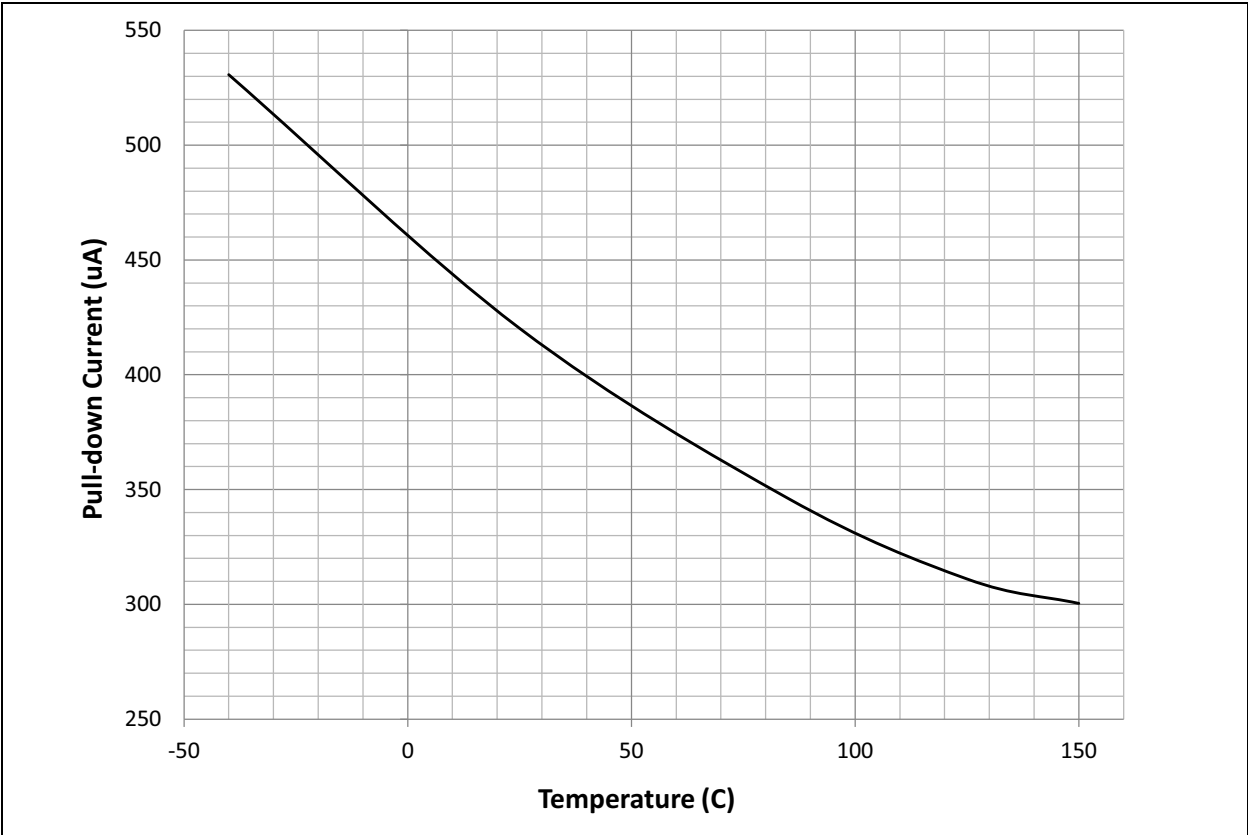
FIGURE 33-11: TYPICAL I_{DOZE} vs. V_{DD} (DOZE 1:128, 70 MIPS)
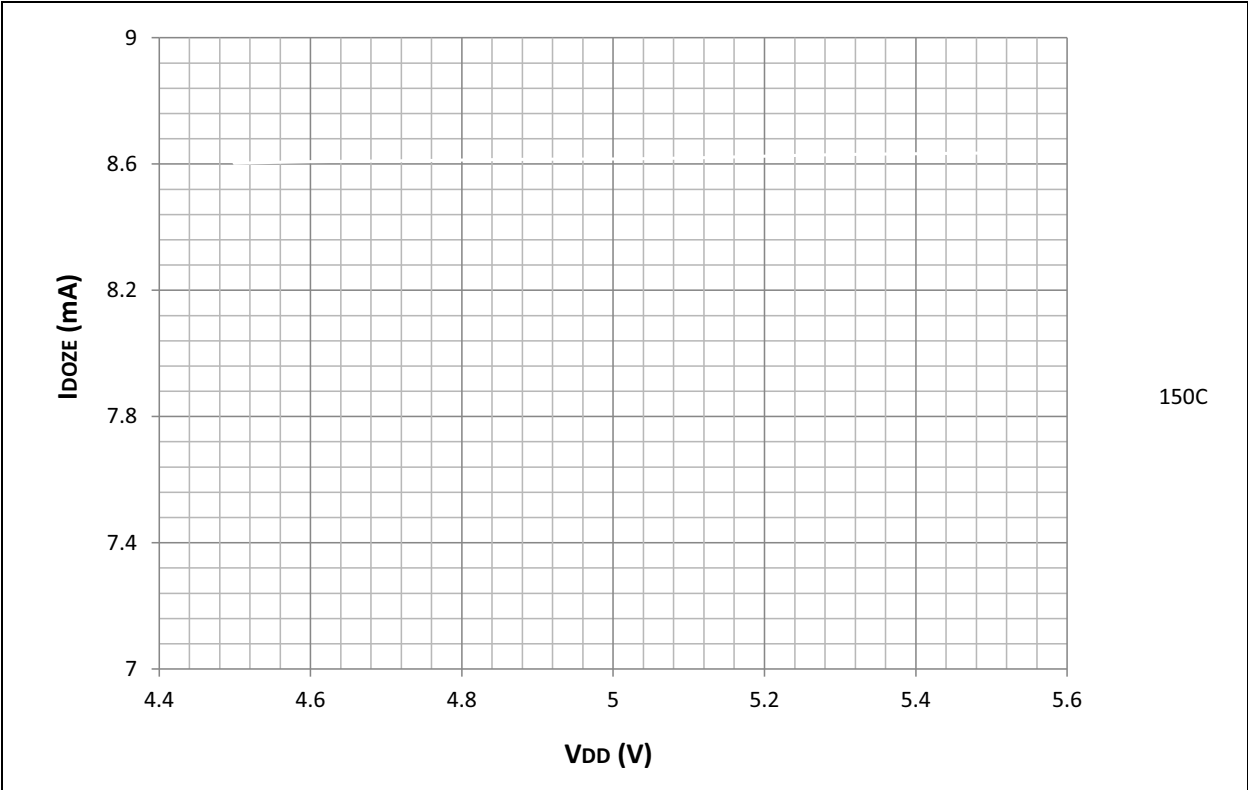

FIGURE 33-12: TYPICAL/MAXIMUM I_{DOZE} vs. TEMPERATURE (DOZE 1:128, 70 MIPS)