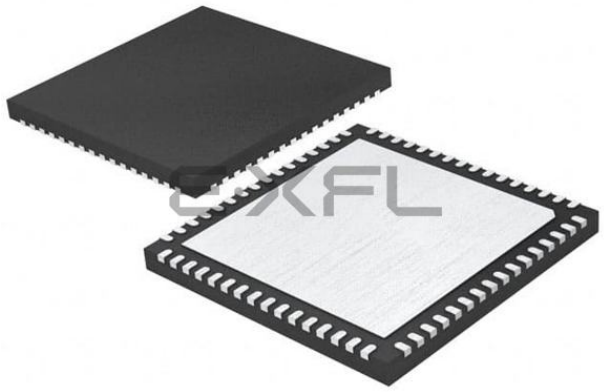

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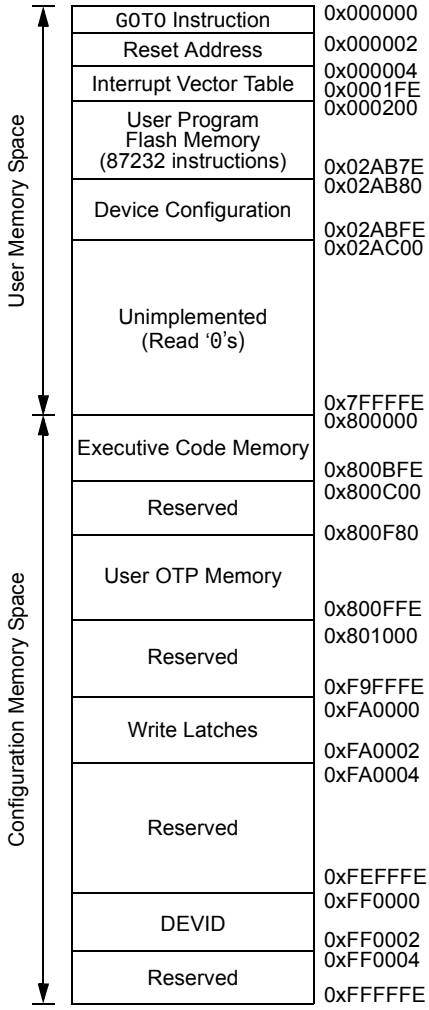
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev256gm106-i-mr

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EV256GM00X/10X DEVICES(1)



Note 1: Memory areas are not shown to scale.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
WR(1)	WREN(1)	WRERR(1)	NVMSIDL(2)	—	—	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	NVMOP3(1,3,4)	NVMOP2(1,3,4)	NVMOP1(1,3,4)	NVMOP0(1,3,4)
bit 7							bit 0

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Flash program or erase operations are enabled
- 0 = Flash program or erase operations are inhibited

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Primary Flash operation discontinues when the device enters Idle mode
- 0 = Primary Flash operation continues when the device enters Idle mode.

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **RPDF:** Row Programming Data Format Control bit
- 1 = Row data to be stored in RAM is in a compressed format
- 0 = Row data to be stored in RAM is in an uncompressed format

bit 8 **URERR:** Row Programming Data Underrun Error Flag bit
- 1 = Row programming operation has been terminated due to a data underrun error
- 0 = No data underrun has occurred

bit 7-4 **Unimplemented:** Read as '0'

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (I_{IDLE}), and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.

3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector No.	IRQ No.	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
External Interrupt 0 (INT0)	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
Input Capture 1 (IC1)	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
Output Compare 1 (OC1)	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
Timer1 (T1)	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA Channel 0 (DMA0)	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
Input Capture 2 (IC2)	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
Output Compare 2 (OC2)	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
Timer2 (T2)	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
Timer3 (T3)	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1 Error (SPI1E)	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 Transfer Done (SPI1)	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
UART1 Receiver (U1RX)	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
UART1 Transmitter (U1TX)	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
ADC1 Convert Done (AD1)	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA Channel 1 (DMA1)	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
NVM Write Complete (NVM)	23	15	0x000032	IFS0<15>	IEC0<15>	IPC3<14:12>
I2C1 Slave Event (SI2C1)	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
I2C1 Master Event (MI2C1)	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
Comparator Combined Event (CMP1)	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
Input Change Interrupt (CN)	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
External Interrupt 1 (INT1)	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
DMA Channel 2 (DMA2)	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
Output Compare 3 (OC3)	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
Output Compare 4 (OC4)	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
Timer4 (T4)	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
Timer5 (T5)	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
External Interrupt 2 (INT2)	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
UART2 Receiver (U2RX)	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
UART2 Transmitter (U2TX)	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2 Error (SPI2E)	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 Transfer Done (SPI2)	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
CAN1 RX Data Ready (C1RX)(1)	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
CAN1 Event (C1)(1)	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA Channel 3 (DMA3)	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
Input Capture 3 (IC3)	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
Input Capture 4 (IC4)	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
Reserved	54	46	0x000070	—	—	—
PWM Special Event Match Interrupt (PSEM)	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>
Reserved	69	61	0x00008E	—	—	—
Reserved	71-72	63-64	0x000092-0x000094	—	—	—

Note 1: This interrupt source is available on dsPIC33EVXXXGM10X devices only.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
1 = DMA3STB register is selected
0 = DMA3STA register is selected

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
1 = DMA2STB register is selected
0 = DMA2STA register is selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
1 = DMA1STB register is selected
0 = DMA1STA register is selected

bit 0 **PPST0:** Channel 0 Ping-Pong mode Status Flag bit
1 = DMA0STB register is selected
0 = DMA0STA register is selected

NOTES:

14.0 DEADMAN TIMER (DMT)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Deadman Timer (DMT)"** (DS70005155) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

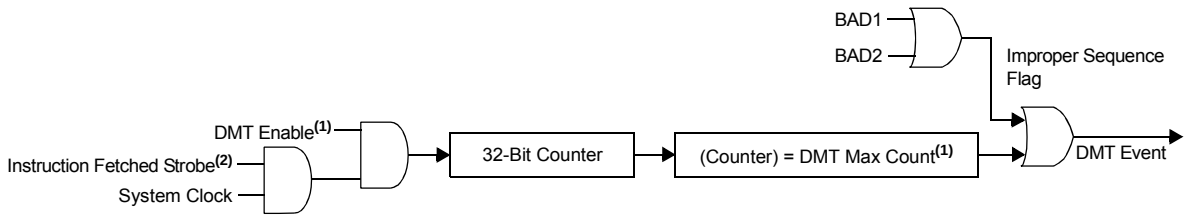
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical, and safety-critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 14-1 shows a block diagram of the Deadman Timer module.

FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.

2: DMT window interval is controlled by the value of the FDMTINTVL and FDMTINTVH Configuration registers.

REGISTER 22-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits 7-0, controls Buffer n.

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer, TRBm, is a transmit buffer
0 = Buffer, TRBm, is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQm is set.

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

Figure 25-2, shows the user-programmable blanking function block diagram.

FIGURE 25-2: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

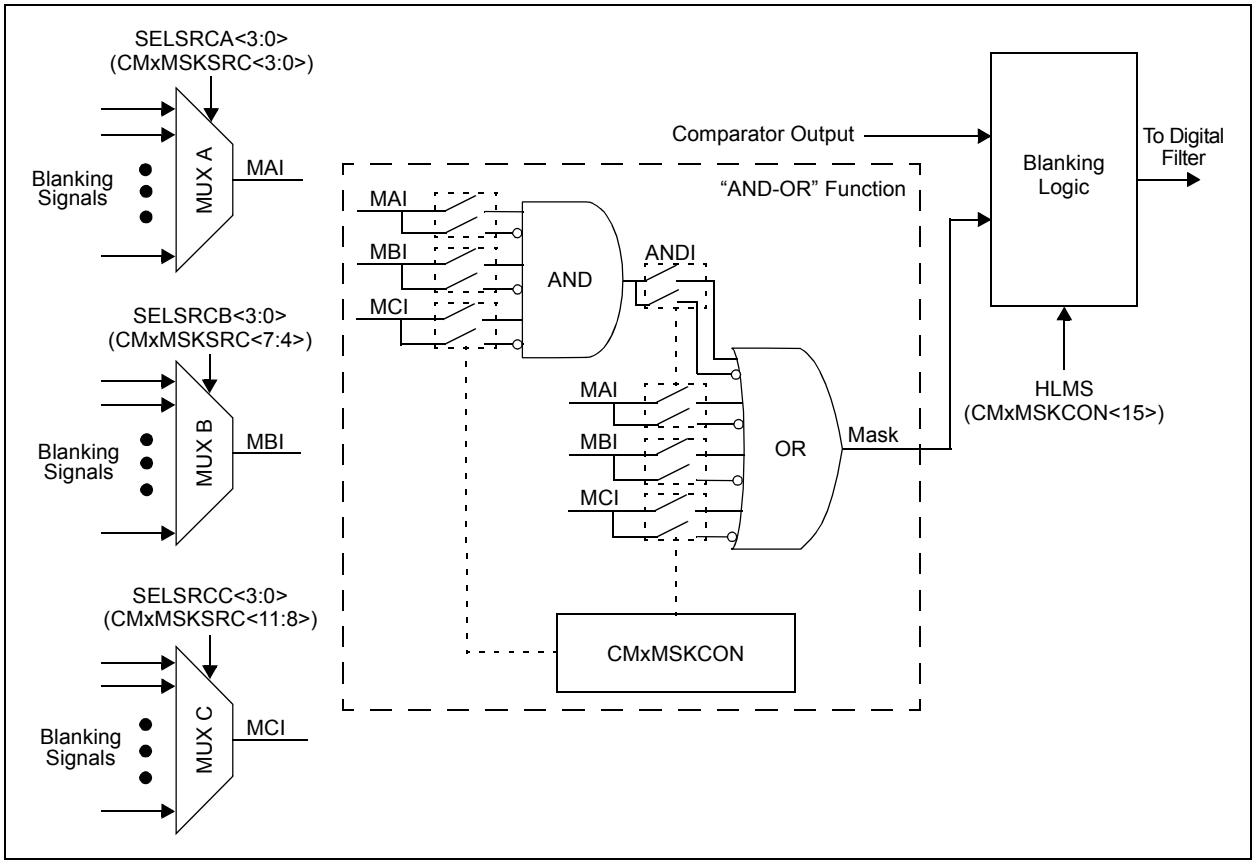
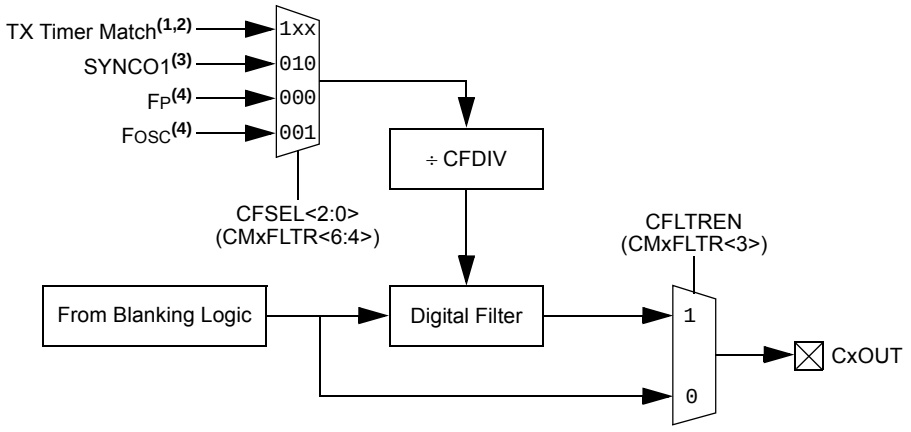


Figure 25-3, shows the digital filter interconnect block diagram.

FIGURE 25-3: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the PWMx Module Register Interconnect Diagram (Figure 17-2).
4: See the Oscillator System Diagram (Figure 9-1).

26.2 Comparator Voltage Reference Registers

REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF1O Pin) bit
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from the CVREF1O pin

bit 13-12 **Unimplemented:** Read as '0'

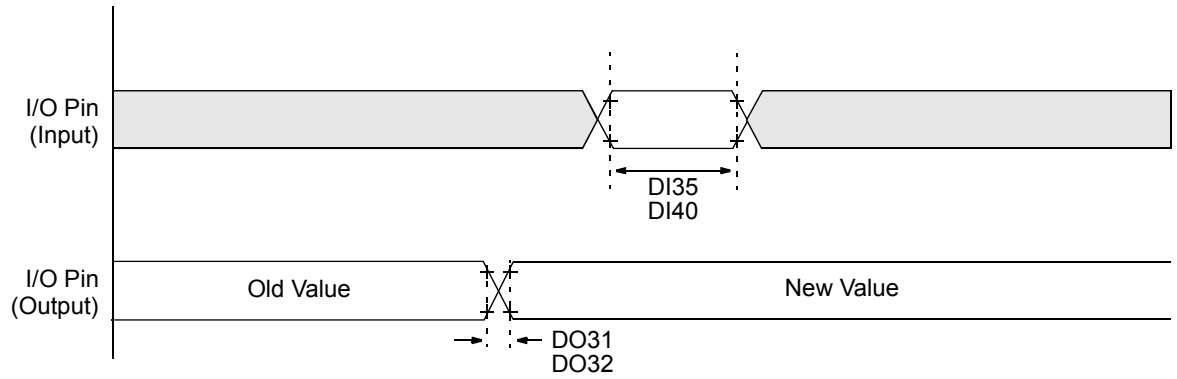
bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = CVREFIN = CVREF+
0 = CVREFIN is generated by the resistor network

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

FIGURE 30-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

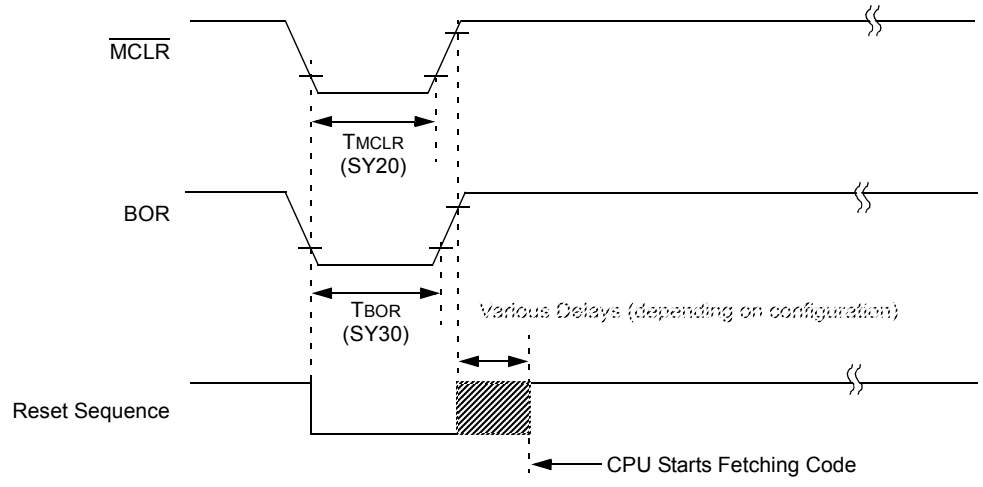
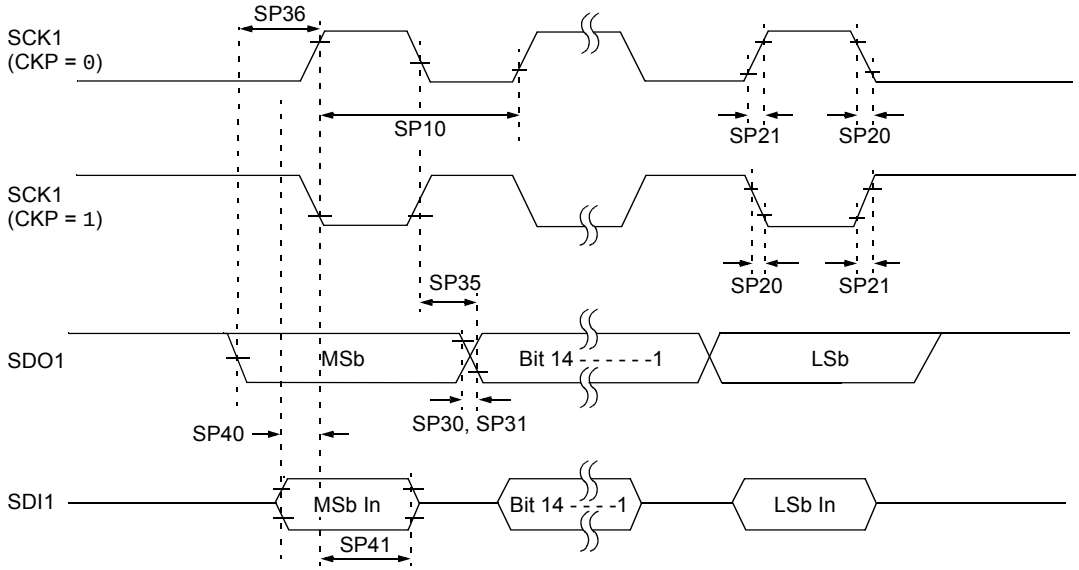


FIGURE 30-22: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-40: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 31-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU Current Source							
HCTMUI1	IOUT1	Base Range	—	550	—	nA	CTMUICON<9.8> = 01
HCTMUI2	IOUT2	10x Range	—	5.5	—	μA	CTMUICON<9.8> = 10
HCTMUI3	IOUT3	100x Range	—	55	—	μA	CTMUICON<9.8> = 11
HCTMUI0	IOUT4	1000x Range	—	550	—	μA	CTMUICON<9.8> = 00
HCTMUFV1	VF	Temperature Diode Forward Voltage(2)	—	0.525	—	V	TA = +25°C, CTMUICON<9.8> = 01
			—	0.585	—	V	TA = +25°C, CTMUICON<9.8> = 10
			—	0.645	—	V	TA = +25°C, CTMUICON<9.8> = 11

Note 1: Normal value at center point of current trim range (CTMUICON<15:10> = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements are taken with the following conditions:

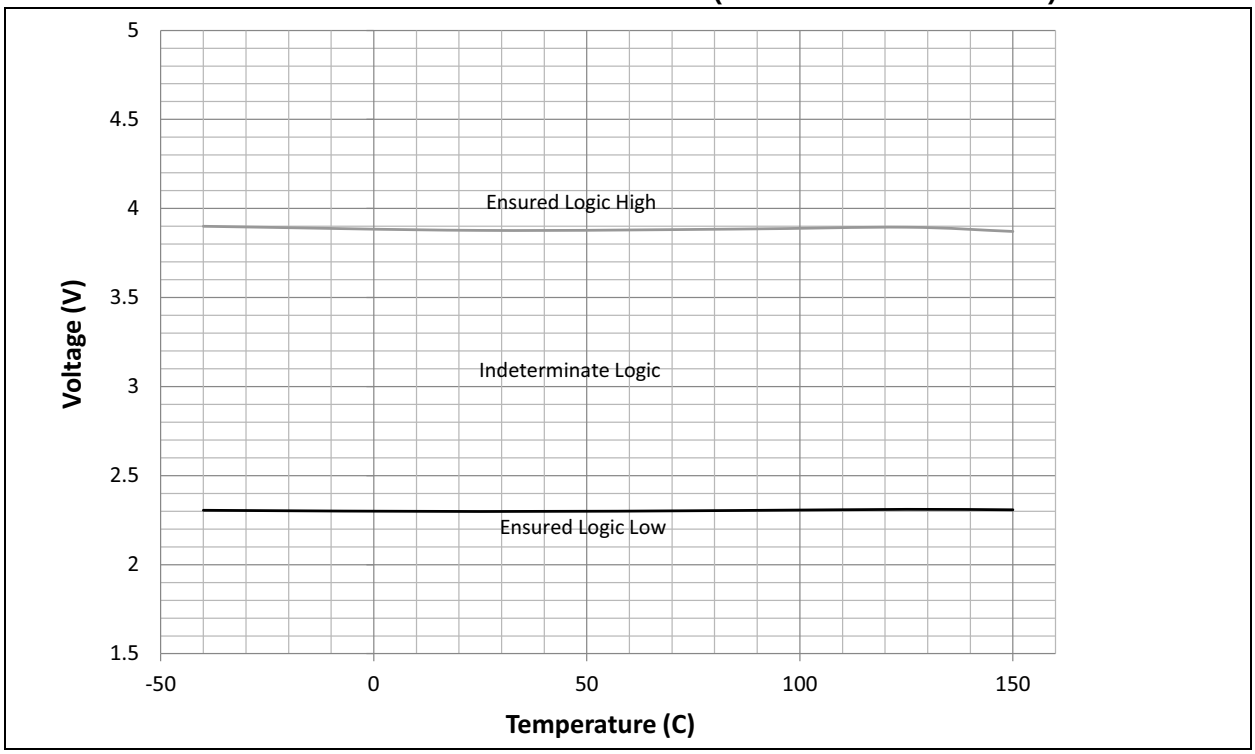
- VREF = AVDD = 5.0V
- ADC module configured for 10-bit mode
- ADC module configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- CPU executing

```
while(1)
{
NOP();
}
```

- Device operating from the FRC with no PLL

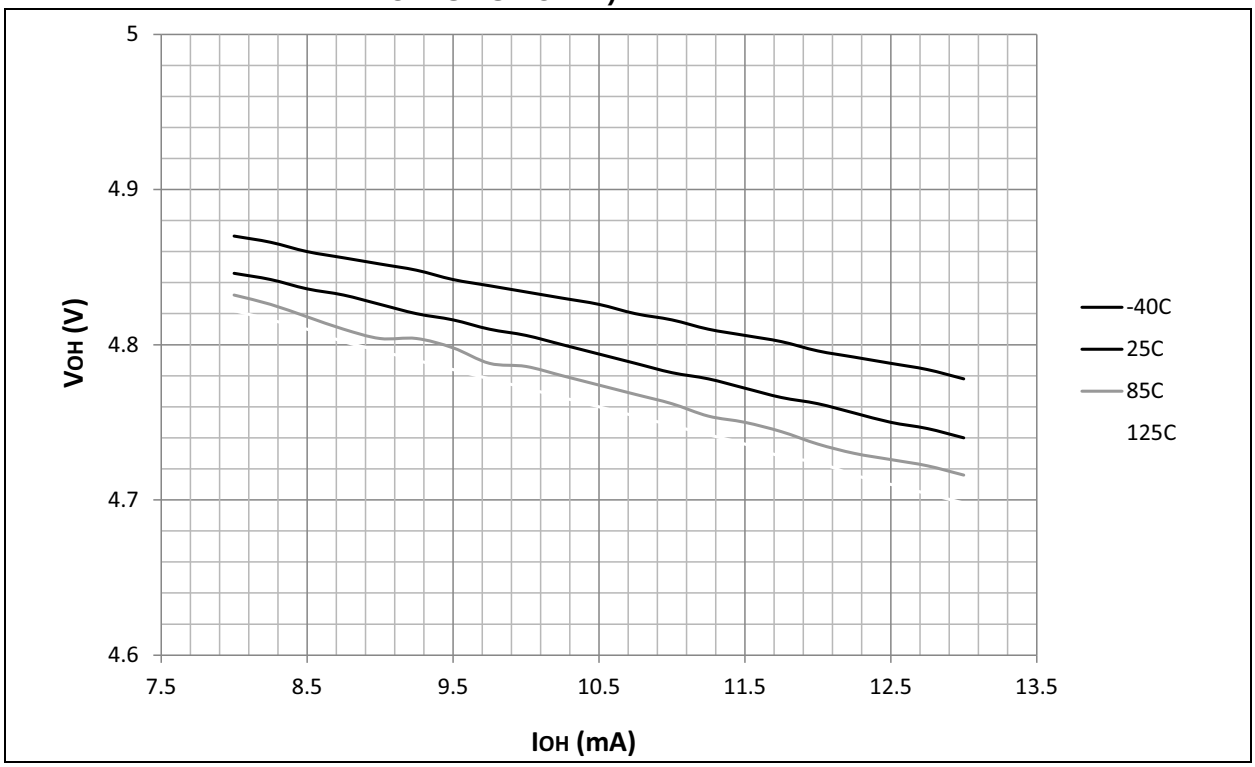
32.9 Voltage Input Low (VIL) – Voltage Input High (VIH)

FIGURE 32-29: TYPICAL VIH/VIL vs. TEMPERATURE (GENERAL PURPOSE I/Os)



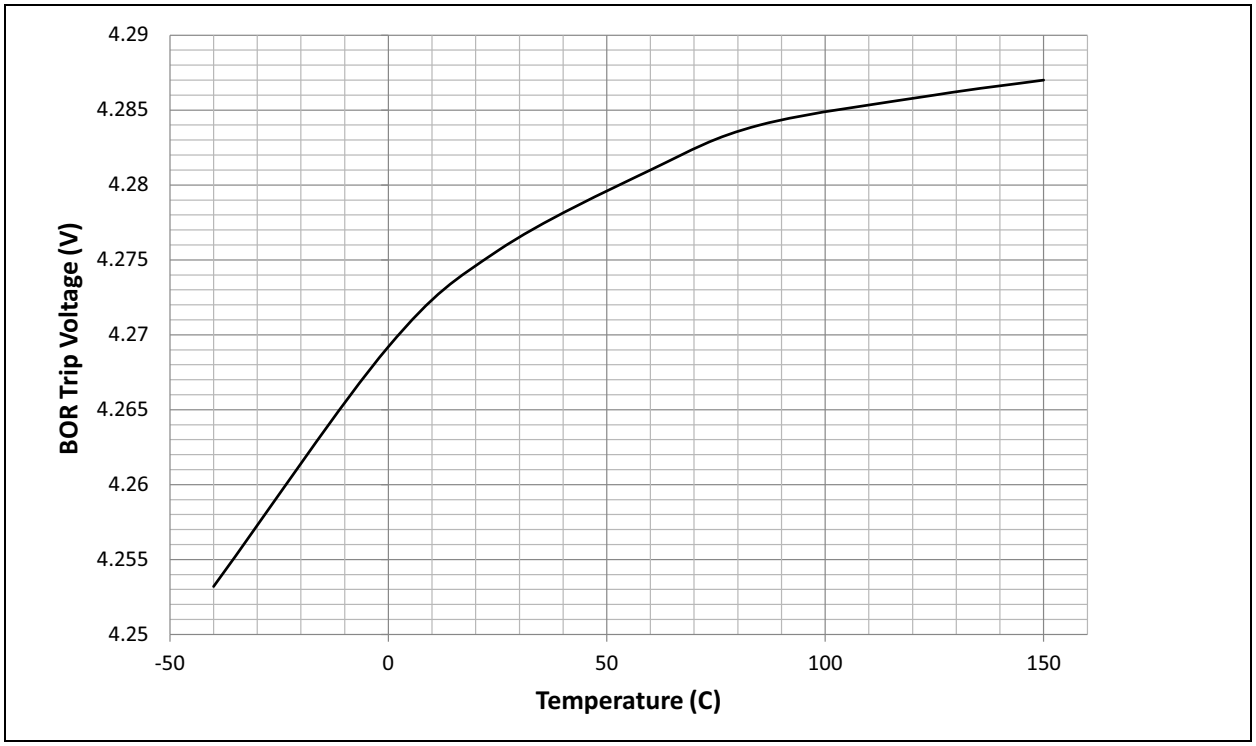
32.10 Voltage Output Low (VOL) – Voltage Output High (VOH)

FIGURE 32-30: TYPICAL VOH 8x DRIVER PINS vs. IOH (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



32.12 VBOR

FIGURE 32-35: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



32.13 RAM Retention

FIGURE 32-36: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE

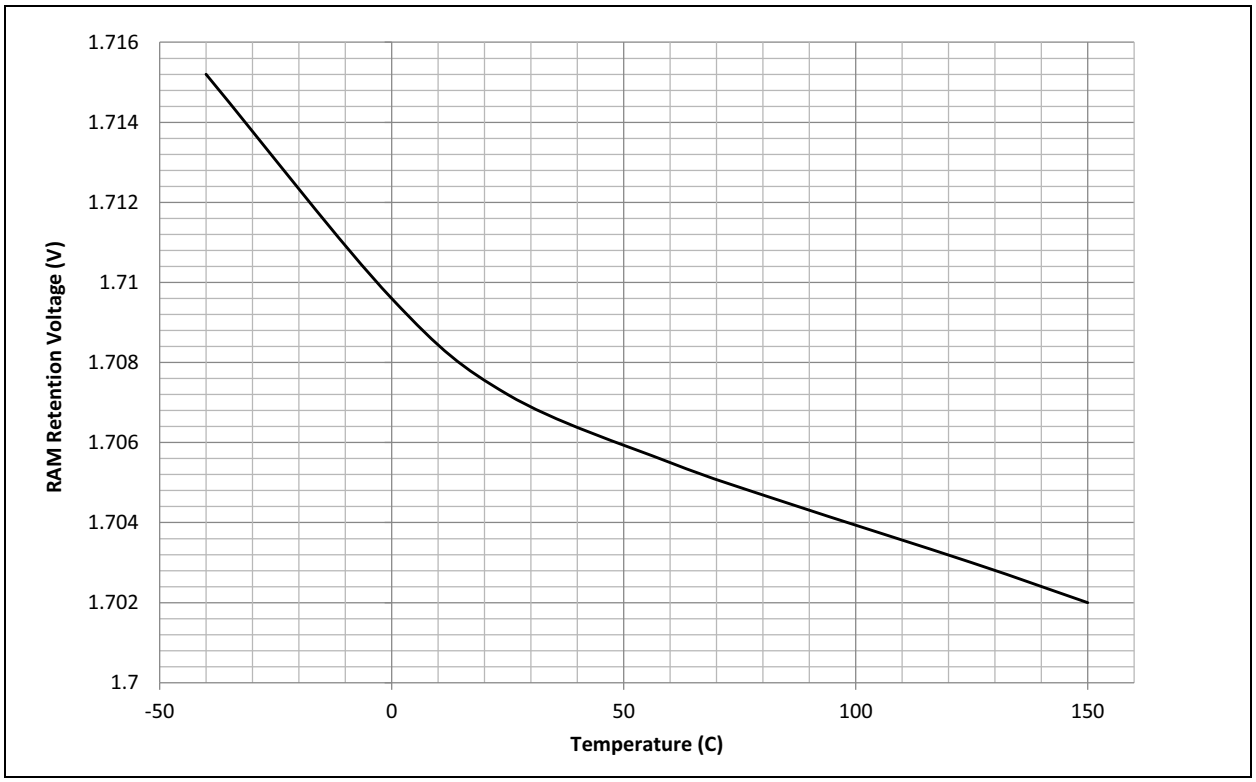


FIGURE 32-47: TYPICAL INL (V_{DD} = 5.5V, +85°C)

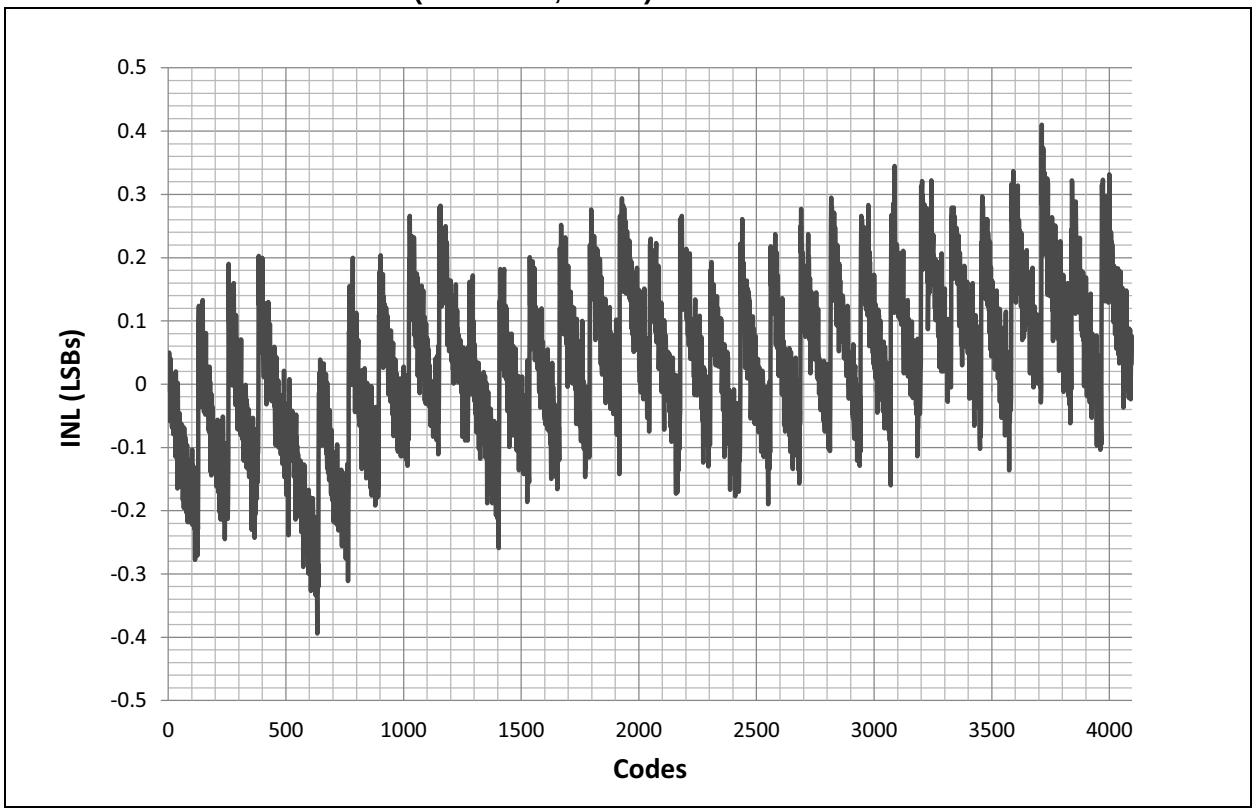
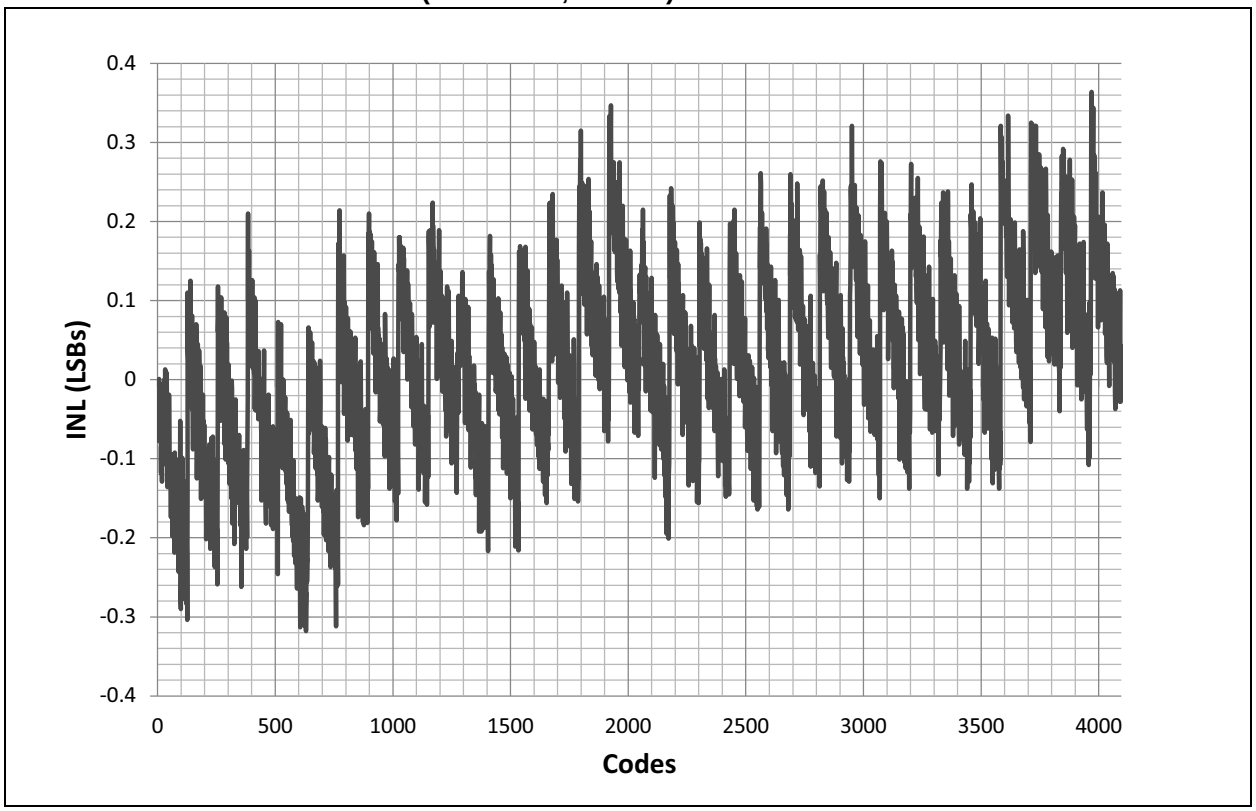


FIGURE 32-48: TYPICAL INL (V_{DD} = 5.5V, +125°C)



32.19 ADC Gain Offset Error

FIGURE 32-49: TYPICAL ADC GAIN ERROR vs. TEMPERATURE

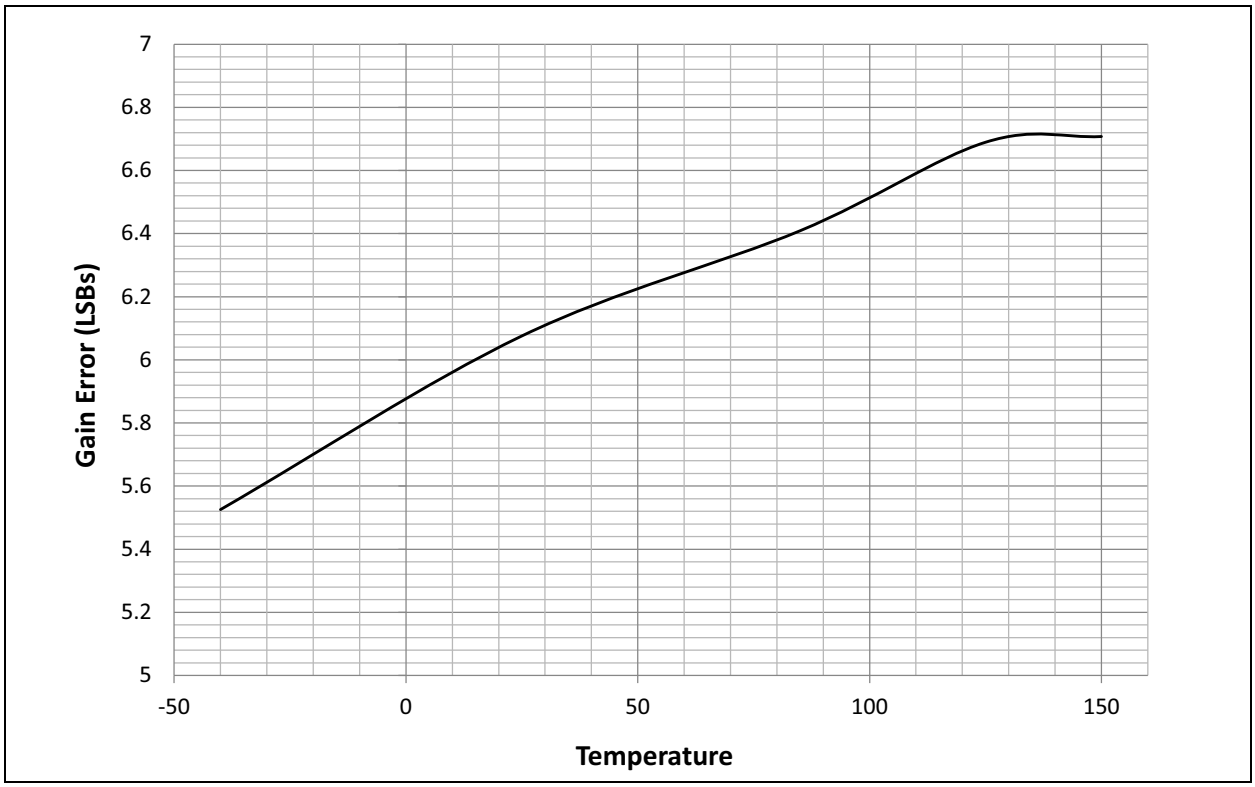
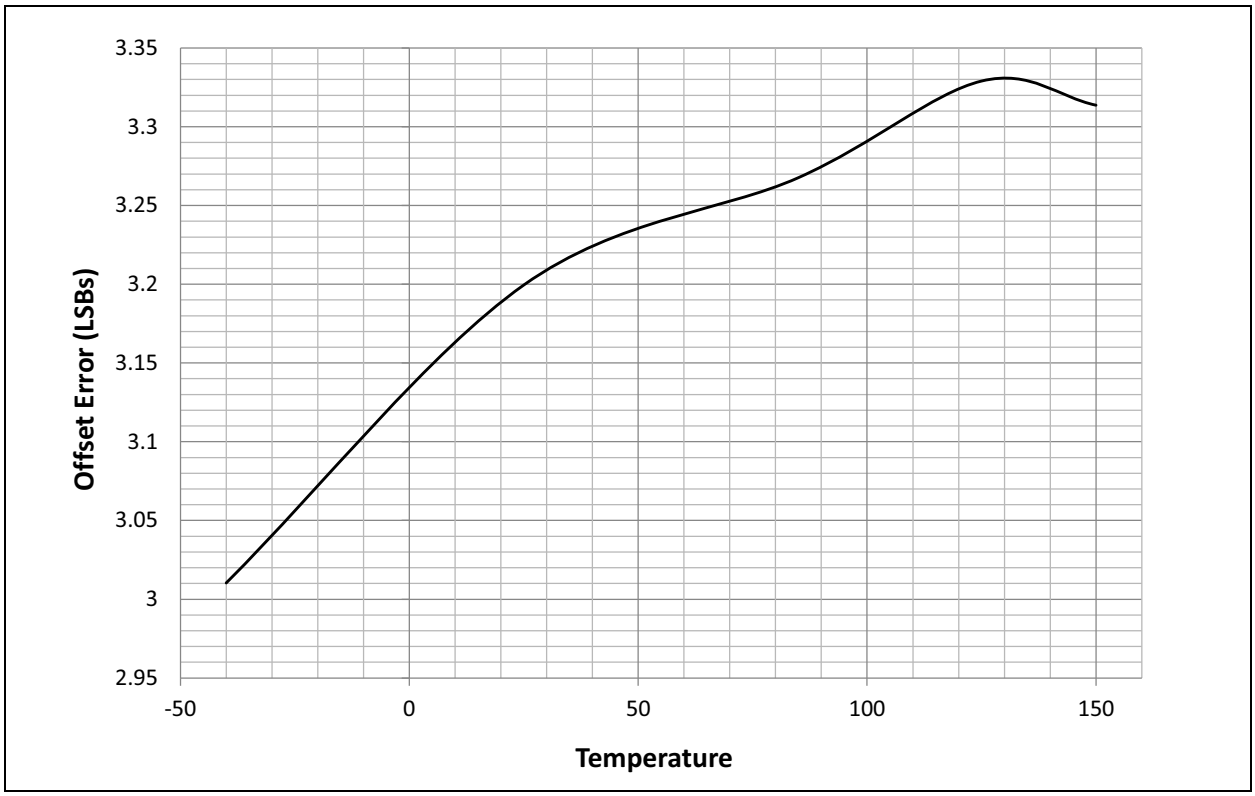


FIGURE 32-50: TYPICAL ADC OFFSET ERROR vs. TEMPERATURE



33.8 Pull-up/Pull-Down Current

FIGURE 33-23: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE

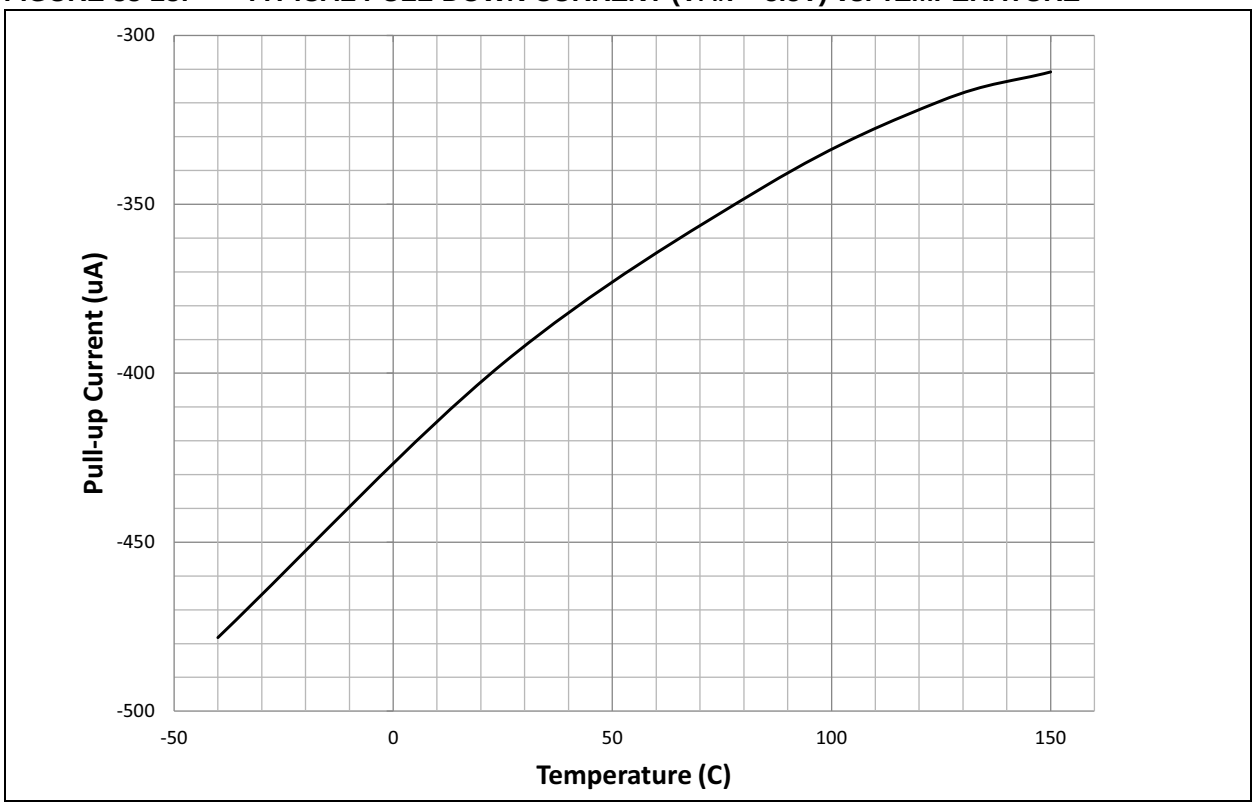


FIGURE 33-24: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE

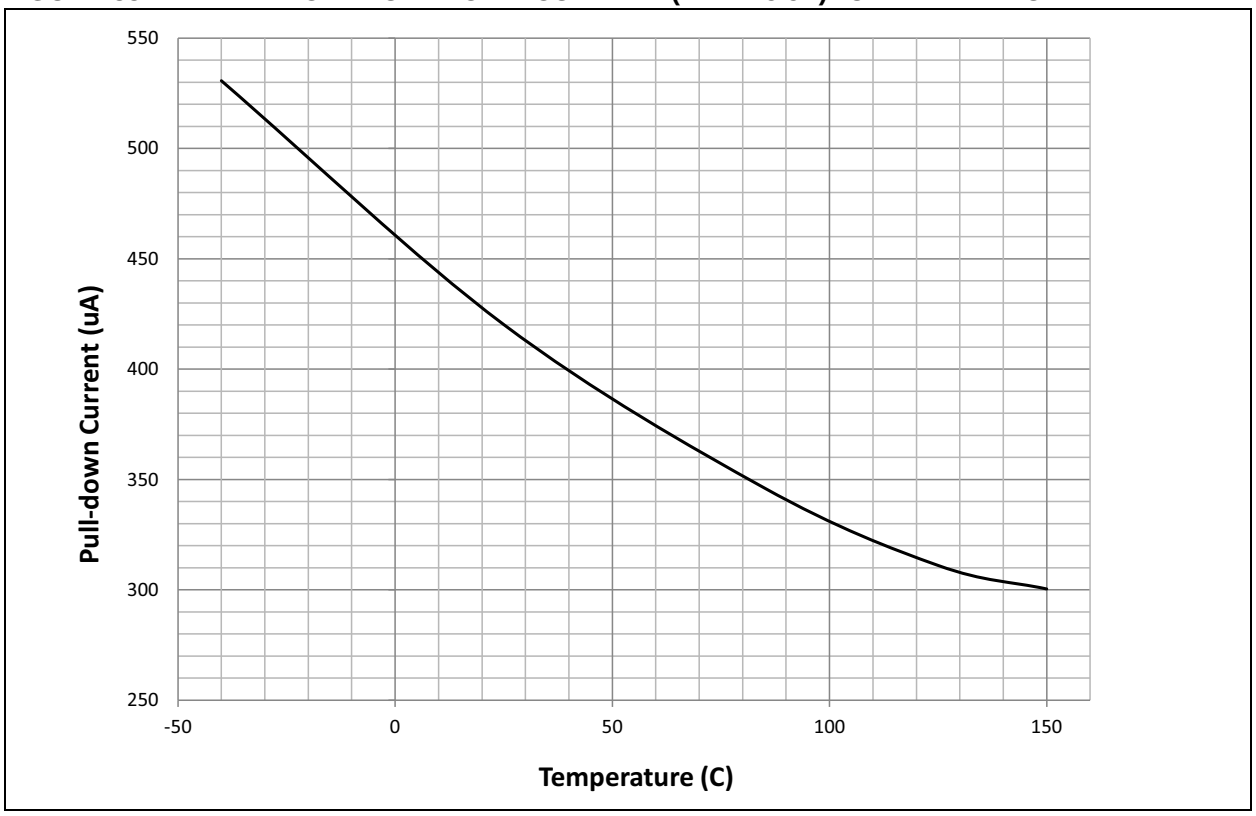
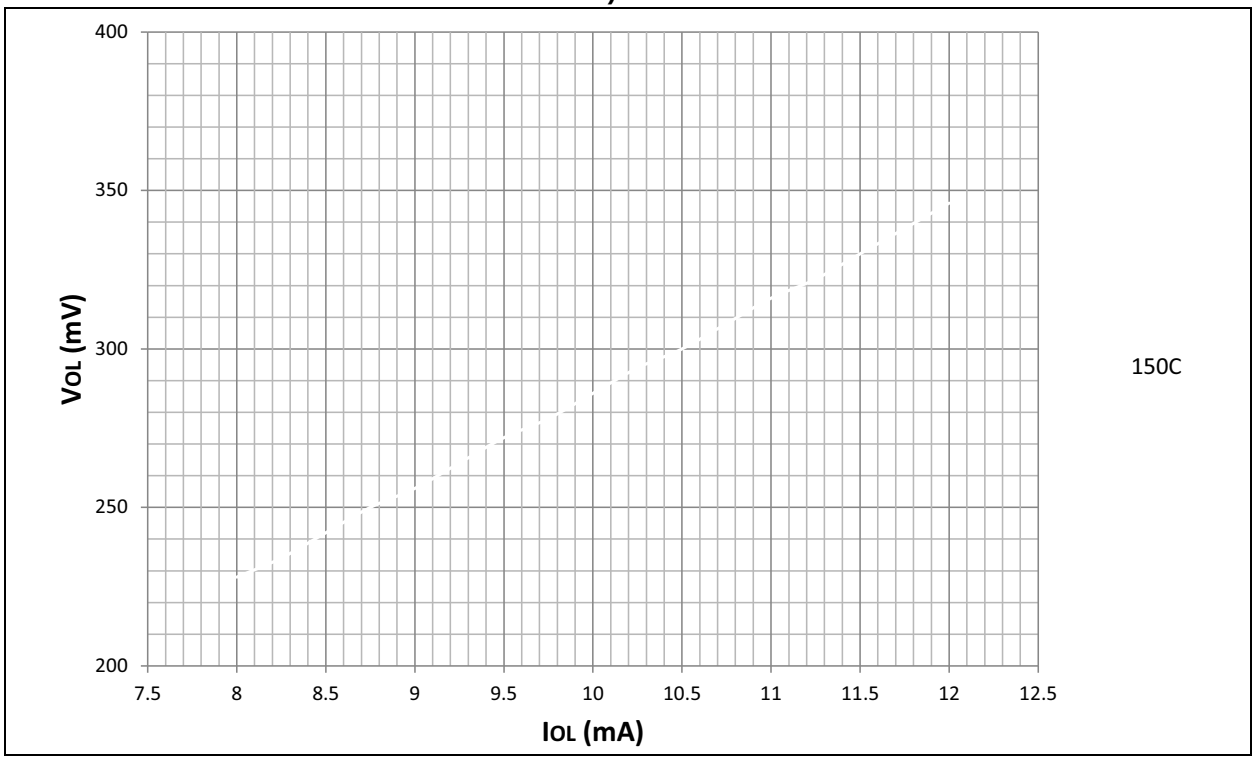


FIGURE 33-29: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



33.11 VREG

FIGURE 33-30: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE