**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
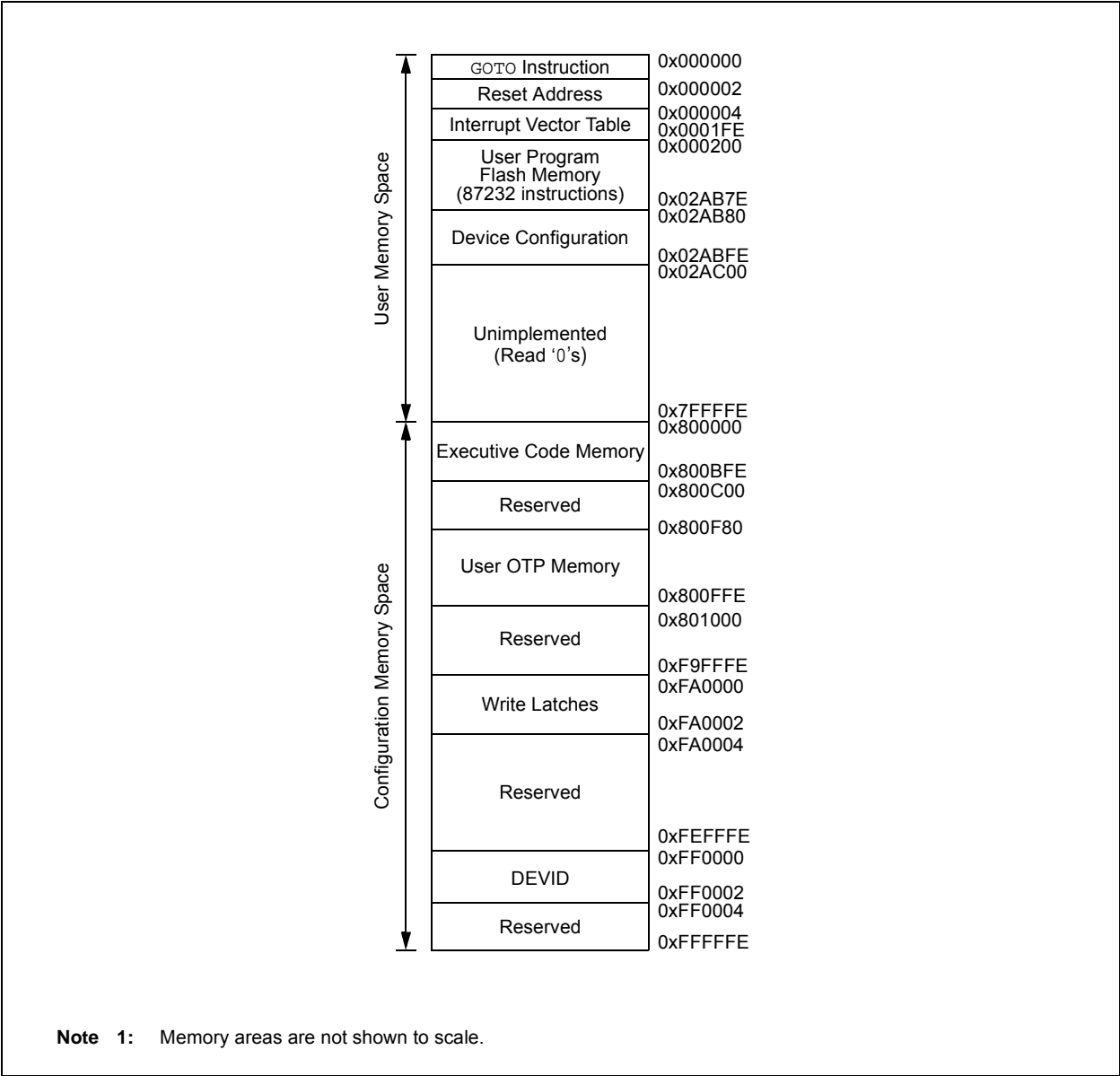
**Applications of "Embedded - Microcontrollers"**

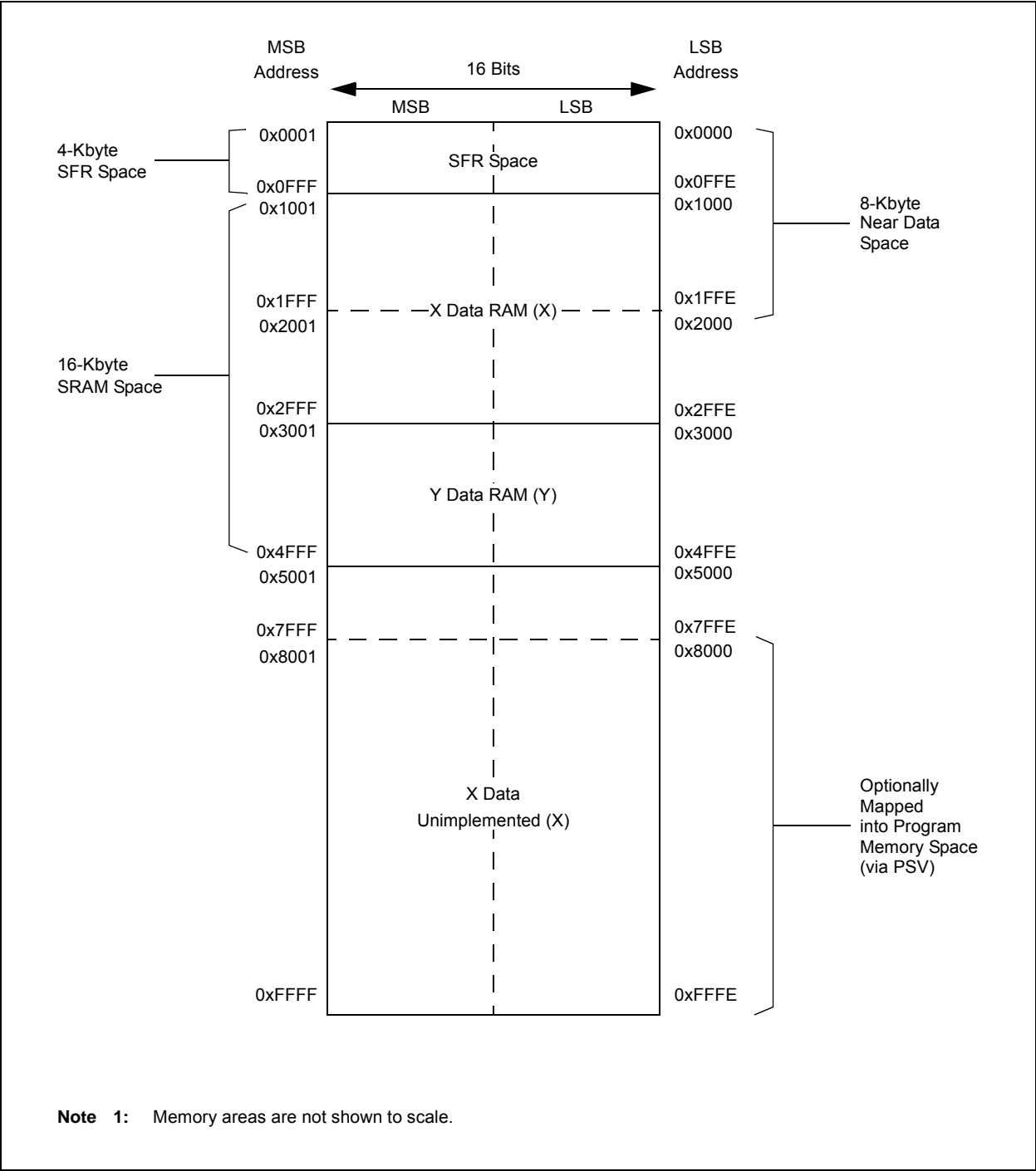| Details | |
| --- | --- |
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (11K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm004-e-pt |

**FIGURE 4-4:** **PROGRAM MEMORY MAP FOR dsPIC33EV256GM00X/10X DEVICES[1]**

| | Address |
|---|---|
| GOTO Instruction | 0x000000 |
| Reset Address | 0x000002 |
| Interrupt Vector Table | 0x000004 / 0x0001FE |
| User Program Flash Memory (87232 instructions) | 0x000200 / 0x02AB7E |
| Device Configuration | 0x02AB80 / 0x02ABFE |
| Unimplemented (Read '0's) | 0x02AC00 / 0x7FFFFE |
| Executive Code Memory | 0x800000 / 0x800BFE |
| Reserved | 0x800C00 / 0x800F80 |
| User OTP Memory | 0x800F80 / 0x800FFE |
| Reserved | 0x801000 / 0xF9FFFE |
| Write Latches | 0xFA0000 / 0xFA0002 |
| Reserved | 0xFA0004 / 0xFEFFFE |
| DEVID | 0xFF0000 / 0xFF0002 |
| Reserved | 0xFF0004 / 0xFFFFFE |

User Memory Space: 0x000000 – 0x7FFFFE
Configuration Memory Space: 0x800000 – 0xFFFFFE

**Note 1:** Memory areas are not shown to scale.

**FIGURE 4-8:     DATA MEMORY MAP FOR 256-Kbyte DEVICES(1)**



| | | |
|---|---|---|
| MSB Address | 16 Bits | LSB Address |
| | MSB        LSB | |

4-Kbyte SFR Space — 0x0001 ... 0x0FFF | SFR Space | 0x0000 ... 0x0FFE

8-Kbyte Near Data Space — 0x1000 ... 0x1FFE 0x2000

16-Kbyte SRAM Space — 0x1001 ... 0x1FFF 0x2001 | X Data RAM (X) |

0x2FFF 0x3001 | Y Data RAM (Y) | 0x2FFE 0x3000

0x4FFF 0x5001 | | 0x4FFE 0x5000

0x7FFF 0x8001 | | 0x7FFE 0x8000

| X Data Unimplemented (X) | Optionally Mapped into Program Memory Space (via PSV)

0xFFFF | | 0xFFFE

**Note   1:**   Memory areas are not shown to scale.

## 4.3.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x2FFF, is always accessible regardless of the contents of the Data Space Page registers; it is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x002FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of Base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, the DSRPAG and DSWPAG registers are initialized to 0x001 at Reset.

> **Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.
>
> **2:** Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where the base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF of the Data Space, will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-12.

For more information on the PSV page access using Data Space Page registers, refer to **Section 5.0 "Program Space Visibility from Data Space"** in **"dsPIC33E/PIC24E Program Memory"** (DS70000613) of the *"dsPIC33/PIC24 Family Reference Manual"*.

**FIGURE 4-12: EDS MEMORY MAP**
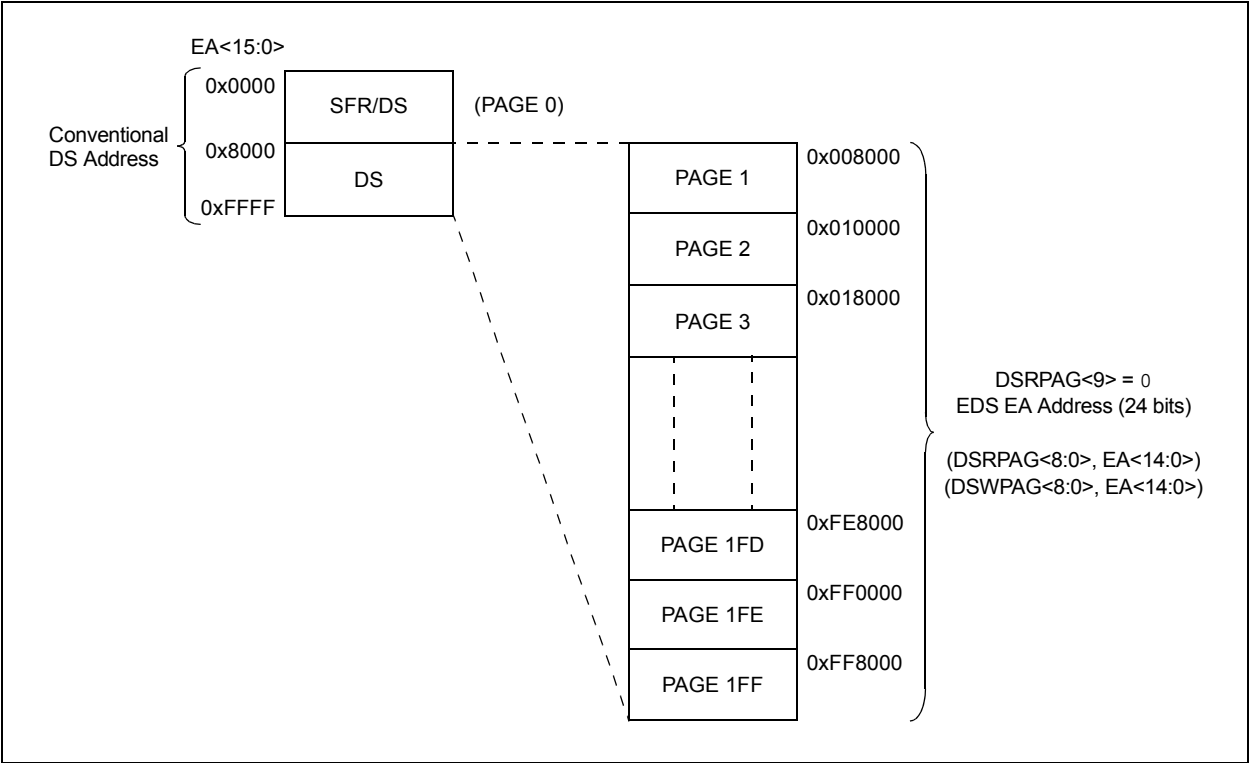
**REGISTER 6-1:** **RCON: RESET CONTROL REGISTER[1] (CONTINUED)**

bit 3     **SLEEP:** Wake-up from Sleep Flag bit

`1` = Device has been in Sleep mode
`0` = Device has not been in Sleep mode

bit 2     **IDLE:** Wake-up from Idle Flag bit

`1` = Device was in Idle mode
`0` = Device was not in Idle mode

bit 1     **BOR:** Brown-out Reset Flag bit

`1` = A Brown-out Reset has occurred
`0` = A Brown-out Reset has not occurred

bit 0     **POR:** Power-on Reset Flag bit

`1` = A Power-on Reset has occurred
`0` = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN<1:0> Configuration bits are '`11`' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 7-2:** **CORCON: CORE CONTROL REGISTER**[1]

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|-------|-----|-------|-------|-------|-----|-----|-----|
| VAR | — | US1 | US0 | EDT | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-----|-------|-------|
| SATA | SATB | SATDW | ACCSAT | IPL3[2] | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
 1 = Variable exception processing latency is enabled
 0 = Fixed exception processing latency is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3[2]
 1 = CPU Interrupt Priority Level is greater than 7
 0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** For complete register details, see Register 3-2.
 **2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

**REGISTER 10-1:** **PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)**

bit 2          **Unimplemented:** Read as '0'

bit 1          **C1MD:** CAN1 Module Disable bit[1]

      1 = CAN1 module is disabled
      0 = CAN1 module is enabled

bit 0          **AD1MD:** ADC1 Module Disable bit

      1 = ADC1 module is disabled
      0 = ADC1 module is enabled

**Note  1:**   This bit is available on dsPIC33EVXXXGM10X devices only.

**REGISTER 10-2:** **PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-----|-------|-------|-------|-------|
| — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-----|-------|-------|-------|-------|
| — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12      **Unimplemented:** Read as '0'

bit 11-8       **IC4MD:IC1MD:** Input Capture x (x = 1-4) Module Disable bits

      1 = Input Capture x module is disabled
      0 = Input Capture x module is enabled

bit 7-4        **Unimplemented:** Read as '0'

bit 3-0        **OC4MD:OC1MD:** Output Compare x (x = 1-4) Module Disable bits

      1 = Output Compare x module is disabled
      0 = Output Compare x module is enabled

**REGISTER 10-5:     PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-----|-----|-----|-------|-------|-------|
| — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11      **Unimplemented:** Read as '0'

bit 10-8       **PWM3MD:PWM1MD:** PWMx (x = 1-3) Module Disable bit

1 = PWMx module is disabled
0 = PWMx module is enabled

bit 7-0        **Unimplemented:** Read as '0'

**NOTES:**

**REGISTER 17-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|-------|-------|-------|-------|----------|---------|-----|-----|
| PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|----------|----------|-------|-------|-------|-------|
| — | — | BCH[1] | BCL[1] | BPHH | BPHL | BPLH | BPLL |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15　　**PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxH

bit 14　　**PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxH

bit 13　　**PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxL

bit 12　　**PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxL

bit 11　　**FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected Fault input
0 = Leading-Edge Blanking is not applied to the selected Fault input

bit 10　　**CLLEBEN:** Current-Limit Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected current-limit input
0 = Leading-Edge Blanking is not applied to the selected current-limit input

bit 9-6　　**Unimplemented:** Read as '0'

bit 5　　**BCH:** Blanking in Selected Blanking Signal High Enable bit[1]
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when the selected blanking signal is high

bit 4　　**BCL:** Blanking in Selected Blanking Signal Low Enable bit[1]
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when the selected blanking signal is low

bit 3　　**BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is high
0 = No blanking when the PWMxH output is high

bit 2　　**BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is low
0 = No blanking when the PWMxH output is low

bit 1　　**BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
0 = No blanking when the PWMxL output is high

bit 0　　**BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
0 = No blanking when the PWMxL output is low

**Note 1:** The blanking signal is selected through the BLANKSEL<3:0> bits in the AUXCONx register.

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, the SPIxTXB bit is full
0 = Transmit has started, the SPIxTXB bit is empty

Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in the hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, the SPIxRXB bit is full
0 = Receive is incomplete, the SPIxRXB bit is empty

Standard Buffer mode:
Automatically set in the hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

## REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE[1] |

bit 15                                                    bit 8

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEN[2] | CKP | MSTEN | SPRE2[3] | SPRE1[3] | SPRE0[3] | PPRE1[3] | PPRE0[3] |

bit 7                                                    bit 0

| Legend: | | |
|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared       x = Bit is unknown |

bit 15-13    **Unimplemented:** Read as '0'

bit 12    **DISSCK:** Disable SCKx Pin bit (SPI Master modes only)
        1 = Internal SPI clock is disabled, pin functions as I/O
        0 = Internal SPI clock is enabled

bit 11    **DISSDO:** Disable SDOx Pin bit
        1 = SDOx pin is not used by the module; pin functions as I/O
        0 = SDOx pin is controlled by the module

bit 10    **MODE16:** Word/Byte Communication Select bit
        1 = Communication is word-wide (16 bits)
        0 = Communication is byte-wide (8 bits)

bit 9    **SMP:** SPIx Data Input Sample Phase bit
        <u>Master mode:</u>
        1 = Input data is sampled at the end of data output time
        0 = Input data is sampled at the middle of data output time
        <u>Slave mode:</u>
        SMP must be cleared when SPIx is used in Slave mode.

bit 8    **CKE:** Clock Edge Select bit[1]
        1 = Serial output data changes on transition from active clock state to Idle clock state (refer to bit 6)
        0 = Serial output data changes on transition from Idle clock state to active clock state (refer to bit 6)

bit 7    **SSEN:** Slave Select Enable bit (Slave mode)[2]
        1 = $\overline{SSx}$ pin is used for Slave mode
        0 = $\overline{SSx}$ pin is not used by the module; pin is controlled by port function

bit 6    **CKP:** Clock Polarity Select bit
        1 = Idle state for clock is a high level; active state is a low level
        0 = Idle state for clock is a low level; active state is a high level

bit 5    **MSTEN:** Master Mode Enable bit
        1 = Master mode
        0 = Slave mode

**Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

    **2:** This bit must be cleared when FRMEN = 1.

    **3:** Do not set both primary and secondary prescalers to the value of 1:1.

                                         

**REGISTER 19-1:    I2CxCON1: I2Cx CONTROL REGISTER 1 (CONTINUED)**

bit 7          **GCEN:** General Call Enable bit (I$^2$C Slave mode only)

1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6          **STREN:** SCLx Clock Stretch Enable bit

In I$^2$C Slave mode only, used in conjunction with the SCLREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5          **ACKDT:** Acknowledge Data bit

In I$^2$C Master mode, during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I$^2$C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4          **ACKEN:** Acknowledge Sequence Enable bit

In I$^2$C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3          **RCEN:** Receive Enable bit (I$^2$C Master mode only)

1 = Enables Receive mode for I$^2$C, automatically cleared by hardware at the end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2          **PEN:** Stop Condition Enable bit (I$^2$C Master mode only)

1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1          **RSEN:** Restart Condition Enable bit (I$^2$C Master mode only)

1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0          **SEN:** Start Condition Enable bit (I$^2$C Master mode only)

1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

**Note 1:**   Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

**2:**   Automatically cleared to '0' at the beginning of slave transmission.

## 21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains two UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EVXXXGM00X/10X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

> **Note:** Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UART Error Conditions

**FIGURE 21-1: UARTx SIMPLIFIED BLOCK DIAGRAM**
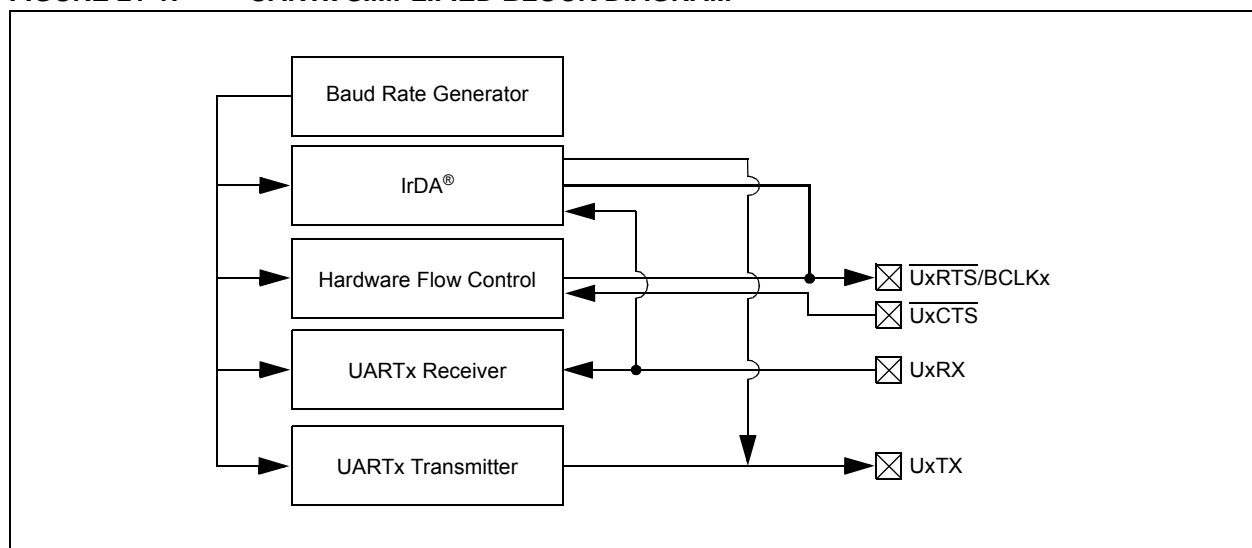
**REGISTER 22-4:** **CxFCTRL: CANx FIFO CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|-------|-------|-------|-----|-----|-----|-----|-----|
| DMABS2 | DMABS1 | DMABS0 | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-----|-----|-------|-------|-------|-------|-------|-------|
| — | — | FSA5 | FSA4 | FSA3 | FSA2 | FSA1 | FSA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13     **DMABS<2:0>:** DMA Buffer Size bits

       `111` = Reserved
       `110` = 32 buffers in RAM
       `101` = 24 buffers in RAM
       `100` = 16 buffers in RAM
       `011` = 12 buffers in RAM
       `010` = 8 buffers in RAM
       `001` = 6 buffers in RAM
       `000` = 4 buffers in RAM

bit 12-6     **Unimplemented:** Read as '0'

bit 5-0     **FSA<5:0>:** FIFO Area Starts with Buffer bits

       `11111` = Receive Buffer RB31
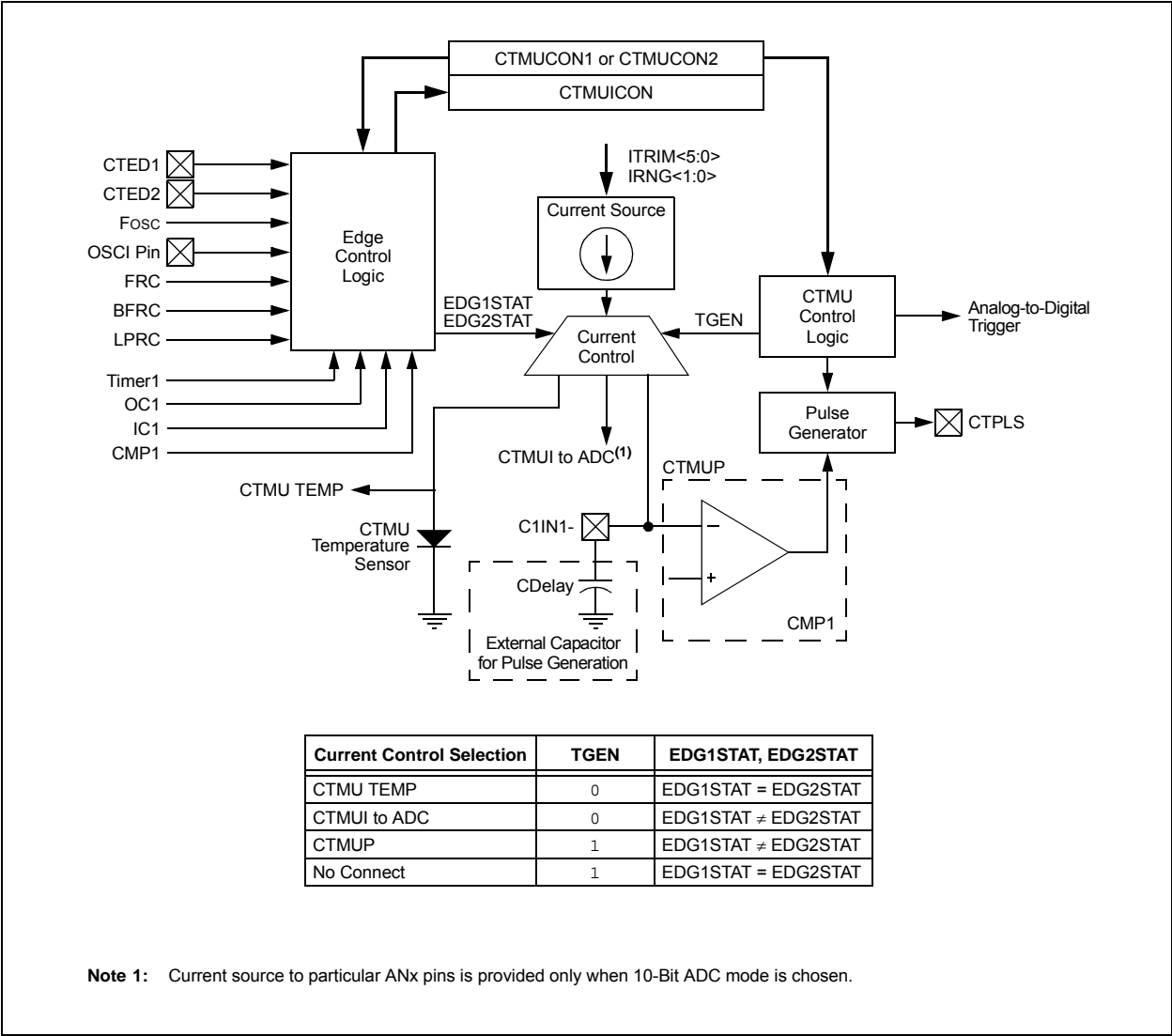       `11110` = Receive Buffer RB30
       •
       •
       •
       `00001` = TX/RX Buffer TRB1
       `00000` = TX/RX Buffer TRB0

**FIGURE 23-1:** **CTMU BLOCK DIAGRAM**



| Current Control Selection | TGEN | EDG1STAT, EDG2STAT |
|---|---|---|
| CTMU TEMP | 0 | EDG1STAT = EDG2STAT |
| CTMUI to ADC | 0 | EDG1STAT ≠ EDG2STAT |
| CTMUP | 1 | EDG1STAT ≠ EDG2STAT |
| No Connect | 1 | EDG1STAT = EDG2STAT |

**Note 1:** Current source to particular ANx pins is provided only when 10-Bit ADC mode is chosen.

**TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature    -40°C $\leq$ TA $\leq$ +85°C for Industrial    -40°C $\leq$ TA $\leq$ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param. | Symbol | Characteristic[1] | Min. | Typ.[2] | Max. | Units | Conditions |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 25 | MHz | See **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 20 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 20 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 15 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}\downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}\uparrow$ to SDO1 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}\uparrow$ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**TABLE 30-50: OP AMP/COMPARATOR x SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature   -40°C ≤ TA ≤ +85°C for Industrial                             -40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min. | Typ.(1) | Max. | Units | Conditions |
| **Comparator AC Characteristics** | | | | | | | |
| CM10 | TRESP | Response Time | — | 19 | 80 | ns | V+ input step of 100 mV, V- input held at VDD/2 |
| CM11 | TMC2OV | Comparator Mode Change to Output Valid | — | — | 10 | µs | |
| **Comparator DC Characteristics** | | | | | | | |
| CM30 | VOFFSET | Comparator Offset Voltage | -80 | ±60 | 80 | mV | |
| CM31 | VHYST | Input Hysteresis Voltage | — | 30 | — | mV | |
| CM32 | TRISE/ TFALL | Comparator Output Rise/Fall Time | — | 20 | — | ns | 1 pF load capacitance on input |
| CM33 | VGAIN | Open-Loop Voltage Gain | — | 90 | — | db | |
| CM34 | VICM | Input Common-Mode Voltage | AVSS | — | AVDD | V | |
| **Op Amp AC Characteristics** | | | | | | | |
| CM20 | SR | Slew Rate | — | 9 | — | V/µs | 10 pF load |
| CM21 | PM | Phase Margin | — | 35 | — | °C | G = 100V/V, 10 pF load |
| CM22 | GM | Gain Margin | — | 20 | — | db | G = 100V/V, 10 pF load |
| CM23 | GBW | Gain Bandwidth | — | 10 | — | MHz | 10 pF load |
| **Op Amp DC Characteristics** | | | | | | | |
| CM40 | VCMR | Common-Mode Input Voltage Range | AVSS | — | AVDD | V | |
| CM41 | CMRR | Common-Mode Rejection Ratio | — | 45 | — | db | VCM = AVDD/2 |
| CM42 | VOFFSET | Op Amp Offset Voltage | -50 | ±6 | 50 | mV | |
| CM43 | VGAIN | Open-Loop Voltage Gain | — | 90 | — | db | |
| CM44 | IOS | Input Offset Current | — | — | — | — | See pad leakage currents in Table 30-10 |
| CM45 | IB | Input Bias Current | — | — | — | — | See pad leakage currents in Table 30-10 |
| CM46 | IOUT | Output Current | — | — | 420 | µA | With minimum value of RFEEDBACK (CM48) |
| CM48 | RFEEDBACK | Feedback Resistance Value | 8 | — | — | kΩ | **Note 2** |
| CM49a | VOUT | Output Voltage | AVSS + 0.075 | — | AVDD – 0.075 | V | IOUT = 420 µA |

**Note 1:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**2:** Resistances can vary by ±10% between op amps.

**3:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

## 31.2 AC Characteristics and Timing Parameters

The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

### TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

| AC CHARACTERISTICS | **Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)**<br>Operating temperature   -40°C ≤ TA ≤ +150°C<br>Operating voltage VDD range as described in Table 31-1. |
|---|---|

### FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS
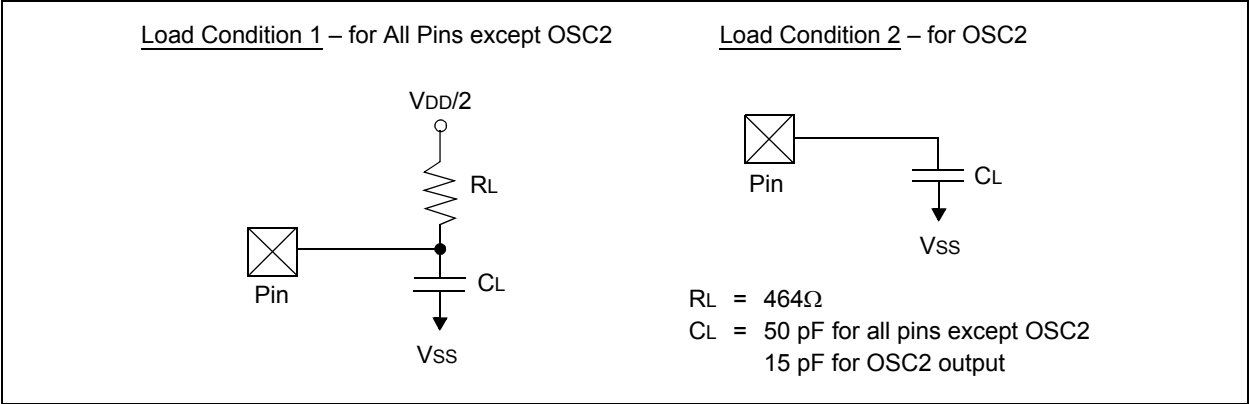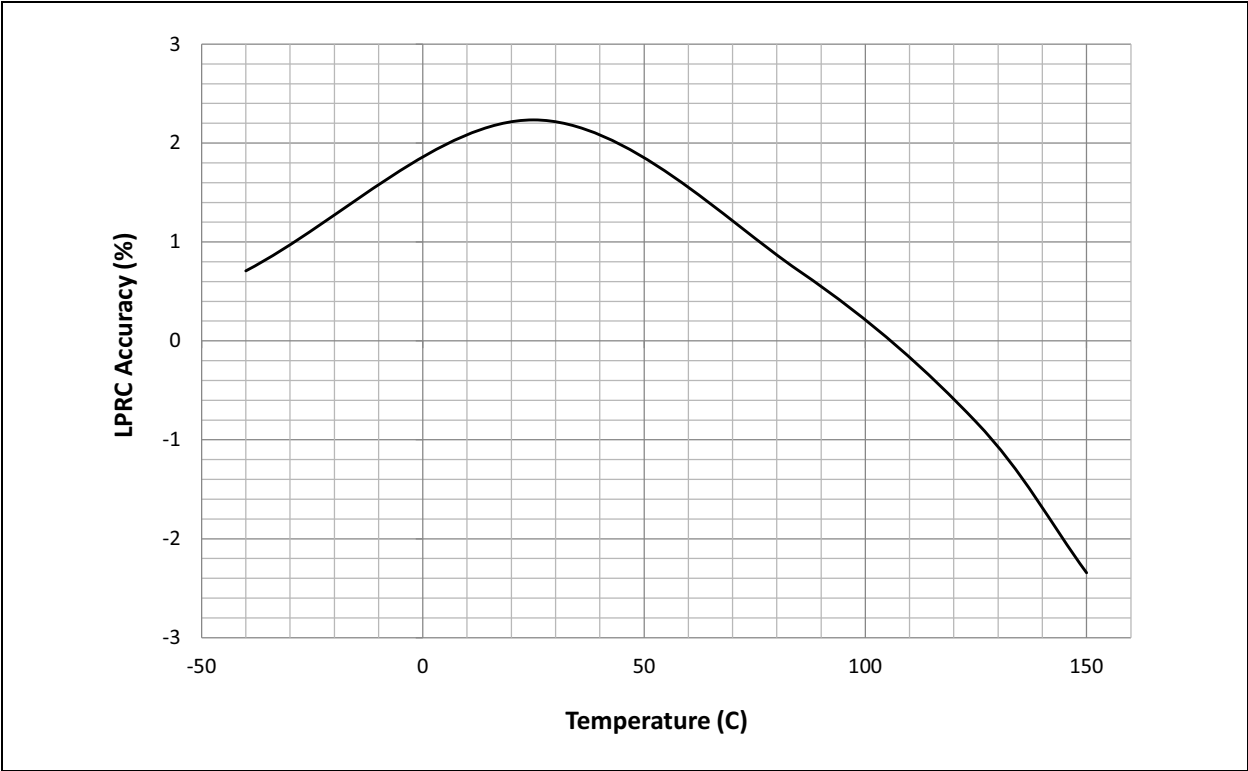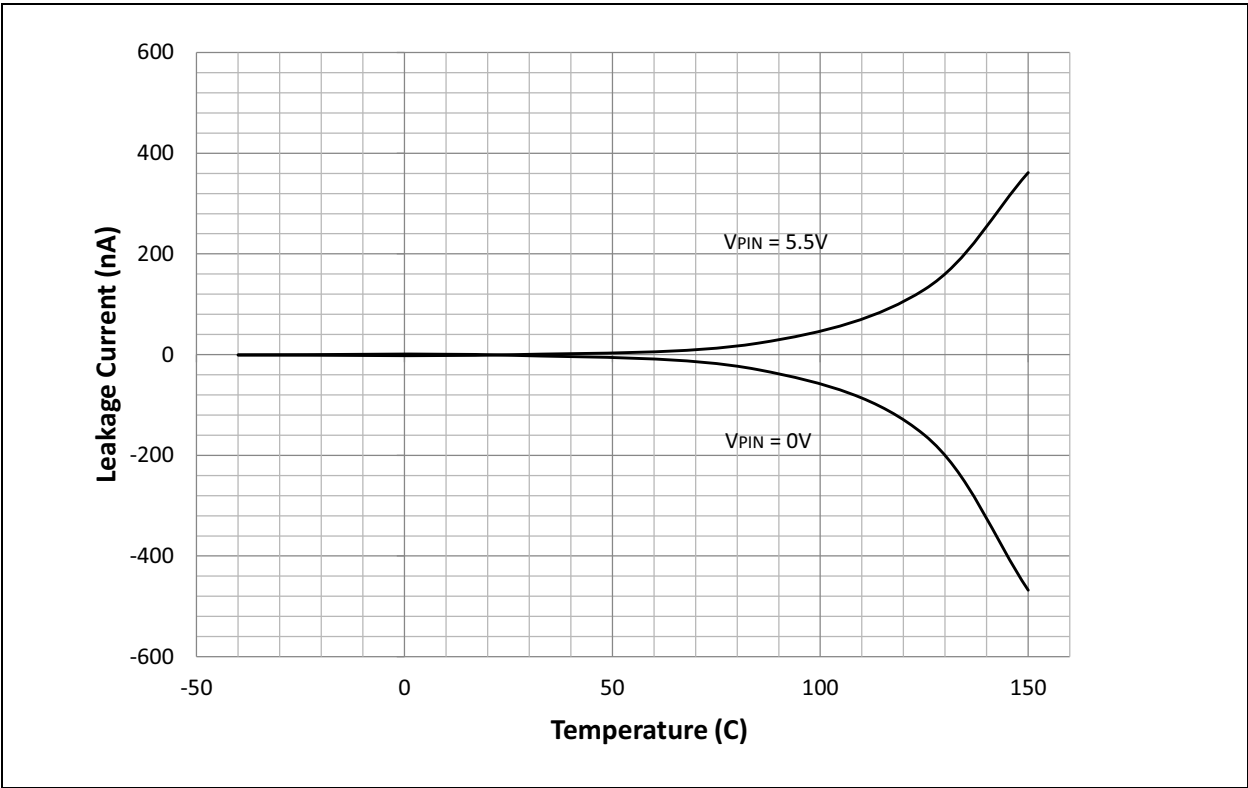
**FIGURE 32-23:** **TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V V$_{DD}$)**
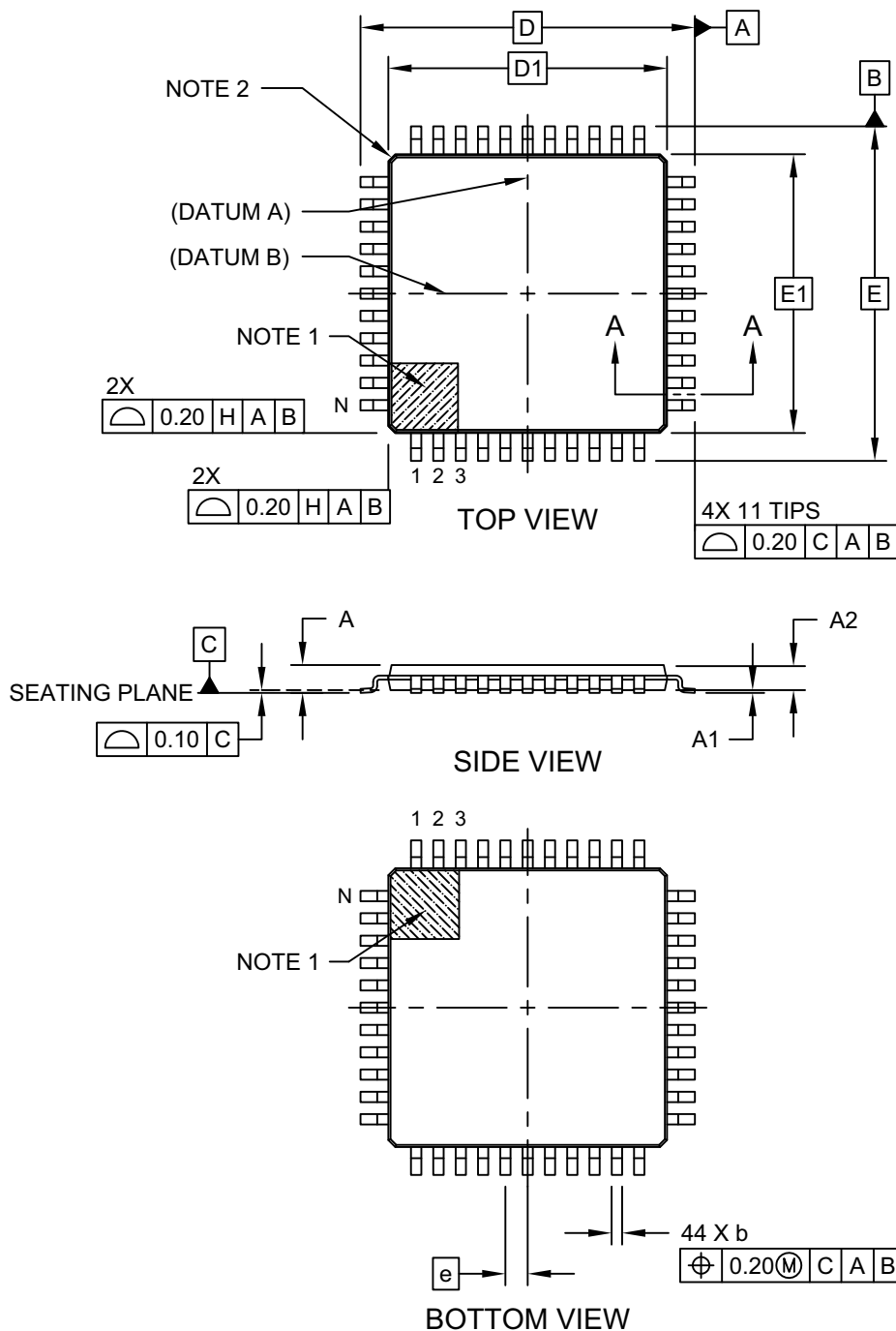


## 32.7    Leakage Current

**FIGURE 32-24:** **TYPICAL I$_{IL}$ vs. TEMPERATURE ($\overline{MCLR}$)**

## 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

NOTE 2

(DATUM A)

(DATUM B)

NOTE 1

2X
△ 0.20 H A B

2X
△ 0.20 H A B

N

1 2 3

TOP VIEW

4X 11 TIPS
△ 0.20 C A B

SEATING PLANE

C

△ 0.10 C

A

A2

A1

SIDE VIEW

1 2 3

N

NOTE 1

BOTTOM VIEW

44 X b
⊕ 0.20 Ⓜ C A B

e

Microchip Technology Drawing  C04-076C Sheet 1 of 2