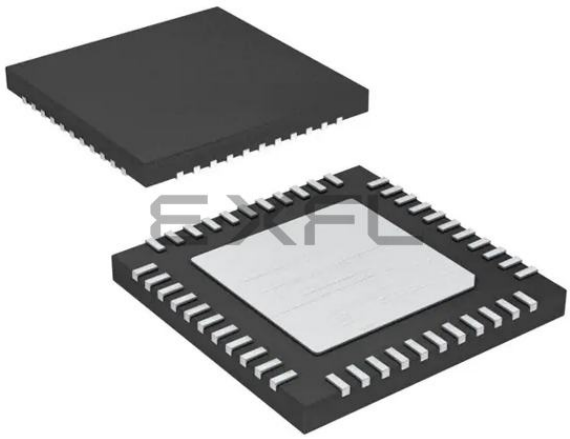
Microchip Technology - DSPIC33EV32GM004T-I/ML Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

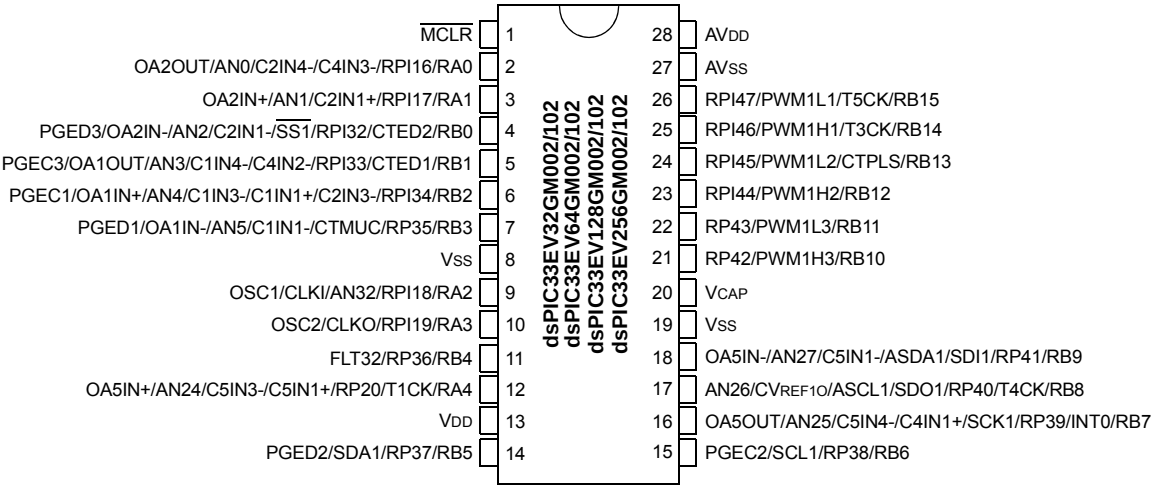
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm004t-i-ml

Pin Diagrams

28-Pin SPDIP/SOIC/SSOP(1,2,3)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

© 2013-2016 Microchip Technology Inc.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
C1RX	I	ST	Yes	CAN1 bus receive pin.
C1TX	O	—	Yes	CAN1 bus transmit pin.
SENT1TX	O	—	Yes	SENT1 transmit pin.
SENT1RX	I	—	Yes	SENT1 receive pin.
SENT2TX	O	—	Yes	SENT2 transmit pin.
SENT2RX	I	—	Yes	SENT2 receive pin.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs.
C1OUT	O	—	Yes	Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3-	I	Analog	No	Comparator 2 inputs.
C2OUT	O	—	Yes	Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3-	I	Analog	No	Comparator 3 inputs.
C3OUT	O	—	Yes	Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3-	I	Analog	No	Comparator 4 inputs.
C4OUT	O	—	Yes	Comparator 4 output.
C5IN1+, C5IN2-, C5IN1-, C5IN3-	I	Analog	No	Comparator 5 inputs.
C5OUT	O	—	Yes	Comparator 5 output.
FLT1-FLT2	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3-FLT8	I	ST	NO	PWM Fault Inputs 3 to 8.
FLT32	I	ST	NO	PWM Fault Input 32.
DTCMP1-DTCMP3	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 to 3.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 to 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 to 3.
SYNCI1	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1	O	—	Yes	PWM Synchronization Output 1.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

© 2013-2016 Microchip Technology Inc.

4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (see Figure 4-5).

Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during the code execution. This arrangement provides compatibility with the Data Memory Space Addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EVXXXGM00X/10X family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000 of Flash memory, with the actual address for the start of code at address, 0x000002 of Flash memory.

For more information on the Interrupt Vector Tables, see **Section 7.1 “Interrupt Vector Table”**.

FIGURE 4-5: PROGRAM MEMORY ORGANIZATION

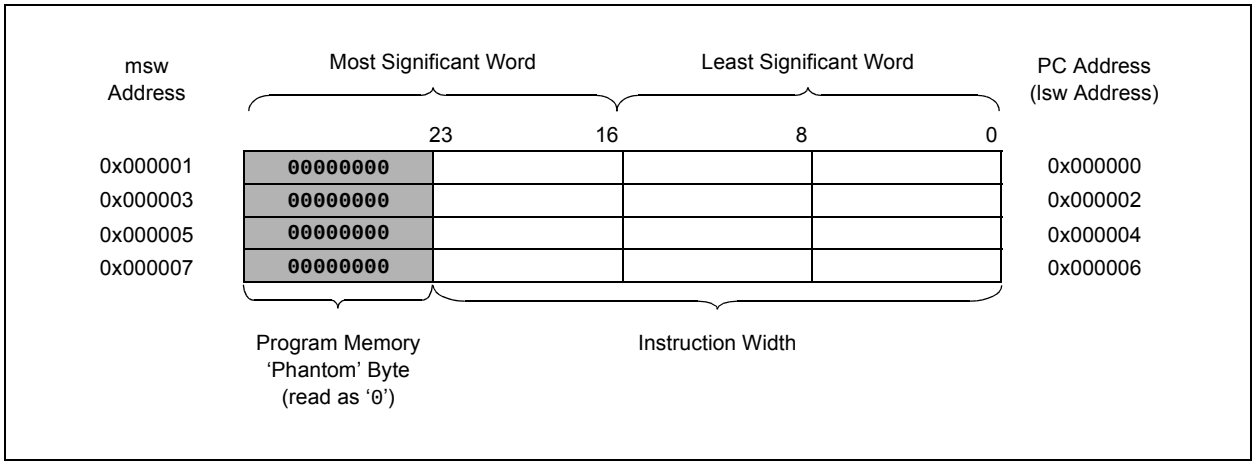


TABLE 4-41: PORTF REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E64	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF<1:0>		0003
PORTF	0E66	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF<1:0>		xxxx
LATF	0E68	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF<1:0>		xxxx
ODCF	0E6A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF<1:0>		0000
CNENF	0E6C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF<1:0>		0000
CNPUF	0E6E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF<1:0>		0000
CNPDF	0E70	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: PORTG REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E78	—	—	—	—	—	—	TRISG<9:6>				—	—	—	—	—	—	03C0
PORTG	0E7A	—	—	—	—	—	—	RG<9:6>				—	—	—	—	—	—	xxxx
LATG	0E7C	—	—	—	—	—	—	LATG<9:6>				—	—	—	—	—	—	xxxx
ODCG	0E7E	—	—	—	—	—	—	ODCG<9:6>				—	—	—	—	—	—	0000
CNENG	0E80	—	—	—	—	—	—	CNIEG<9:6>				—	—	—	—	—	—	0000
CNPUG	0E82	—	—	—	—	—	—	CNPUG<9:6>				—	—	—	—	—	—	0000
CNPDG	0E84	—	—	—	—	—	—	CNPDG<9:6>				—	—	—	—	—	—	0000
ANSELG	0E86	—	—	—	—	—	—	ANSG<9:6>				—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

© 2013-2016 Microchip Technology Inc.

4.7 Interfacing Program and Data Memory Spaces

The dsPIC33EVXXXGM00X/10X family architecture uses a 24-bit wide Program Space and a 16-bit wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both the spaces.

Aside from normal execution, the architecture of the dsPIC33EVXXXGM00X/10X family devices provides two methods by which Program Space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

Table 4-47 shows the construction of the Program Space address.

How the data is accessed from Program Space is shown in Figure 4-17.

TABLE 4-47: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCFAR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **OCFAR<7:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 14-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0, HC	R-0, HC	R-0, HC	U-0	U-0	U-0	U-0	R-0
BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Deadman Timer Bad STEP1<7:0> Value Detect bit
1 = Incorrect STEP1<7:0> value was detected
0 = Incorrect STEP1<7:0> value was not detected

bit 6 **BAD2:** Deadman Timer Bad STEP2<7:0> Value Detect bit
1 = Incorrect STEP2<7:0> value was detected
0 = Incorrect STEP2<7:0> value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman Timer event was detected (counter expired, or bad STEP1<7:0> or STEP2<7:0> value was entered prior to counter increment)
0 = Deadman Timer event was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman Timer clear window is open
0 = Deadman Timer clear window is not open

© 2013-2016 Microchip Technology Inc.

REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When Set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When Set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWMx time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
3: DTC<1:0> = 11 for DTCP to be effective; else, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 17-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx<15:0>:** PWMx Generator Duty Cycle Value bits

REGISTER 17-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation: Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL.

© 2013-2016 Microchip Technology Inc.

REGISTER 17-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LEB<11:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LEB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

© 2013-2016 Microchip Technology Inc.

REGISTER 22-16: CxRXFnSID: CANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 22-17: CxRXFnEID: CANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

© 2013-2016 Microchip Technology Inc.

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
78	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
79	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
80	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
81	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
82	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
83	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
84	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
85	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

© 2013-2016 Microchip Technology Inc.

29.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers (MCU) and dsPIC® digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
  - MPLAB® X IDE Software
- Compilers/Assemblers/Linkers
  - MPLAB XC Compiler
  - MPASM™ Assembler
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
  - MPLAB X SIM Software Simulator
- Emulators
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
  - MPLAB ICD 3
  - PICkit™ 3
- Device Programmers
  - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows®, Linux and Mac OS® X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- Call graph window

Project-Based Workspaces:

- Multiple projects
- Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- Built-in support for Bugzilla issue tracker

TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
OS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{FOSC}{\text{Time Base or Communication Clock}}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)							
F20a	FRC	-1	0.5	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
F20b	FRC	-2	1	+2	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V

Note 1: Frequency calibrated at +25°C and 5.0V. TUN<5:0> bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

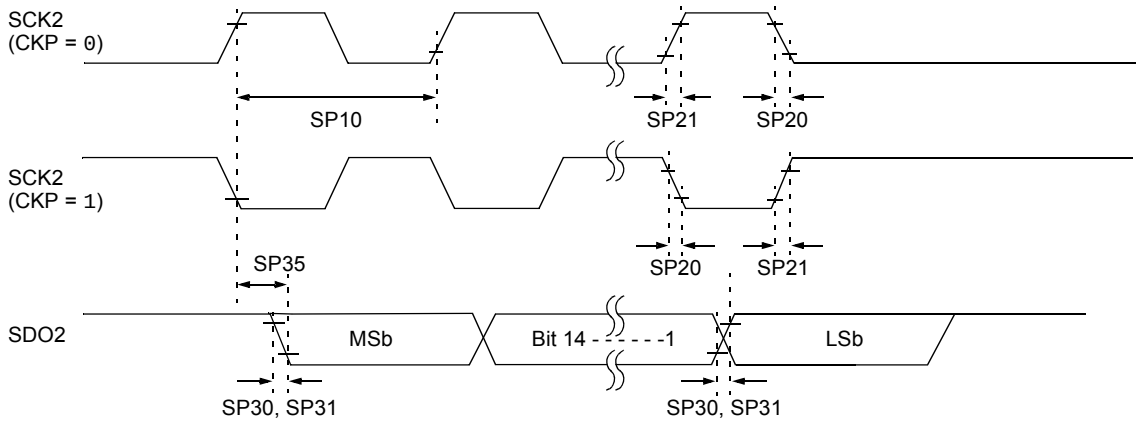
AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
LPRC @ 32.768 kHz(1)							
F21a	LPRC	-15	5	+15	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
F21b	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V

Note 1: Change of LPRC frequency as VDD changes.

TABLE 30-30: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 30-31	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-32	—	1	0,1	1
9 MHz	—	Table 30-33	—	0	0,1	1
15 MHz	—	—	Table 30-34	1	0	0
11 MHz	—	—	Table 30-35	1	1	0
15 MHz	—	—	Table 30-36	0	1	0
11 MHz	—	—	Table 30-37	0	0	0

FIGURE 30-12: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

© 2013-2016 Microchip Technology Inc.

SENTx Module 238
Shared I/O Port Structure 143
SPIx Module 222
Type B Timer (Timer2 and Timer4) 176
Type B/Type C Timer Pair (32-Bit Timer) 177
Type C Timer (Timer3 and Timer5) 176
UARTx Module 247
User-Programmable Blanking Function 302
Watchdog Timer (WDT) 325
Brown-out Reset (BOR) 324

C

C Compilers
MPLAB XC 338
CAN
CAN Module
Control Registers 255
Message Buffers 275
Word 0 275
Word 1 275
Word 2 276
Word 3 276
Word 4 277
Word 5 277
Word 6 278
Word 7 278
Modes of Operation 254
Overview 253
Characteristics for High-Temperature
Devices (+150°C) 439
Characteristics for Industrial/Extended Temperature
Devices (-40°C to +125°C) 413
Charge Time Measurement Unit (CTMU) 279
Charge Time Measurement Unit. *See* CTMU.
Code Examples
Port Write/Read 144
PORTA Slew Selections 145
PWM1 Write-Protected Register
Unlock Sequence 200
PWRSAV Instruction Syntax 133
Code Protection 317, 326
CodeGuard Security 317, 326
Comparator Voltage Reference
Configuring 313
Control Registers 315
Configuration Bits 317
Description 320
Controller Area Network (CAN) 253
Controller Area Network. *See* CAN.
CPU 21
Addressing Modes 21
Arithmetic Logic Unit (ALU) 30
Control Registers 25
Data Space Addressing 21
DSP Engine 30
Instruction Set 21
Programmer's Model 23
CTMU
Control Registers 281
Customer Change Notification Service 493
Customer Notification Service 493
Customer Support 493

D

Data Address Space 36
Alignment 36
Memory Map for 256-Kbyte Devices 39
Memory Map for 32-Kbyte Devices 37
Memory Map for 64/128-Kbyte Devices 38
Near Data Space 36
SFR Space 36
Width 36
Data Space
Extended X 72
Memory Arbitration, Bus Master Priority 73
Paged Memory Scheme 68
DC Characteristics 342
Brown-out Reset (BOR) 349
CTMU Current Source 394
Doze Current (IDOZE) 347
Filter Capacitor (CEFC) Specifications 343
High Temperature 404
Brown-out Reset (BOR) 407
CTMU Current Source 410
I/O Pin Input Specifications 406
I/O Pin Output Specifications 407
Idle Current (IIDLE) 405
Op Amp/ Comparator x 411
Operating Current (IDD) 405
Operating MIPS vs. Voltage 404
Power-Down Current (IPD) 405
Program Memory 407
Temperature and Voltage Specifications 404
Doze Current (IDOZE) 405
I/O Pin Input Specifications 348
I/O Pin Output Specifications 349
Idle Current (IIDLE) 345
Internal Band Gap Reference Voltage 350
Op Amp/Comparator x Specifications 392
Op Amp/Comparator x Voltage Reference
Specifications 393
Operating Current (IDD) 344
Operating MIPS vs. Voltage 342
Power-Down Current (IPD) 346
Program Memory 350
Temperature and Voltage Specifications 343
Thermal Operating Conditions 342
Deadman Timer (DMT) 181
Control Registers 182
Deadman Timer. *See* DMT.
Development Support 337
Direct Memory Access. *See* DMA.
DMA Controller
Channel to Peripheral Associations 110
Control Registers 111
Supported Peripherals 109
DMAC Registers
DMAxCNT 111
DMAxCON 111
DMAxPAD 111
DMAxREQ 111
DMAxSTAH/L 111
DMAxSTBH/L 111
DMT
Doze Mode 135

© 2013-2016 Microchip Technology Inc.

RPOR11 (Peripheral Pin Select Output 11) 170
RPOR12 (Peripheral Pin Select Output 12) 171
RPOR13 (Peripheral Pin Select Output 13) 171
RPOR2 (Peripheral Pin Select Output 2) 166
RPOR3 (Peripheral Pin Select Output 3) 166
RPOR4 (Peripheral Pin Select Output 4) 167
RPOR5 (Peripheral Pin Select Output 5) 167
RPOR6 (Peripheral Pin Select Output 6) 168
RPOR7 (Peripheral Pin Select Output 7) 168
RPOR8 (Peripheral Pin Select Output 8) 169
RPOR9 (Peripheral Pin Select Output 9) 169
SENTxCON1 (SENTx Control 1) 241
SENTxDATH (SENTx Receive Data High) 245
SENTxDATL (SENTx Receive Data Low) 245
SENTxSTAT (SENTx Status) 243
SEVTCMP (PWMx Primary Special Event Compare) 206
SPIxCON1 (SPIx Control 1) 226
SPIxCON2 (SPIx Control 2) 228
SPIxSTAT (SPIx Status and Control) 224
SR (CPU STATUS) 25, 101
T1CON (Timer1 Control) 174
TRGCONx (PWMx Trigger Control) 212
TRIGx (PWMx Primary Trigger Compare Value) 214
TxCON (Timer2 and Timer4 Control) 178
TyCON (Timer3 and Timer5 Control) 179
UxMODE (UARTx Mode) 249
UxSTA (UARTx Status and Control) 251
Resets 91
Brown-out Reset (BOR) 91
Configuration Mismatch Reset (CM) 91
Illegal Condition Reset (IOPUWR) 91
Illegal Address Mode 91
Illegal Opcode 91
Security 91
Uninitialized W Register 91
Master Clear Pin Reset (MCLR) 91
Master Reset Signal (SYSRST) 91
Power-on Reset (POR) 91
RESET Instruction (SWR) 91
Trap Conflict Reset (TRAPR) 91
Watchdog Timer Time-out Reset (WDTO) 91
Revision History 485

S

SENTx Protocol Data Frames 238
Serial Peripheral Interface (SPI) 221
Serial Peripheral Interface. *See* SPI.
Single-Edge Nibble Transmission (SENT) 237
Receive Mode 240
Transmit Mode 239
Single-Edge Nibble Transmission for Automotive Applications 237
Single-Edge Nibble Transmission. *See* SENT.
Software Simulator
MPLAB X SIM 339
Software Stack Pointer (SSP) 74
Special Features of the CPU 317
SPI
Control Registers 224
Helpful Tips 223

T

Temperature and Voltage Specifications
AC 351
High Temperature
AC 408
Thermal Packaging Characteristics 342
Third-Party Development Tools 340
Timer1 173
Control Register 174
Timer2/3 and Timer4/5 175
Control Registers 178
Timing Diagrams
10-Bit ADC Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0) 400
10-Bit ADC Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010) 400
12-Bit ADC Conversion (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0) 398
BOR and Master Clear Reset 354
CANx I/O 391
External Clock 352
High-Speed PWMx Characteristics 361
High-Speed PWMx Fault 361
I/O Characteristics 354
I2Cx Bus Data (Master Mode) 387
I2Cx Bus Data (Slave Mode) 389
I2Cx Bus Start/Stop Bits (Master Mode) 387
I2Cx Bus Start/Stop Bits (Slave Mode) 389
Input Capture x (ICx) 359
OCx/PWMx Characteristics 360
Output Compare x (OCx) Characteristics 360
Power-on Reset Characteristics 355
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) 377
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) 376
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 0) 374
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 1) 375
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) 385
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) 383
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) 379
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) 381
SPI2 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) 365
SPI2 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) 364
SPI2 Master Mode (Half-Duplex, Transmit Only, CKE = 0) 362
SPI2 Master Mode (Half-Duplex, Transmit Only, CKE = 1) 363
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) 372
SPI2 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) 370

© 2013-2016 Microchip Technology Inc.

NOTES:

© 2013-2016 Microchip Technology Inc.