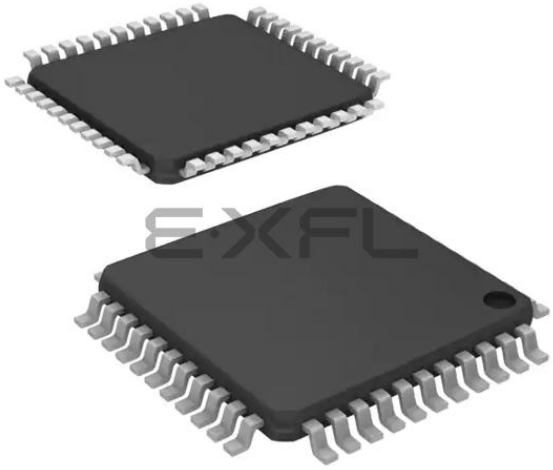
# Microchip Technology - DSPIC33EV32GM004T-I/PT Datasheet



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## What is "Embedded - Microcontrollers"?

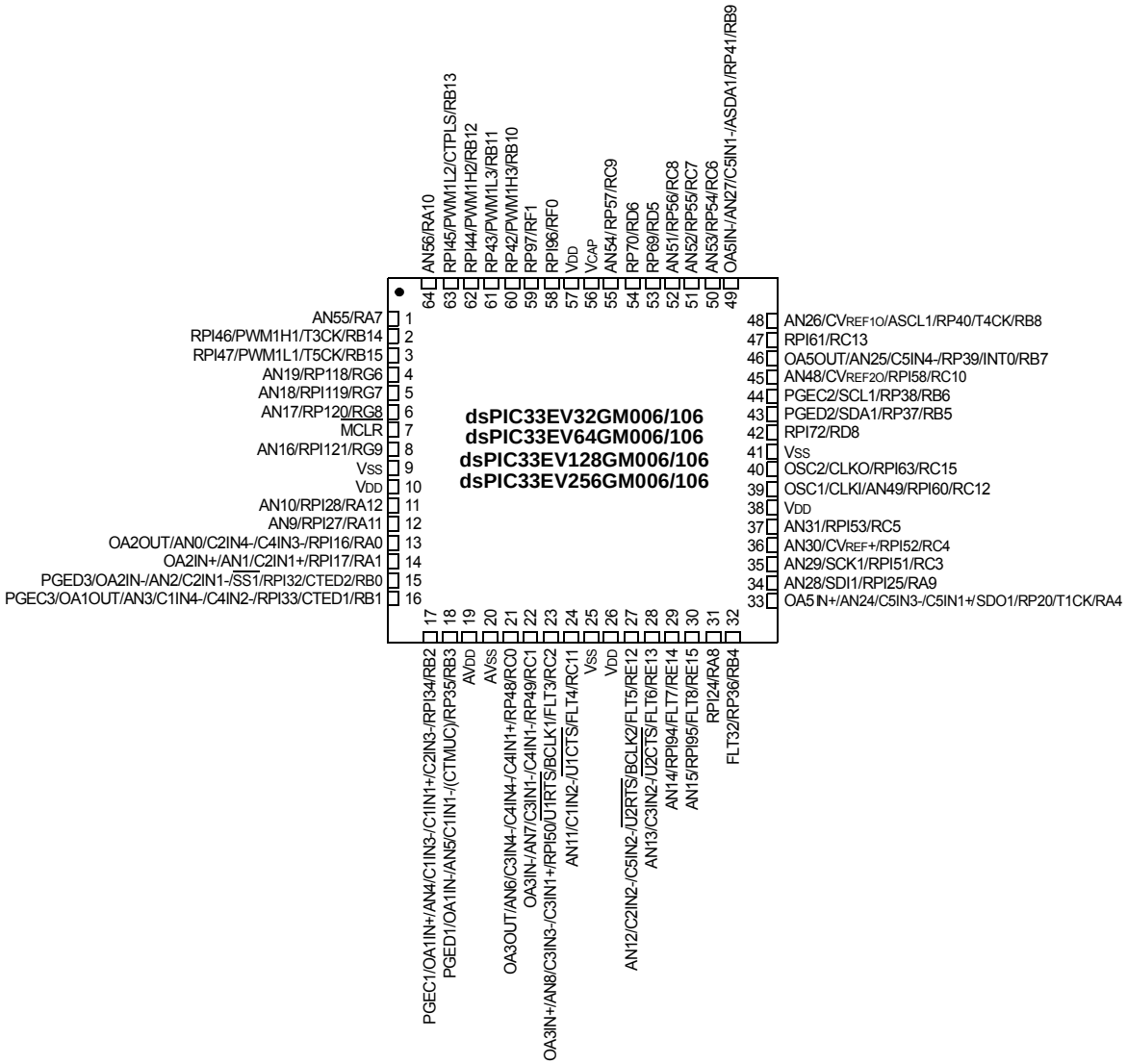
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 32KB (11K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 24x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm004t-i-pt |

## Pin Diagrams (Continued)

**64-Pin QFN(1,2,3,4)**




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

**4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | — | — | — | — | — | — | TRISA<4:0> | | | | | DF9F |
| PORTA | 0E02 | — | — | — | — | — | — | — | — | — | — | — | RA<4:0> | | | | | 0000 |
| LATA | 0E04 | — | — | — | — | — | — | — | — | — | — | — | LATA<4:0> | | | | | 0000 |
| ODCA | 0E06 | — | — | — | — | — | — | — | — | — | — | — | ODCA<4:0> | | | | | 0000 |
| CNENA | 0E08 | — | — | — | — | — | — | — | — | — | — | — | CNIEA<4:0> | | | | | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | — | — | — | — | — | — | CNPUA<4:0> | | | | | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | — | — | — | — | — | — | CNPDA<4:0> | | | | | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | ANSA4 | — | ANSA<2:0> | | | 1813 |
| SR1A | 0E10 | — | — | — | — | — | — | — | — | — | — | — | SR1A4 | — | — | — | — | 0000 |
| SR0A | 0E12 | — | — | — | — | — | — | — | — | — | — | — | SR0A4 | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E14 | TRISB<15:0> | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E16 | RB<15:0> | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E18 | LATB<15:0> | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E1A | ODCB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E1C | CNIEB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1E | CNPUB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E20 | CNPDB<15:0> | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E22 | — | — | — | — | — | — | ANSB<9:7> | | | — | — | — | ANSB<3:0> | | | | 038F |
| SR1B | 0E24 | — | — | — | — | — | — | SR1B<9:7> | | | — | — | SR1B4 | — | — | — | — | 0000 |
| SR0B | 0E26 | — | — | — | — | — | — | SR0B<9:7> | | | — | — | SR0B4 | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)**

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LSTCH<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH<3:0>:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

**REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SCK2R7 | SCK2R6 | SCK2R5 | SCK2R4 | SCK2R3 | SCK2R2 | SCK2R1 | SCK2R0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SDI2R | SDI2R6 | SDI2R5 | SDI2R4 | SDI2R3 | SDI2R2 | SDI2R1 | SDI2R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **SCK2R<7:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **SDI2R<7:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

**NOTES:**

## 13.0 TIMER2/3 AND TIMER4/5

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

**Note:** For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

**Note:** Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

**REGISTER 14-5: DMTCNTL: DEADMAN TIMER COUNT REGISTER LOW**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| COUNTER<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| COUNTER<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **COUNTER<15:0>:** Read Current Contents of Lower DMT Counter bits

**REGISTER 14-6: DMTCNTH: DEADMAN TIMER COUNT REGISTER HIGH**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| COUNTER<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| COUNTER<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **COUNTER<31:16>:** Read Current Contents of Higher DMT Counter bits

**REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = Reserved
11110 = Reserved
11101 = Reserved
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization(5)
11010 = Analog Comparator 3 is the source for the capture timer synchronization(5)
11001 = Analog Comparator 2 is the source for the capture timer synchronization(5)
11000 = Analog Comparator 1 is the source for the capture timer synchronization(5)
10111 = Analog Comparator 5 is the source for the capture timer synchronization(5)
10110 = Analog Comparator 4 is the source for the capture timer synchronization(5)
10101 = Reserved
10100 = Reserved
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = Reserved
01001 = Reserved
01000 = Input Capture 4 is the source for the capture timer synchronization(6)
00111 = Input Capture 3 is the source for the capture timer synchronization(6)
00110 = Input Capture 2 is the source for the capture timer synchronization(6)
00101 = Input Capture 1 is the source for the capture timer synchronization(6)
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Reserved

**Note 1:** The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
**2:** The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
**3:** This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
**4:** Do not use the ICx module as its own sync or trigger source.
**5:** This option should only be selected as a trigger source and not as a synchronization source.
**6:** When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

**NOTES:**

**REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER**

| HS-0, HC | HS-0, HC | HS-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC1 | DTC0 | DTCP(3) | — | — | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = Fault interrupt is not pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = Current-limit interrupt is not pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = Trigger interrupt is not pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = Trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC<1:0> = 11 for DTCP to be effective; else, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

**REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1 (CONTINUED)**

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **NIBCNT<2:0>:** Nibble Count Control bits

111 = Reserved; do not use
110 = Module transmits/receives 6 data nibbles in a SENT data pocket
101 = Module transmits/receives 5 data nibbles in a SENT data pocket
100 = Module transmits/receives 4 data nibbles in a SENT data pocket
011 = Module transmits/receives 3 data nibbles in a SENT data pocket
010 = Module transmits/receives 2 data nibbles in a SENT data pocket
001 = Module transmits/receives 1 data nibbles in a SENT data pocket
000 = Reserved; do not use

**Note 1:** This bit has no function in Receive mode (RCVEN = 1).

**2:** This bit has no function in Transmit mode (RCVEN = 0).

**REGISTER 20-3: SENTxDATL: SENTx RECEIVE DATA REGISTER LOW(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DATA4<3:0> | | | | DATA5<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DATA6<3:0> | | | | CRC<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **DATA4<3:0>:** Data Nibble 4 Data bits

bit 11-8 **DATA5<3:0>:** Data Nibble 5 Data bits

bit 7-4 **DATA6<3:0>:** Data Nibble 6 Data bits

bit 3-0 **CRC<3:0>:** CRC Nibble Data bits

**Note 1:** Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

**REGISTER 20-4: SENTxDATH: SENTx RECEIVE DATA REGISTER HIGH(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STAT<3:0> | | | | DATA1<3:0> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DATA2<3:0> | | | | DATA3<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **STAT<3:0>:** Status Nibble Data bits

bit 11-8 **DATA1<3:0>:** Data Nibble 1 Data bits

bit 7-4 **DATA2<3:0>:** Data Nibble 2 Data bits

bit 3-0 **DATA3<3:0>:** Data Nibble 3 Data bits

**Note 1:** Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

**REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0, HC | R/W-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN(1) | UTXBF | TRMT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
|---|---|---|---|---|---|---|---|
| URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HC = Hardware Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15,13 **UTXISEL<1:0>:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA® encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or has completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register (TSR) Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL<1:0>:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for transmit operation.

## 22.3 CAN Control Registers

**REGISTER 22-1: CxCTRL1: CANx CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CSIDL | ABAT | CANCKS | REQOP2 | REQOP1 | REQOP0 |
| bit 15 | | | | | | | bit 8 |

| R-1 | R-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OPMODE2 | OPMODE1 | OPMODE0 | — | CANCAP | — | — | WIN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CANx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** CANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Sets Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Sets Configuration mode
011 = Sets Listen Only mode
010 = Sets Loopback mode
001 = Sets Disable mode
000 = Sets Normal Operation mode

bit 7-5 **OPMODE<2:0>**: Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CANx Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

**REGISTER 22-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7MSK1 | F7MSK0 | F6MSK1 | F6MSK0 | F5MSK1 | F5MSK0 | F4MSK1 | F4MSK0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3MSK1 | F3MSK0 | F2MSK1 | F2MSK0 | F1MSK1 | F1MSK0 | F0MSK1 | F0MSK0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **F7MSK<1:0>:** Mask Source for Filter 7 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain the mask
01 = Acceptance Mask 1 registers contain the mask
00 = Acceptance Mask 0 registers contain the mask

bit 13-12 **F6MSK<1:0>:** Mask Source for Filter 6 bit (same values as bits 15-14)

bit 11-10 **F5MSK<1:0>:** Mask Source for Filter 5 bit (same values as bits 15-14)

bit 9-8 **F4MSK<1:0>:** Mask Source for Filter 4 bit (same values as bits 15-14)

bit 7-6 **F3MSK<1:0>:** Mask Source for Filter 3 bit (same values as bits 15-14)

bit 5-4 **F2MSK<1:0>:** Mask Source for Filter 2 bit (same values as bits 15-14)

bit 3-2 **F1MSK<1:0>:** Mask Source for Filter 1 bit (same values as bits 15-14)

bit 1-0 **F0MSK<1:0>:** Mask Source for Filter 0 bit (same values as bits 15-14)

**REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)**

bit 5-0 **CH0SA<5:0>:** Channel 0 Positive Input Select for Sample MUX A bits(1,3)

111111 = Channel 0 positive input is AN63 (Unconnected)
111110 = Channel 0 positive input is AN62 (CTMU temperature diode)
111101 = Channel 0 positive input is AN61 (internal band gap voltage)
•
•
•
011111 = Channel 0 positive input is AN31
011110 = Channel 0 positive input is AN30
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 (Op Amp 2)(2)

**Note 1:** AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

**3:** See the **"Pin Diagrams"** section for the available analog channels for each device.

## 26.0 COMPARATOR VOLTAGE REFERENCE

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

### 26.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRxCON registers (Register 26-1 and Register 26-2). The comparator voltage reference provides a range of output voltages with 128 distinct levels. The comparator reference supply voltage can come from either $V_{DD}$ and $V_{SS}$, or the external $CV_{REF}+$ and $AV_{SS}$ pins. The voltage source is selected by the CVRSS bit (CVRxCON<11>). The settling time of the comparator voltage reference must be considered when changing the $CV_{REF}$ output.

## 32.18 ADC INL

**FIGURE 32-45: TYPICAL INL ($V_{DD}$ = 5.5V, -40°C)**

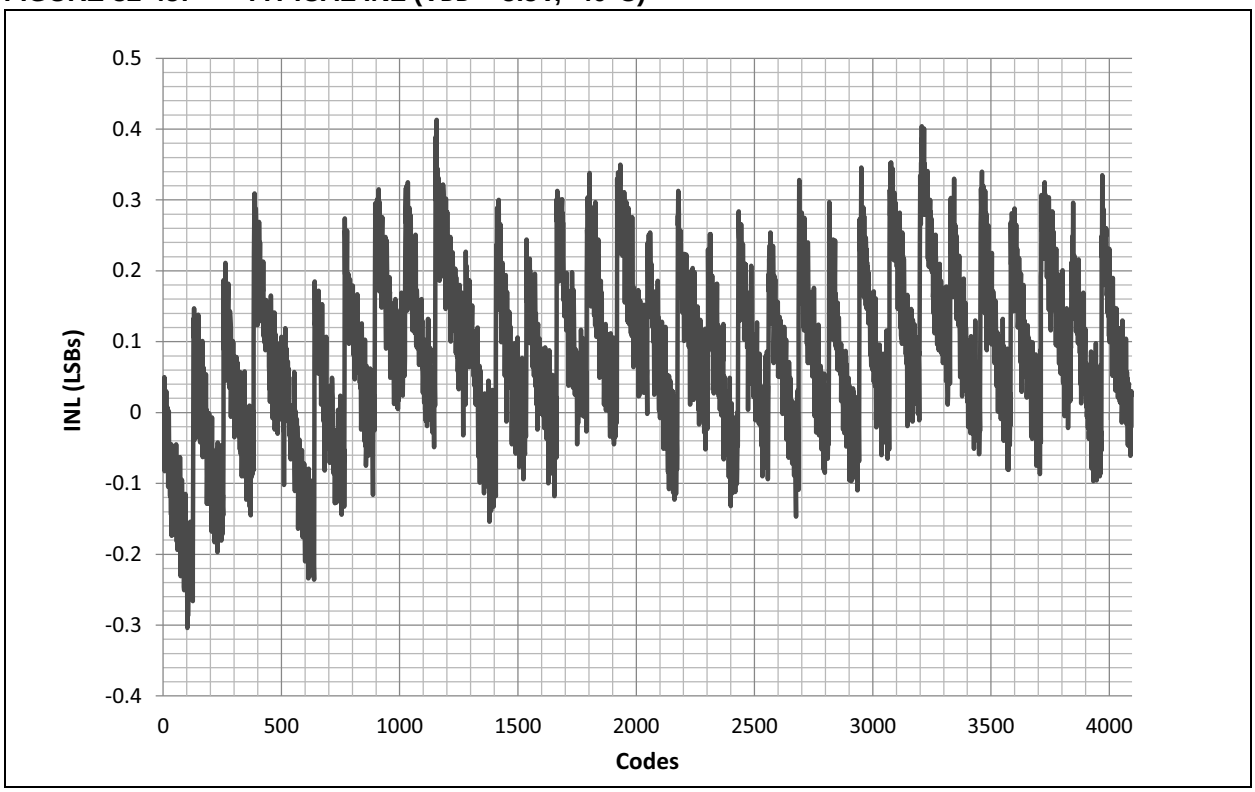



**FIGURE 32-46: TYPICAL INL ($V_{DD}$ = 5.5V, +25°C)**