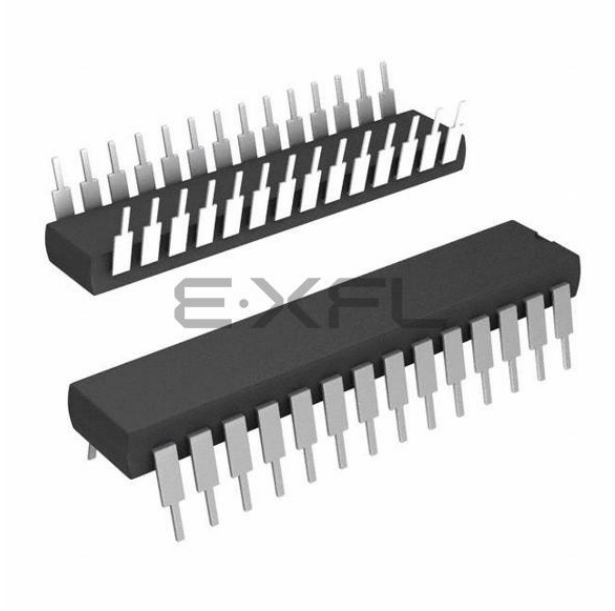
# Microchip Technology - DSPIC33EV32GM102-E/SP Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 32KB (11K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 11x10/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.300", 7.62mm) |
| Supplier Device Package | 28-SPDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm102-e-sp |

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| AN0-AN19<br>AN24-AN32<br>AN48, AN49<br>AN51-AN56 | I | Analog | No | Analog input channels. |
| CLKI | I | ST/ CMOS | No | External clock source input. Always associated with OSC1 pin function. |
| CLKO | O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1 | I | ST/ CMOS | No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise. |
| OSC2 | I/O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| REFCLKO | O | — | Yes | Reference clock output. |
| IC1-IC4 | I | ST | Yes | Capture Inputs 1 to 4. |
| OCFA | I | ST | Yes | Compare Fault A input (for compare channels). |
| OC1-OC4 | O | — | Yes | Compare Outputs 1 to 4. |
| INT0 | I | ST | No | External Interrupt 0. |
| INT1 | I | ST | Yes | External Interrupt 1. |
| INT2 | I | ST | Yes | External Interrupt 2. |
| RA0-RA4, RA7-RA12 | I/O | ST | Yes | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | Yes | PORTB is a bidirectional I/O port. |
| RC0-RC13, RC15 | I/O | ST | Yes | PORTC is a bidirectional I/O port. |
| RD5-RD6, RD8 | I/O | ST | Yes | PORTD is a bidirectional I/O port. |
| RE12-RE15 | I/O | ST | Yes | PORTE is a bidirectional I/O port. |
| RF0-RF1 | I/O | ST | No | PORTF is a bidirectional I/O port. |
| RG6-RG9 | I/O | ST | Yes | PORTG is a bidirectional I/O port. |
| T1CK | I | ST | No | Timer1 external clock input. |
| T2CK | I | ST | Yes | Timer2 external clock input. |
| T3CK | I | ST | No | Timer3 external clock input. |
| T4CK | I | ST | No | Timer4 external clock input. |
| T5CK | I | ST | No | Timer5 external clock input. |
| CTPLS | O | ST | No | CTMU pulse output. |
| CTED1 | I | ST | No | CTMU External Edge Input 1. |
| CTED2 | I | ST | No | CTMU External Edge Input 2. |
| $\overline{\text{U1CTS}}$ | I | ST | Yes | UART1 Clear-to-Send. |
| $\overline{\text{U1RTS}}$ | O | — | Yes | UART1 Ready-to-Send. |
| U1RX | I | ST | Yes | UART1 receive. |
| U1TX | O | — | Yes | UART1 transmit. |
| $\overline{\text{U2CTS}}$ | I | ST | Yes | UART2 Clear-to-Send. |
| $\overline{\text{U2RTS}}$ | O | — | Yes | UART2 Ready-to-Send. |
| U2RX | I | ST | Yes | UART2 receive. |
| U2TX | O | — | Yes | UART2 transmit. |
| SCK1 | I/O | ST | No | Synchronous serial clock input/output for SPI1. |
| SDI1 | I | ST | No | SPI1 data in. |
| SDO1 | O | — | No | SPI1 data out. |
| $\overline{\text{SS1}}$ | I/O | ST | No | SPI1 slave synchronization or frame pulse I/O. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

## 3.7 Arithmetic Logic Unit (ALU)

The dsPIC33EVXXXGM00X/10X family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. The data for the ALU operation can come from the W register array or from the data memory, depending on the addressing mode of the instruction. Similarly, the output data from the ALU can be written to the W register array or a data memory location.

For information on the SR bits affected by each instruction, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

### 3.7.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

### 3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes the single-cycle per bit of the divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

## 3.8 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON) as follows:

- Fractional or Integer DSP Multiply (IF)
- Signed, Unsigned or Mixed-Sign DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

**TABLE 3-2: DSP INSTRUCTIONS SUMMARY**

| Instruction | Algebraic Operation | ACC Write Back |
|---|---|---|
| `CLR` | $A = 0$ | Yes |
| `ED` | $A = (x - y)^2$ | No |
| `EDAC` | $A = A + (x - y)^2$ | No |
| `MAC` | $A = A + (x \cdot y)$ | Yes |
| `MAC` | $A = A + x^2$ | No |
| `MOVSAC` | No change in A | Yes |
| `MPY` | $A = x \cdot y$ | No |
| `MPY` | $A = x^2$ | No |
| `MPY.N` | $A = -x \cdot y$ | No |
| `MSC` | $A = A - x \cdot y$ | Yes |

**TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1BUFPNT1 | 0420 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 | 0000 |
| C1BUFPNT2 | 0422 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C1BUFPNT3 | 0424 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C1BUFPNT4 | 0426 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C1RXM0SID | 0430 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM0EID | 0432 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM1EID | 0436 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM2EID | 043A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF0EID | 0442 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF1EID | 0446 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF2EID | 044A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF3EID | 044E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF4EID | 0452 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF5EID | 0456 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF6EID | 045A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF7EID | 045E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF8EID | 0462 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF9EID | 0466 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF10EID | 046A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-24: OUTPUT COMPARE REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — | ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Output Compare 1 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC2CON1 | 090A | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — | ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC2R | 0910 | Output Compare 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC2TMR | 0912 | Output Compare 2 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC3CON1 | 0914 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — | ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC3RS | 0918 | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC3R | 091A | Output Compare 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC3TMR | 091C | Output Compare 3 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC4CON1 | 091E | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | — | ENFLTA | — | — | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC4R | 0924 | Output Compare 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC4TMR | 0926 | Output Compare 4 Timer Value Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2**

| R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| GIE | DISI | SWTRAP | — | — | — | — | AIVTEN |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT2EP | INT1EP | INT0EP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IECx bits are enabled
0 = Interrupts are disabled, but traps are still enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled

bit 12-9 **Unimplemented:** Read as ‘0’

bit 8 **AIVTEN:** Alternate Interrupt Vector Table is Enabled bit
1 = AIVT is enabled
0 = AIVT is disabled

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

**NOTES:**

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| T5MD | T4MD | T3MD | T2MD | T1MD | — | PWMMD | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD(1) | AD1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **Unimplemented:** Read as '0'

bit 9 **PWMMD:** PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

**Note 1:** This bit is available on dsPIC33EVXXXGM10X devices only.

## 11.4 Slew Rate Selection

The slew rate selection feature allows the device to have control over the slew rate selection on the required I/O pin which supports this feature. For this purpose, for each I/O port, there are two registers: SR1x and SR0x, which configure the selection of the slew rate. The register outputs are directly connected to the associated I/O pins, which support the slew rate selection function. The SR1x register specifies the MSb and the SR0x register provides the LSb of the 2-bit field that selects the desired slew rate. For example, slew rate selections for PORTA are as follows:

**EXAMPLE 11-2: SLEW RATE SELECTIONS FOR PORTA**

```
SR1Ax, SR0Ax = 00 = Fastest Slew rate
SR1Ax, SR0Ax = 01 = 4x slower Slew rate
SR1Ax, SR0Ax = 10 = 8x slower Slew rate
SR1Ax, SR0Ax = 11 = 16x slower Slew rate
```

## 11.5 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping after it has been established.

### 11.5.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn” or “RPIn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

### 11.5.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and Interrupt-on-Change (IOC) inputs.

In comparison, some digital only peripheral modules are never included in the PPS feature, because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $I^2C$ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between the remappable and non-remappable peripherals is that the remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, the non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all the other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.5.3 CONTROLLING PERIPHERAL PIN SELECT

The PPS features are controlled through two sets of SFRs: one to map the peripheral inputs and the other to map the outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 11.5.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Table 11-1 and Register 11-1 through Register 11-17). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral’s bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selects supported by the device.

**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|
| 000 0000 | I | Vss |
| 000 0001 | I | CMP1(1) |
| 000 0010 | I | CMP2(1) |
| 000 0011 | I | CMP3(1) |
| 000 0100 | I | CMP4(1) |
| 000 0101 | — | — |
| 000 1100 | I | CMP5(1) |
| 000 1101 | — | — |
| 000 1110 | — | — |
| 000 1111 | — | — |
| 001 0000 | I | RPI16 |
| 001 0001 | I | RPI17 |
| 001 0010 | I | RPI18 |
| 001 0011 | I | RPI19 |
| 001 0100 | I/O | RP20 |
| 001 0101 | — | — |
| 001 0110 | — | — |
| 001 0111 | — | — |
| 001 1000 | I | RPI24 |
| 001 1001 | I | RPI25 |
| 001 1010 | — | — |
| 001 1011 | I | RPI27 |
| 001 1100 | I | RPI28 |
| 001 1101 | — | — |
| 001 1110 | — | — |
| 001 1111 | — | — |
| 010 0000 | I | RPI32 |
| 010 0001 | I | RPI33 |
| 010 0010 | I | RPI34 |
| 010 0011 | I/O | RP35 |
| 010 0100 | I/O | RP36 |
| 010 0101 | I/O | RP37 |
| 010 0110 | I/O | RP38 |
| 010 0111 | I/O | RP39 |
| 010 1000 | I/O | RP40 |
| 010 1100 | I | RPI44 |
| 010 1101 | I | RPI45 |
| 010 1110 | I | RPI46 |
| 010 1111 | I | RPI47 |
| 011 0000 | I/O | RP48 |
| 011 0010 | I | RPI50 |
| 011 0011 | I | RPI51 |
| 011 0100 | I | RPI52 |
| 011 0101 | I | RPI53 |
| 011 0110 | I/O | RP54 |
| 011 0111 | I/O | RP55 |
| 011 1000 | I/O | RP56 |
| 011 1001 | I/O | RP57 |
| 011 1010 | I | RPI58 |
| 011 1011 | — | — |
| 011 1100 | I | RPI60 |
| 011 1101 | I | RPI61 |
| 011 1110 | — | — |
| 011 1111 | I | RPI 63 |
| 100 0000 | — | — |
| 100 0001 | — | — |
| 100 0010 | — | — |
| 100 0011 | — | — |
| 100 0100 | — | — |
| 100 0101 | I/O | RP69 |
| 100 0110 | I/O | RP70 |
| 100 0111 | — | — |
| 100 1000 | I | RPI72 |
| 100 1001 | — | — |
| 100 1010 | — | — |
| 100 1011 | — | — |
| 100 1110 | — | — |
| 100 1111 | — | — |
| 101 0010 | — | — |
| 101 0011 | — | — |
| 101 0100 | — | — |
| 010 1001 | I/O | RP41 |
| 010 1010 | I/O | RP42 |
| 010 1011 | I/O | RP43 |
| 101 1000 | — | — |
| 101 1001 | — | — |
| 101 1010 | — | — |
| 101 1011 | — | — |
| 101 1100 | — | — |
| 101 1101 | — | — |

**Legend:** Shaded rows indicate the PPS Input register values that are unimplemented.

**Note 1:** These are virtual pins. See **Section 11.5.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

**REGISTER 14-7: DMTPSCNTL: DMT POST CONFIGURE COUNT STATUS REGISTER LOW**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PSCNT<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PSCNT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PSCNT<15:0>:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

**REGISTER 14-8: DMTPSCNTH: DMT POST CONFIGURE COUNT STATUS REGISTER HIGH**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PSCNT<31:24> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PSCNT<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PSCNT<31:16>:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

**REGISTER 21-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Baud rate measurement on the next character is enabled – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or has completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**3:** This feature is only available on 44-pin and 64-pin devices.

**4:** This feature is only available on 64-pin devices.

**BUFFER 22-7: CANx MESSAGE BUFFER WORD 6**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 7<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 6<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 7<15:8>:** CANx Message Byte 7 bits

bit 7-0 **Byte 6<7:0>:** CANx Message Byte 6 bits

**BUFFER 22-8: CANx MESSAGE BUFFER WORD 7**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT<4:0>(1) | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Code bits(1)
Encodes number of filter that resulted in writing this buffer.

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** Only written by module for receive buffers, unused for transmit buffers.

**REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)**

bit 7-5 **SSRC<2:0>:** Sample Clock Source Select bits

If SSRCG = 1:
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion

If SSRCG = 0:
111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = CTMU ends sampling and starts conversion
101 = Reserved
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Trigger Source Group bit

See SSRC<2:0> for details.

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)

In 12-Bit Mode (AD12B = 1), SIMSAM is Unimplemented and is Read as '0':
1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x) or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADCx Sample Auto-Start bit

1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADCx Sample Enable bit

1 = ADCx Sample-and-Hold amplifiers are sampling
0 = ADCx Sample-and-Hold amplifiers are holding
If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write '0' to end sampling and start conversion. If SSRC<2:0> ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADCx Conversion Status bit(1)

1 = ADCx conversion cycle is completed.
0 = ADCx conversion has not started or is in progress
Automatically set by hardware when conversion is complete. Software can write '0' to clear DONE bit status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

**Note 1:** Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

**TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | See **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 25 | MHz | See **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 and **Note 4** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 and **Note 4** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 20 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 20 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 15 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | See **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}$ ↑ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | See **Note 4** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-32: CANx MODULE I/O TIMING CHARACTERISTICS**

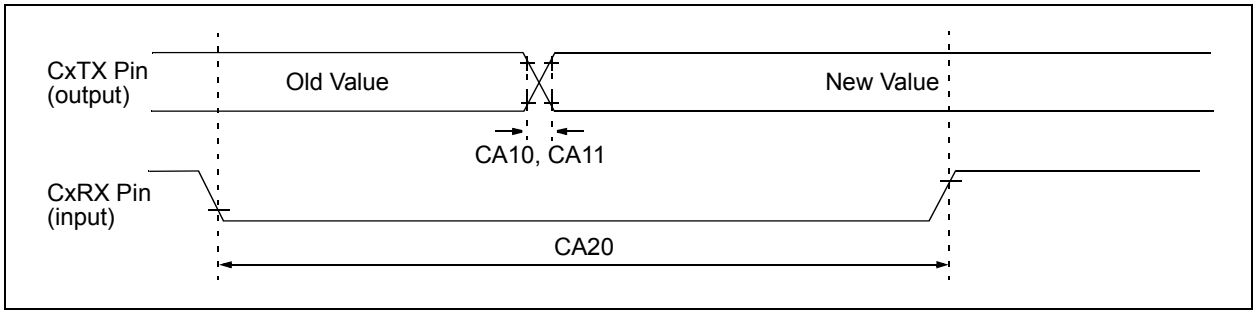



**TABLE 30-48: CANx MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CA10 | TIOF | Port Output Fall Time | — | — | — | ns | See Parameter DO32 |
| CA11 | TIOR | Port Output Rise Time | — | — | — | ns | See Parameter DO31 |
| CA20 | TCWF | Pulse Width to Trigger CAN Wake-up Filter | 120 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 30-33: UARTx MODULE I/O TIMING CHARACTERISTICS**

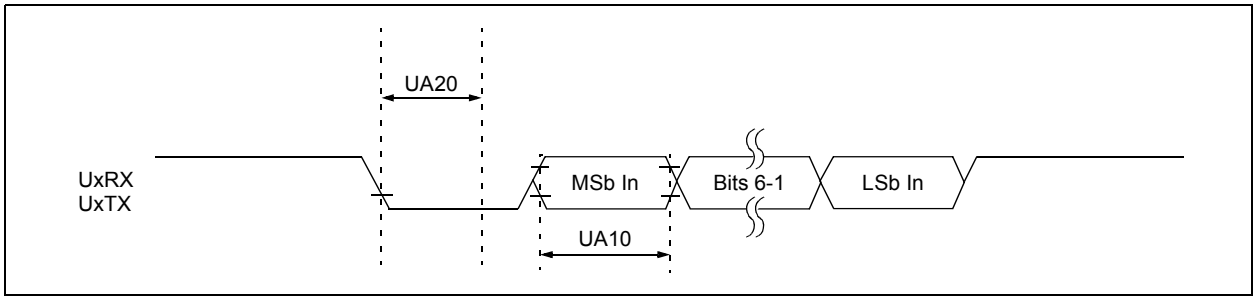



**TABLE 30-49: UARTx MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| UA10 | TUABAUD | UARTx Baud Time | 66.67 | — | — | ns | |
| UA11 | FBAUD | UARTx Baud Frequency | — | — | 15 | Mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UARTx Wake-up | 500 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

## 33.2 IIDLE

**FIGURE 33-5: TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)**

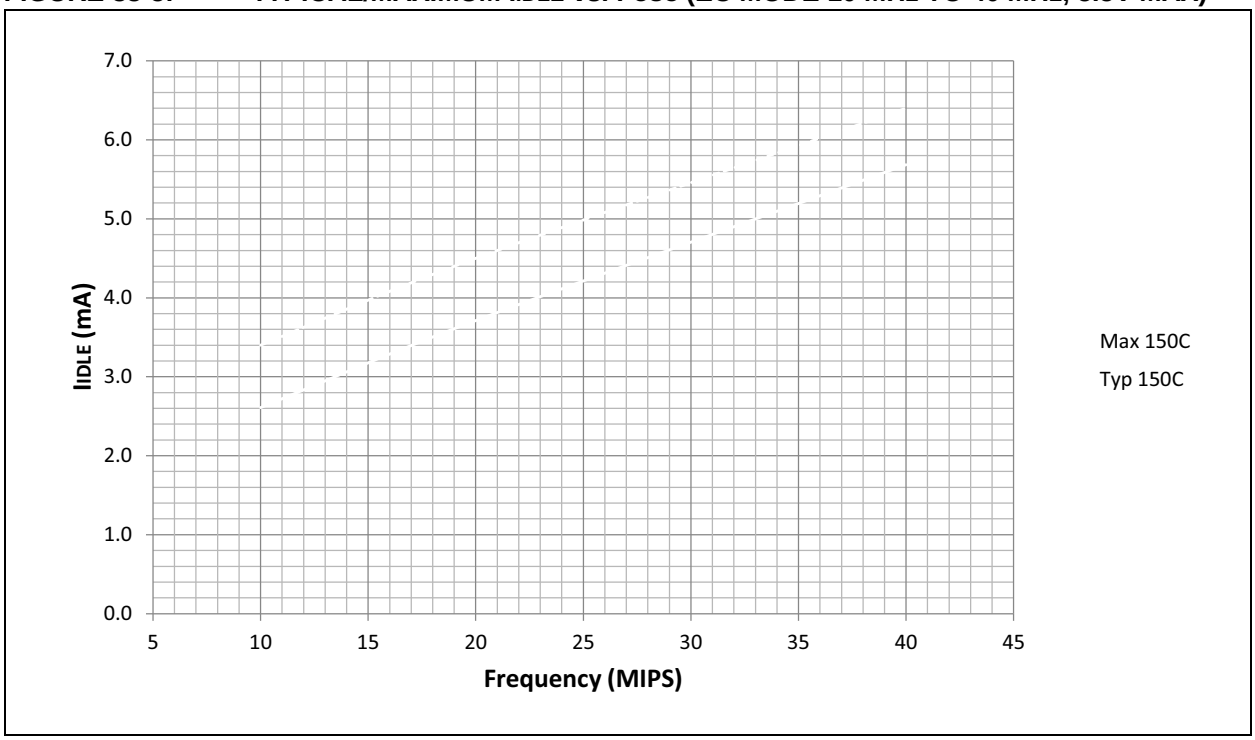



**FIGURE 33-6: TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)**

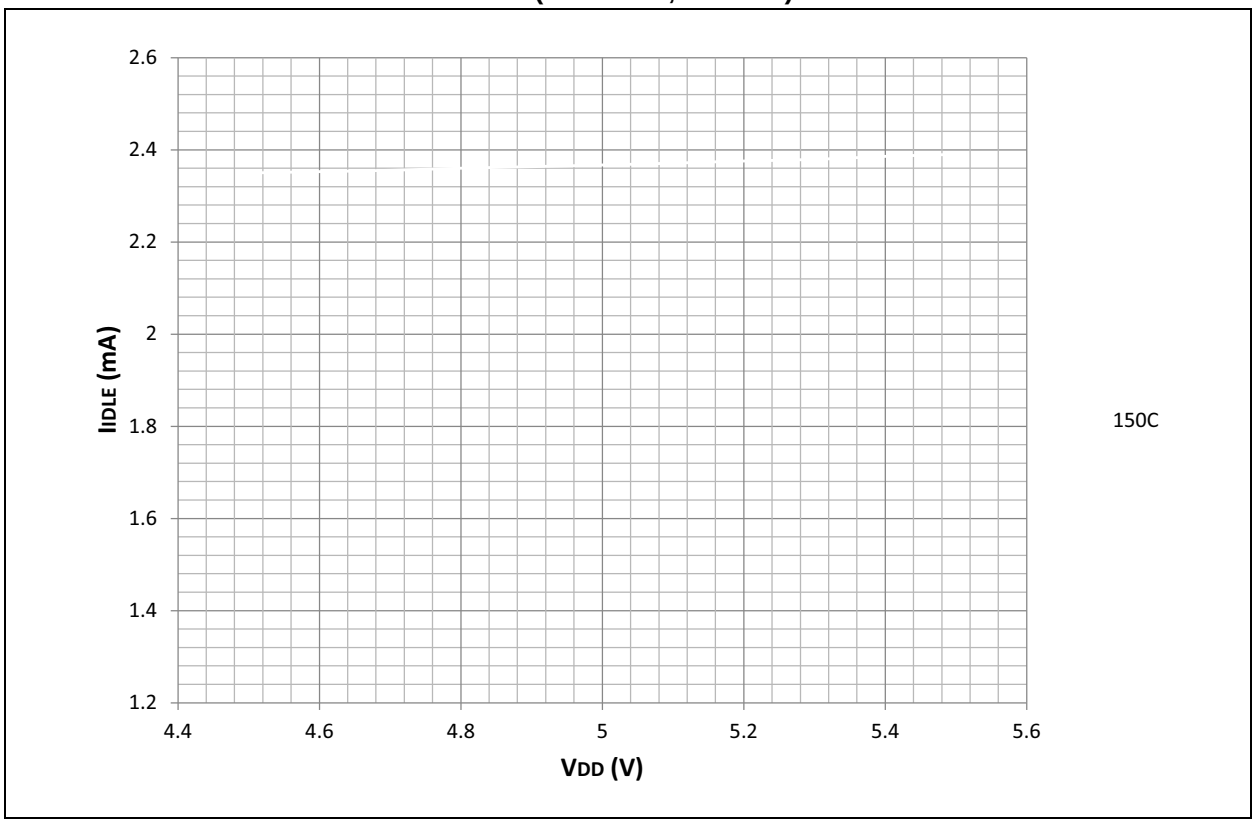


**FIGURE 33-11: TYPICAL IDOZE VS. VDD (DOZE 1:128, 70 MIPS)**

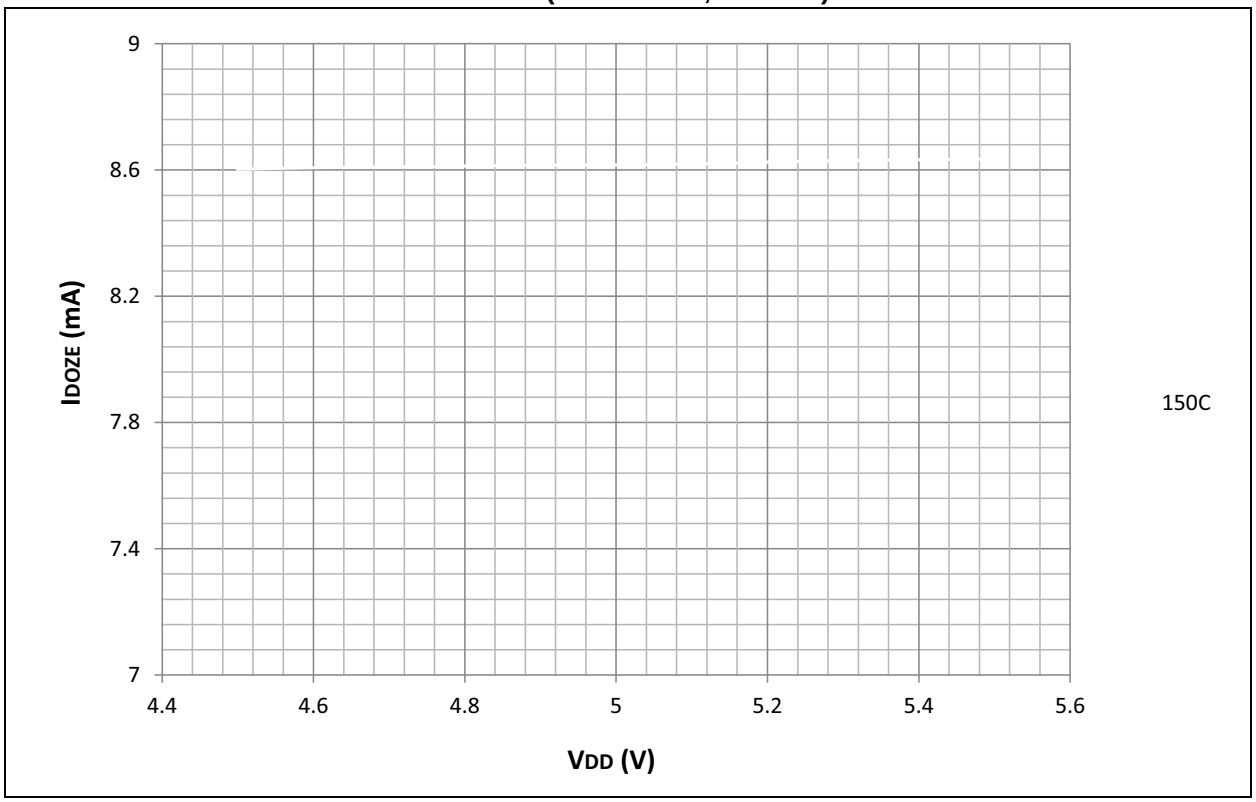
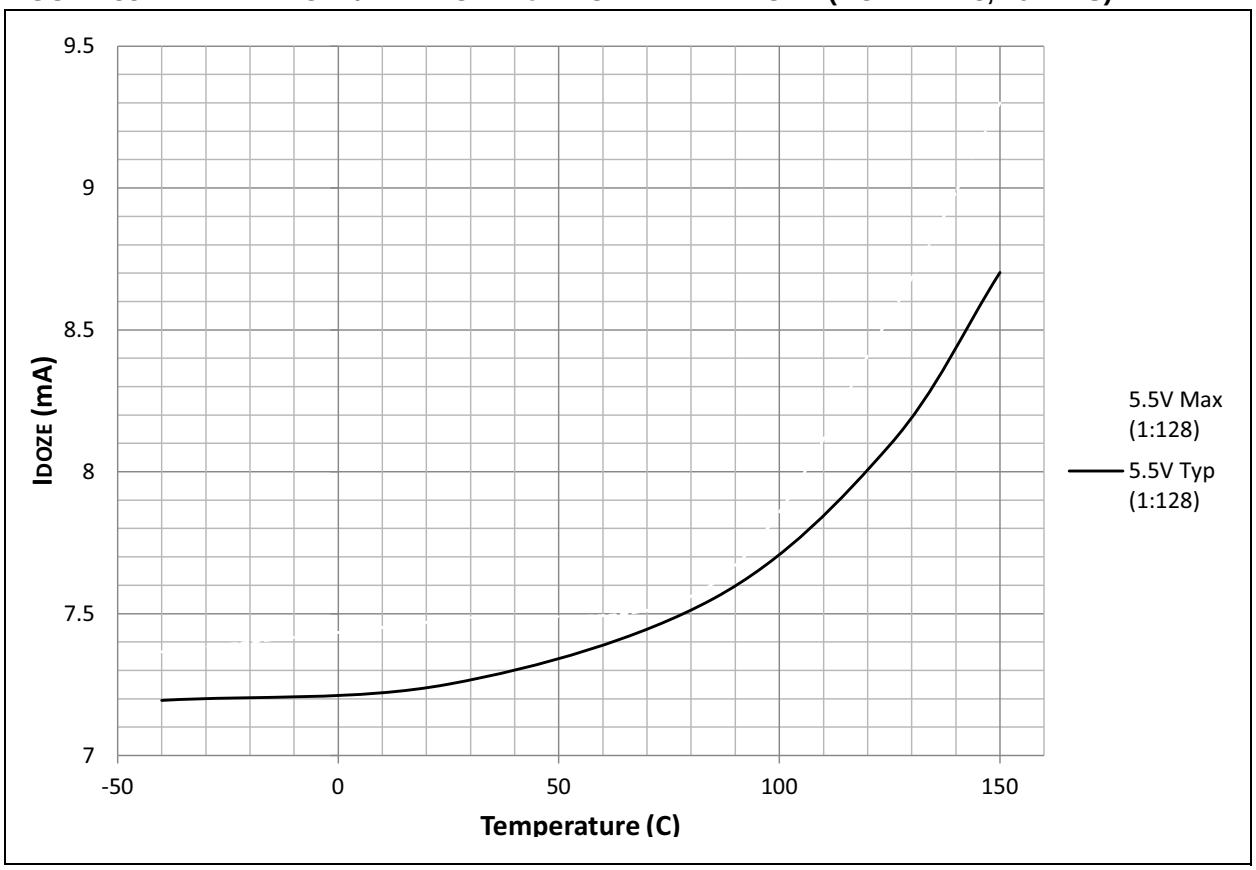



**FIGURE 33-12: TYPICAL/MAXIMUM IDOZE VS. TEMPERATURE (DOZE 1:128, 70 MIPS)**



## INDEX

### A



### B

**NOTES:**