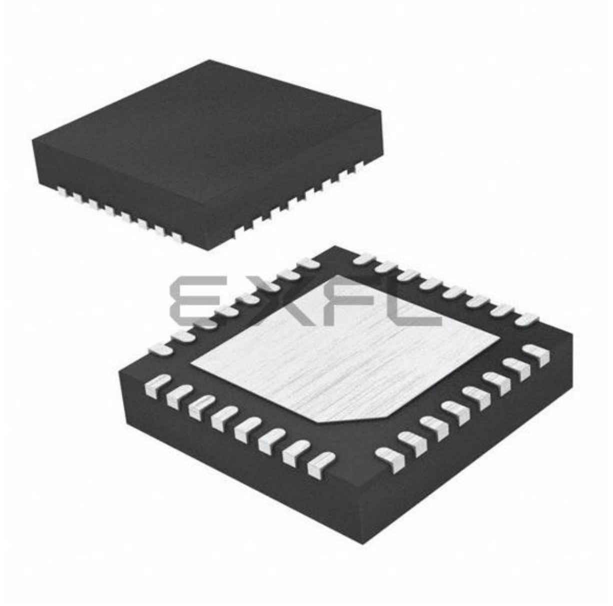


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm102-i-mm

3.7 Arithmetic Logic Unit (ALU)

The dsPIC33EVXXXGM00X/10X family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. The data for the ALU operation can come from the W register array or from the data memory, depending on the addressing mode of the instruction. Similarly, the output data from the ALU can be written to the W register array or a data memory location.

For information on the SR bits affected by each instruction, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.7.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes the single-cycle per bit of the divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.8 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

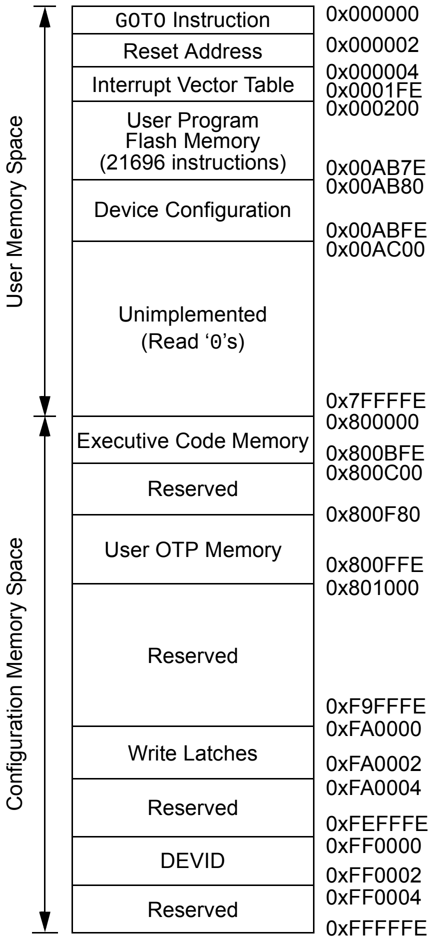
The DSP engine has options selected through bits in the CPU Core Control register (CORCON) as follows:

- Fractional or Integer DSP Multiply (IF)
- Signed, Unsigned or Mixed-Sign DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

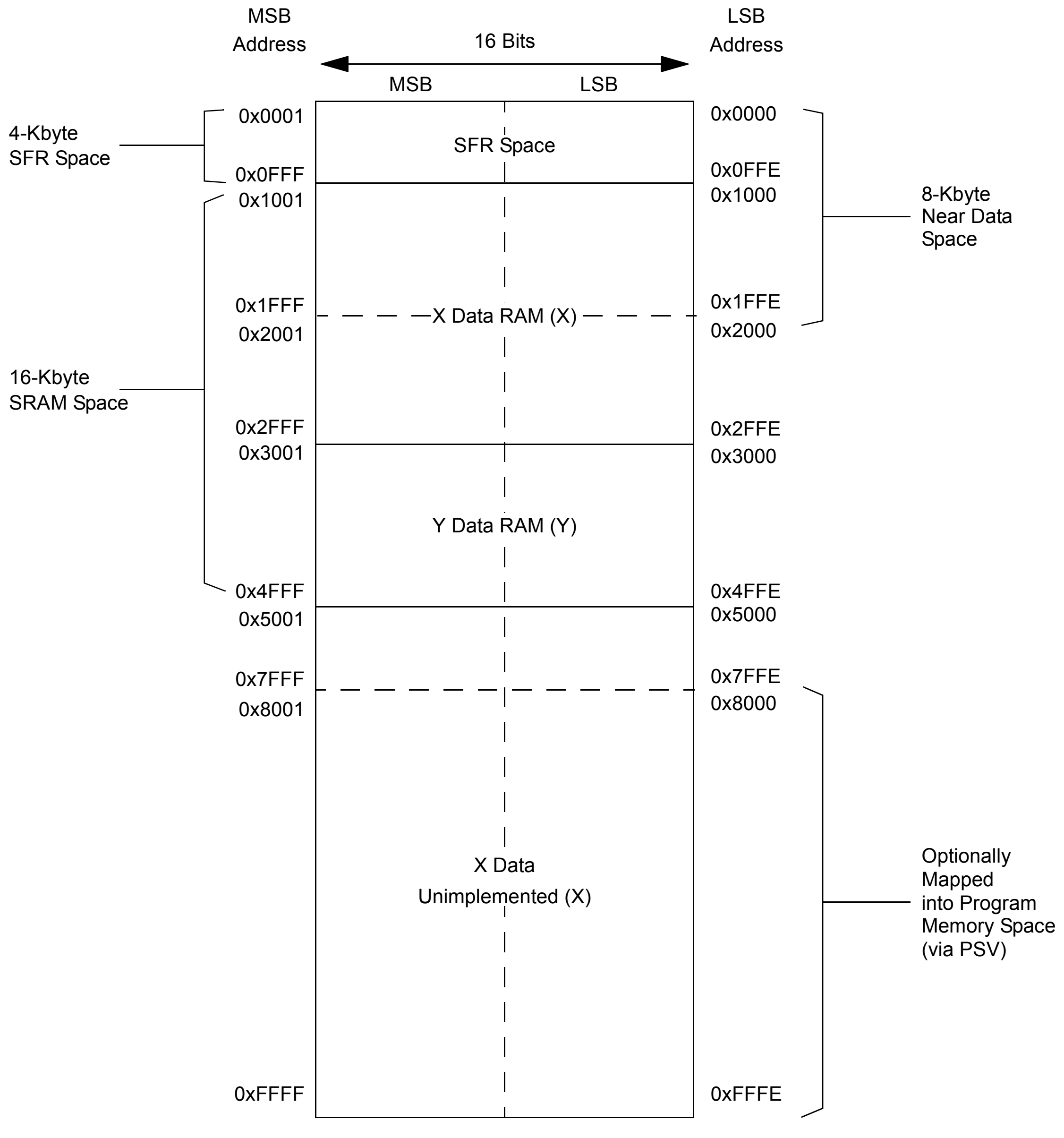
Instruction	Algebraic Operation	ACC Write Back
`CLR`	$A = 0$	Yes
`ED`	$A = (x - y)^2$	No
`EDAC`	$A = A + (x - y)^2$	No
`MAC`	$A = A + (x \bullet y)$	Yes
`MAC`	$A = A + x^2$	No
`MOVSAC`	No change in A	Yes
`MPY`	$A = x \bullet y$	No
`MPY`	$A = x^2$	No
`MPY.N`	$A = - x \bullet y$	No
`MSC`	$A = A - x \bullet y$	Yes

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EV64GM00X/10X DEVICES[1]



Note 1: Memory areas are not shown to scale.

FIGURE 4-8: DATA MEMORY MAP FOR 256-Kbyte DEVICES(1)



Note 1: Memory areas are not shown to scale.

4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																0000
W1	0002	W1																0000
W2	0004	W2																0000
W3	0006	W3																0000
W4	0008	W4																0000
W5	000A	W5																0000
W6	000C	W6																0000
W7	000E	W7																0000
W8	0010	W8																0000
W9	0012	W9																0000
W10	0014	W10																0000
W11	0016	W11																0000
W12	0018	W12																0000
W13	001A	W13																0000
W14	001C	W14																0000
W15	001E	W15																0800
SPLIM	0020	SPLIM																xxxx
ACCAL	0022	ACCAL																xxxx
ACCAH	0024	ACCAH																xxxx
ACCAU	0026	Sign Extension of ACCA<39>								ACCAU								xxxx
ACCBL	0028	ACCBL																xxxx
ACCBH	002A	ACCBH																xxxx
ACCBU	002C	Sign Extension of ACCB<39>								ACCBU								xxxx
PCL	002E	Program Counter Low Word Register															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register							0000
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										0001
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register									0001
RCOUNT	0036	REPEAT Loop Counter Register															0	xxxx
DCOUNT	0038	DCOUNT<15:1>															0	xxxx
DOSTARTL	003A	DOSTARTL<15:1>															0	xxxx
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>						00xx
DOENDL	003E	DOENDL<15:1>															—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

NOTES:

REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT1R<7:0>							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘`0`’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SENT1R<7:0>:** Assign SENT Module Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

`10110101` = Input tied to RPI181
•
•
•
`00000001` = Input tied to CMP1
`00000000` = Input tied to VSS

bit 7-0 **Unimplemented:** Read as ‘`0`’

REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT2R<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘`0`’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘`0`’

bit 7-0 **SENT2R<7:0>:** Assign SENT Module Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

`10110101` = Input tied to RPI181
•
•
•
`00000001` = Input tied to CMP1
`00000000`= Input tied to VSS

16.1 Output Compare Control Registers

REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘`0`’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘`0`’

bit 13 **OCSIDL:** Output Compare x Stop in Idle Mode Control bit

`1` = Output Compare x halts in CPU Idle mode
`0` = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits

`111` = Peripheral clock (FP)
`110` = Reserved
`101` = Reserved
`100` = T1CLK is the clock source of the OCx (only the synchronous clock is supported)
`011` = T5CLK is the clock source of the OCx
`010` = T4CLK is the clock source of the OCx
`001` = T3CLK is the clock source of the OCx
`000` = T2CLK is the clock source of the OCx

bit 9-8 **Unimplemented:** Read as ‘`0`’

bit 7 **ENFLTA:** Output Compare x Fault A Input Enable bit

`1` = Output Compare Fault A (OCFA) input is enabled
`0` = Output Compare Fault A (OCFA) input is disabled

bit 6-5 **Unimplemented:** Read as ‘`0`’

bit 4 **OCFLTA:** PWM Fault A Condition Status bit

`1` = PWM Fault A condition on the OCFA pin has occurred
`0` = PWM Fault A condition on the OCFA pin has not occurred

bit 3 **TRIGMODE:** Trigger Status Mode Select bit

`1` = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
`0` = TRIGSTAT is cleared only by software

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

NOTES:

20.2 Transmit Mode

By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME<15:0> (SENTxCON2<15:0>) bits. The tick period calculations are shown in Equation 20-1.

EQUATION 20-1: TICK PERIOD CALCULATION

$$TICKTIME\langle 15:0\rangle = \frac{T_{TICK}}{T_{CLK}} - 1$$

An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing a value to the FRAMETIME<15:0> (SENTxCON3<15:0>) bits. The formulas used to calculate the value of frame time are shown in Equation 20-2.

EQUATION 20-2: FRAME TIME CALCULATIONS

$$FRAMETIME\langle 15:0\rangle = T_{TICK}/T_{FRAME}$$

$$FRAMETIME\langle 15:0\rangle \geq 122 + 27N$$

$$FRAMETIME\langle 15:0\rangle \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME<15:0> value. FRAMETIME<15:0> values beyond 2047 will have no effect on the length of a data frame.

20.2.1 TRANSMIT MODE CONFIGURATION

20.2.1.1 Initializing the SENTx Module:

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1<11>) = `0` for Transmit mode.
2. Write TXM (SENTxCON1<10>) = `0` for Asynchronous Transmit mode or TXM = `1` for Synchronous mode.
3. Write NIBCNT<2:0> (SENTxCON1<2:0>) for the desired data frame length.
4. Write CRCEN (SENTxCON1<8>) for hardware or software CRC calculation.
5. Write PPP (SENTxCON1<7>) for optional pause pulse.
6. If PPP = `1`, write T_{FRAME} to SENTxCON3.
7. Write SENTxCON2 with the appropriate value for desired tick period.
8. Enable interrupts and set interrupt priority.
9. Write initial status and data values to SENTxDATH/L.
10. If CRCEN = `0`, calculate CRC and write the value to CRC<3:0> (SENTxDATL<3:0>).
11. Set the SNTEN (SENTxCON1<15>) bit to enable the module.

User software updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R/C-0	R-0	R/W-0, HC
PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN(1)
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7 **PAUSE:** Pause Period Status bit

1 = The module is transmitting/receiving a pause period
0 = The module is not transmitting/receiving a pause period

bit 6-4 **NIB<2:0>:** Nibble Status bit

Module in Transmit Mode (RCVEN = 0):
111 = Module is transmitting a CRC nibble
110 = Module is transmitting Data Nibble 6
101 = Module is transmitting Data Nibble 5
100 = Module is transmitting Data Nibble 4
011 = Module is transmitting Data Nibble 3
010 = Module is transmitting Data Nibble 2
001 = Module is transmitting Data Nibble 1
000 = Module is transmitting a status nibble or pause period, or is not transmitting

Module in Receive Mode (RCVEN = 1):
111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred
110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
000 = Module is receiving a status nibble or waiting for Sync

bit 3 **CRCERR:** CRC Status bit (Receive mode only)

1 = A CRC error occurred for the 1-6 data nibbles in SENTxDATH/L
0 = A CRC error has not occurred

bit 2 **FRMERR:** Framing Error Status bit (Receive mode only)

1 = A data nibble was received with less than 12 tick periods or greater than 27 tick periods
0 = Framing error has not occurred

bit 1 **RXIDLE:** SENTx Receiver Idle Status bit (Receive mode only)

1 = The SENTx data bus has been Idle (high) for a period of SYNCMAX<15:0> or greater
0 = The SENTx data bus is not Idle

Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

22.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EVXXXGM10X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Enhanced Controller Area Network (ECAN™)"** (DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

22.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EVXXXGM10X devices contain one CAN module.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The CAN module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0 to 8-Byte Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to Eight Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback Mode Supports Self-Test Operation
- Signaling through Interrupt Capabilities for All CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle Modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors, and then matched against filters to see if it should be received and stored in one of the Receive registers.

Figure 22-1 shows a block diagram of the CANx module.

25.0 OP AMP/COMPARATOR MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

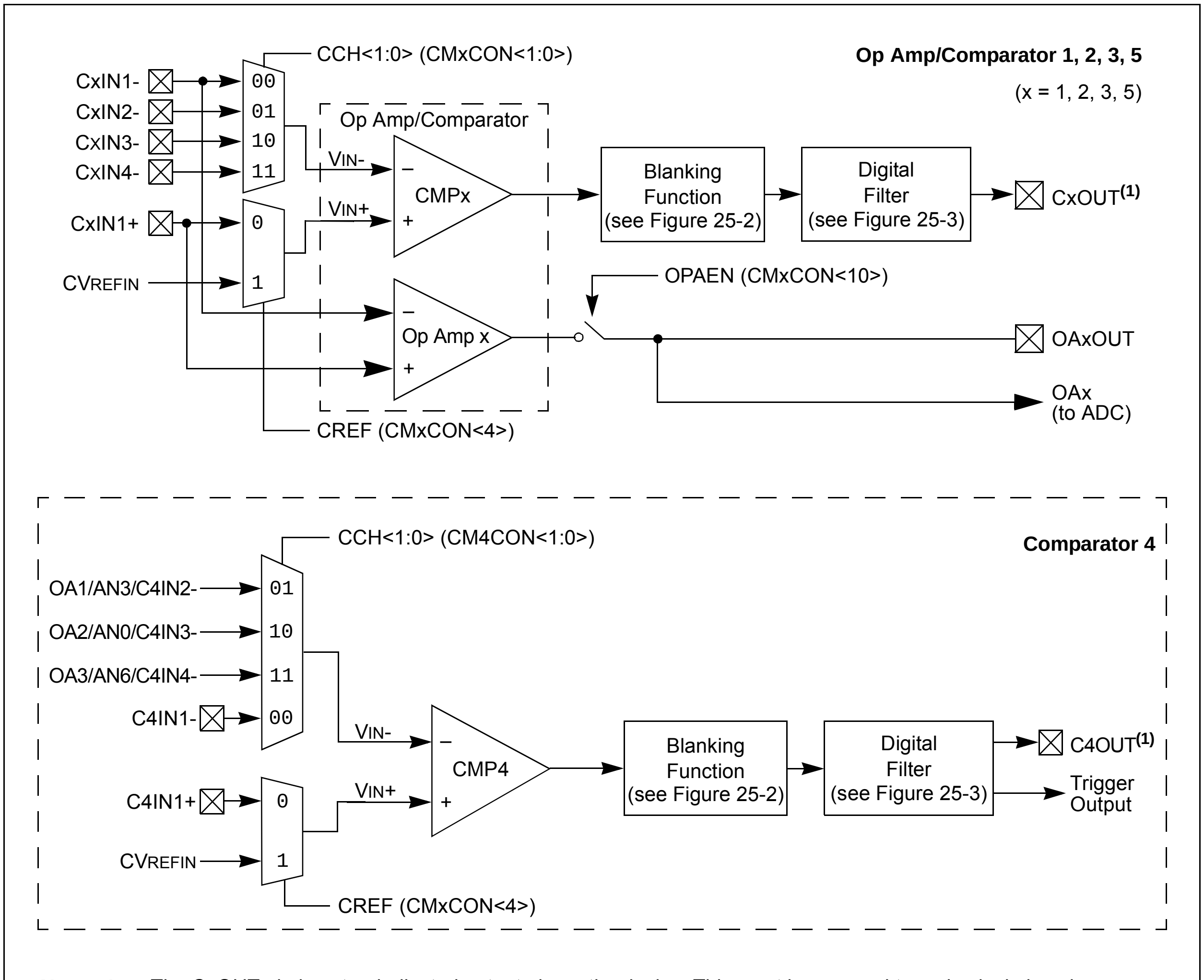
The dsPIC33EVXXXGM00X/10X family devices contain up to five comparators that can be configured in various ways. CMP1, CMP2, CMP3 and CMP5 also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

The following options allow users to:

- Select the Edge for Trigger and Interrupt Generation
- Configure the Comparator Voltage Reference
- Configure Output Blanking and Masking
- Configure as a Comparator or Op Amp (CMP1, CMP2, CMP3 and CMP5 only)

Note: Not all op amp/comparator input/output connections are available on all devices. See the **"Pin Diagrams"** section for available connections.

FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM



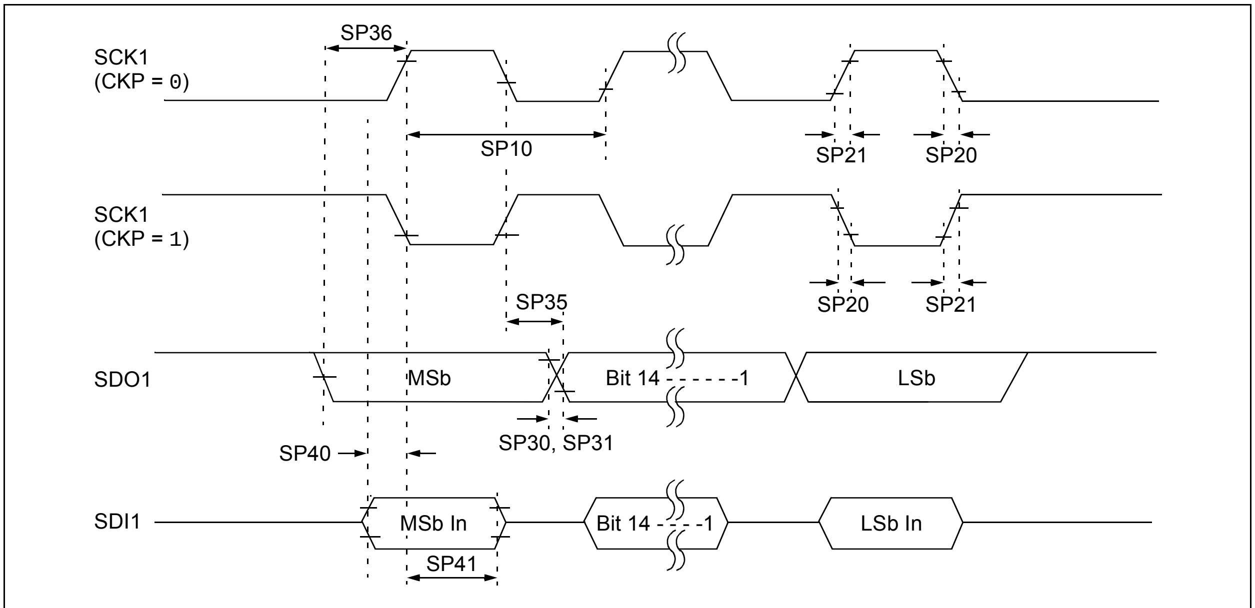
Note 1: The CxOUT pin is not a dedicated output pin on the device. This must be mapped to a physical pin using Peripheral Pin Select (PPS). Refer to **Section 11.0 "I/O Ports"** for more information.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
53	`MUL`	`MUL.SS  Wb,Ws,Wnd`	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		`MUL.SS  Wb,Ws,Acc`	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		`MUL.SU  Wb,Ws,Wnd`	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		`MUL.SU  Wb,Ws,Acc`	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		`MUL.SU  Wb,#lit5,Acc`	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		`MUL.US  Wb,Ws,Wnd`	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		`MUL.US  Wb,Ws,Acc`	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		`MUL.UU  Wb,Ws,Wnd`	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		`MUL.UU  Wb,#lit5,Acc`	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		`MUL.UU  Wb,Ws,Acc`	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		`MULW.SS  Wb,Ws,Wnd`	Wnd = signed(Wb) * signed(Ws)	1	1	None
		`MULW.SU  Wb,Ws,Wnd`	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		`MULW.US  Wb,Ws,Wnd`	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		`MULW.UU  Wb,Ws,Wnd`	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		`MUL.SU  Wb,#lit5,Wnd`	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		`MUL.SU  Wb,#lit5,Wnd`	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		`MUL.UU  Wb,#lit5,Wnd`	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		`MUL.UU  Wb,#lit5,Wnd`	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		`MUL  f`	W3:W2 = f * WREG	1	1	None
54	`NEG`	`NEG  Acc`	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		`NEG  f`	f = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		`NEG  f,WREG`	WREG = $\overline{f}$ + 1	1	1	C,DC,N,OV,Z
		`NEG  Ws,Wd`	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
55	`NOP`	`NOP`	No Operation	1	1	None
		`NOPR`	No Operation	1	1	None
56	`POP`	`POP  f`	Pop f from Top-of-Stack (TOS)	1	1	None
		`POP  Wdo`	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		`POP.D  Wnd`	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		`POP.S`	Pop Shadow Registers	1	1	All
57	`PUSH`	`PUSH  f`	Push f to Top-of-Stack (TOS)	1	1	None
		`PUSH  Wso`	Push Wso to Top-of-Stack (TOS)	1	1	None
		`PUSH.D  Wns`	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		`PUSH.S`	Push Shadow Registers	1	1	None
58	`PWRSAV`	`PWRSAV  #lit1`	Go into Sleep or Idle mode	1	1	WDTO,Sleep
59	`RCALL`	`RCALL  Expr`	Relative Call	1	4	SFA
		`RCALL  Wn`	Computed Call	1	4	SFA
60	`REPEAT`	`REPEAT  #lit15`	Repeat Next Instruction lit15 + 1 times	1	1	None
		`REPEAT  Wn`	Repeat Next Instruction (Wn) + 1 times	1	1	None
61	`RESET`	`RESET`	Software device Reset	1	1	None
62	`RETFIE`	`RETFIE`	Return from interrupt	1	6 (5)	SFA

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 30-22: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



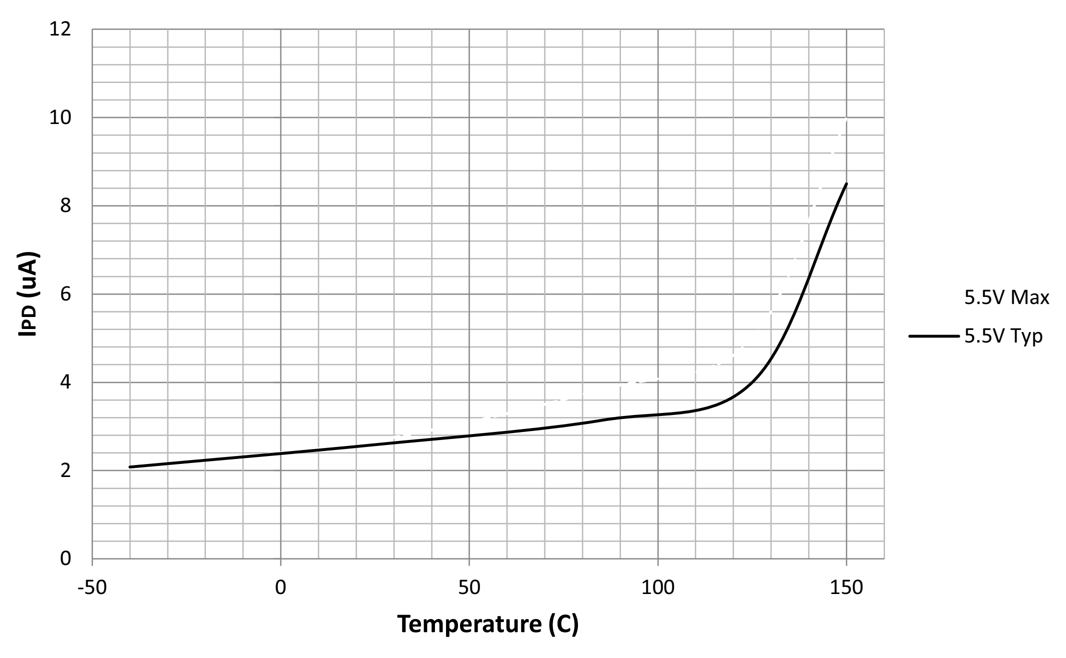
Note: Refer to Figure 30-1 for load conditions.

TABLE 30-40: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**$^{(1)}$	**Min.**	**Typ.**$^{(2)}$	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	

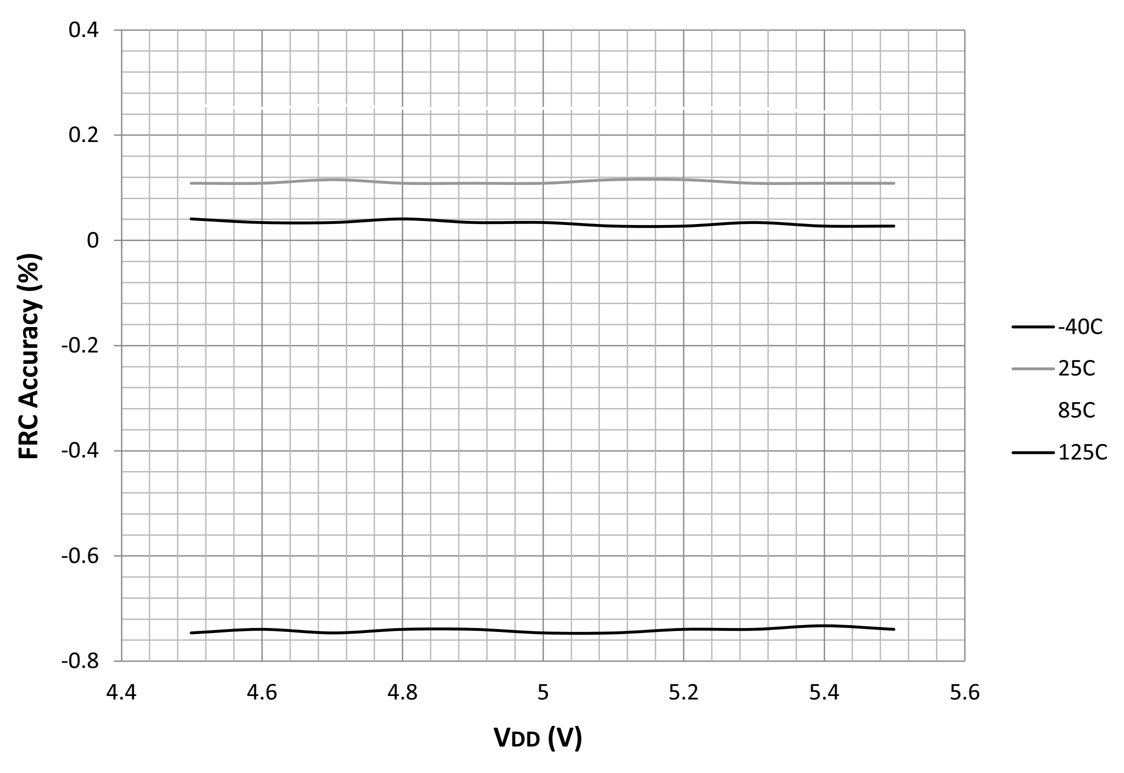
Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.
3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

FIGURE 32-19: TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE



32.5 FRC

FIGURE 32-20: TYPICAL FRC ACCURACY vs. VDD



32.8 Pull-up and Pull-Down Current

FIGURE 32-27: TYPICAL PULL-UP CURRENT ($V_{PIN} = V_{SS}$) vs. TEMPERATURE

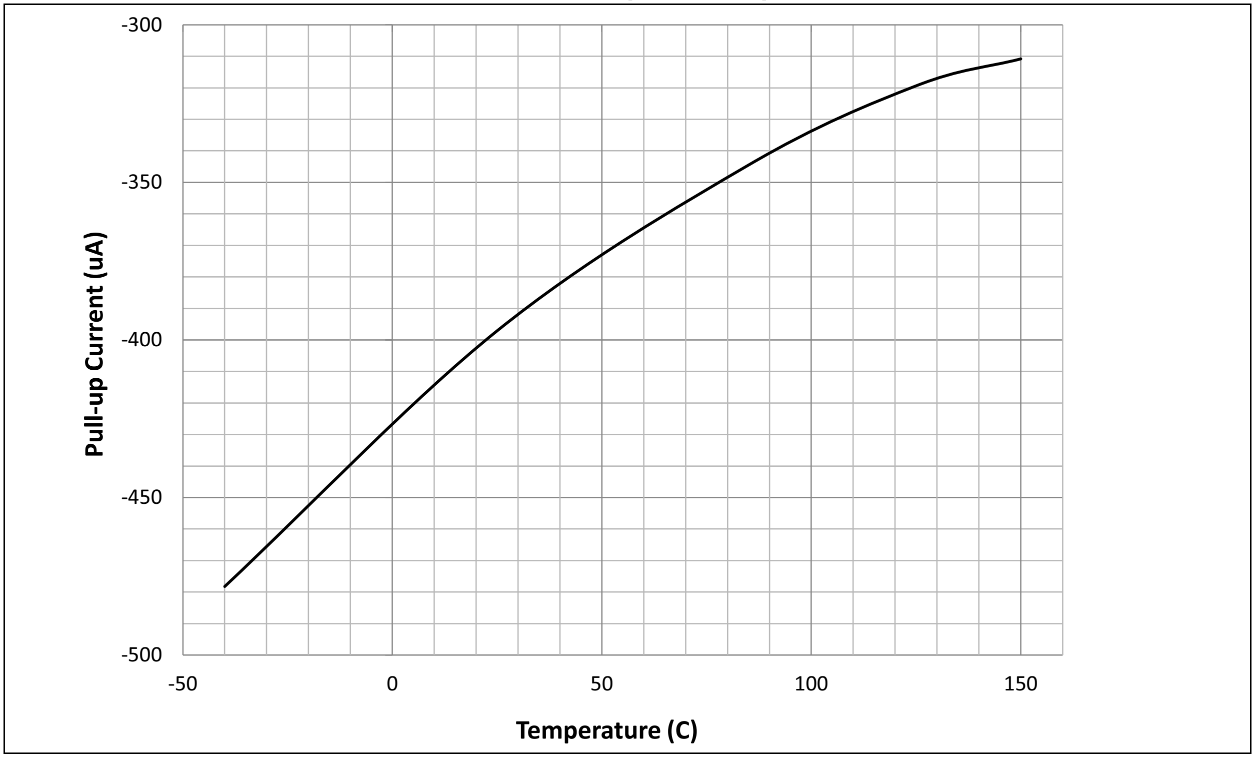


FIGURE 32-28: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE

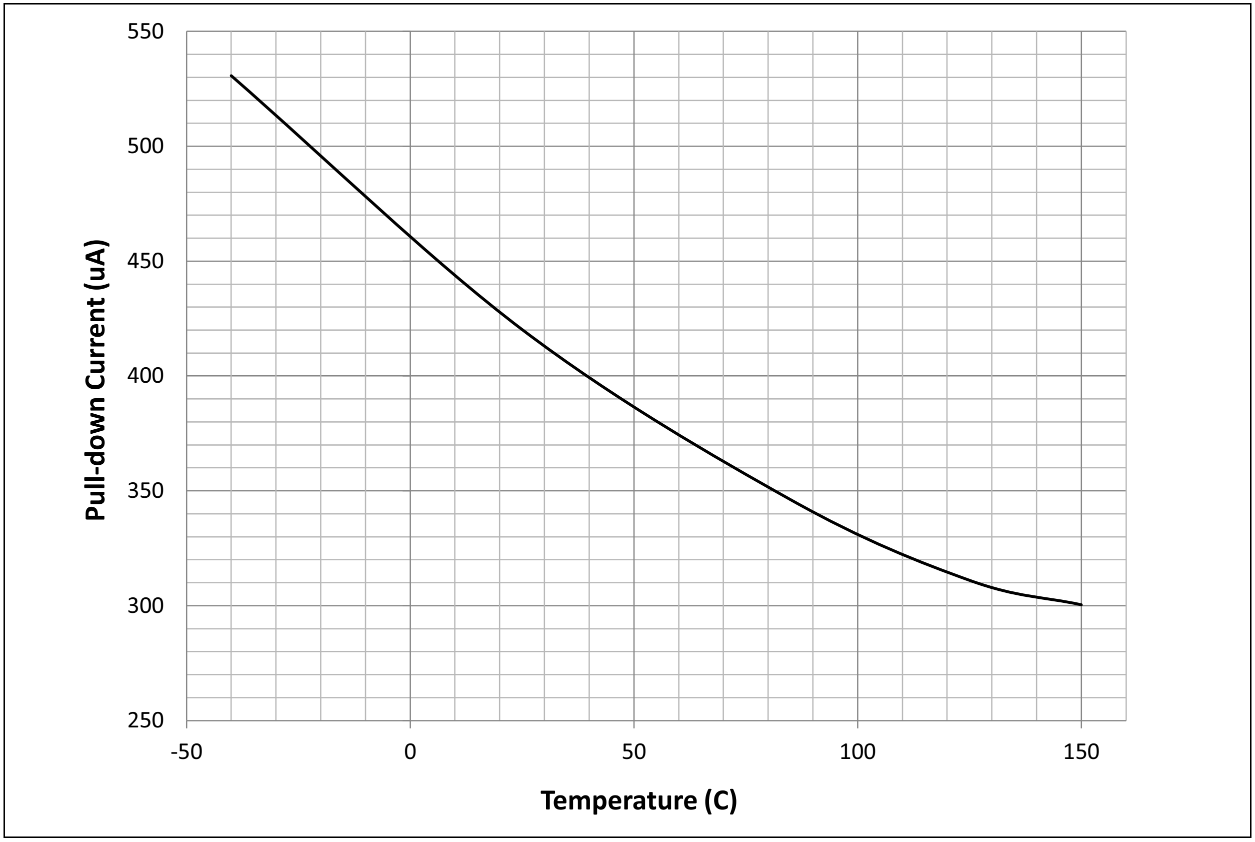


FIGURE 32-47: TYPICAL INL (VDD = 5.5V, +85°C)

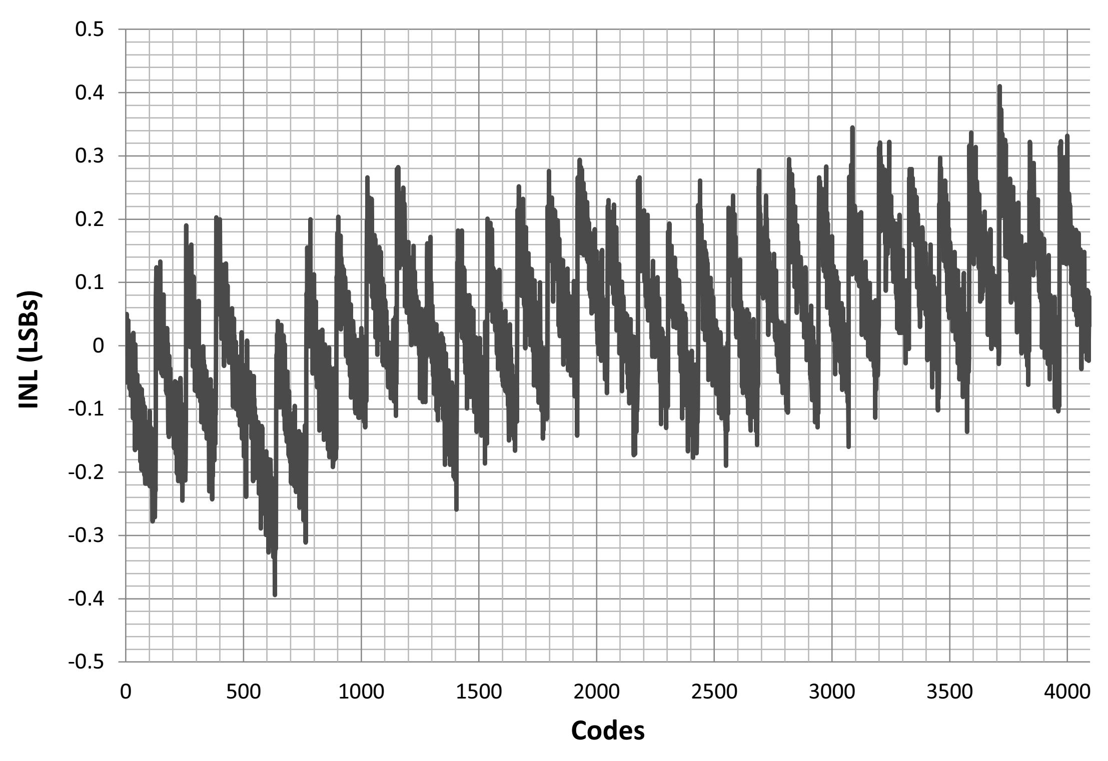


FIGURE 32-48: TYPICAL INL (VDD = 5.5V, +125°C)

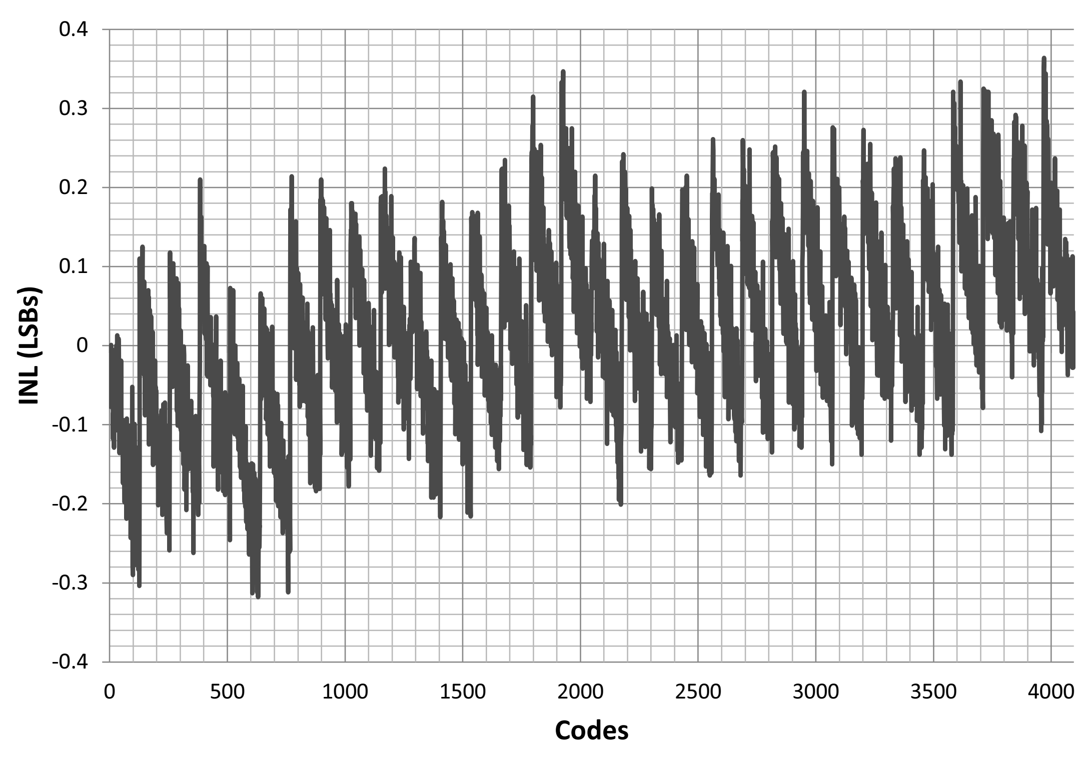
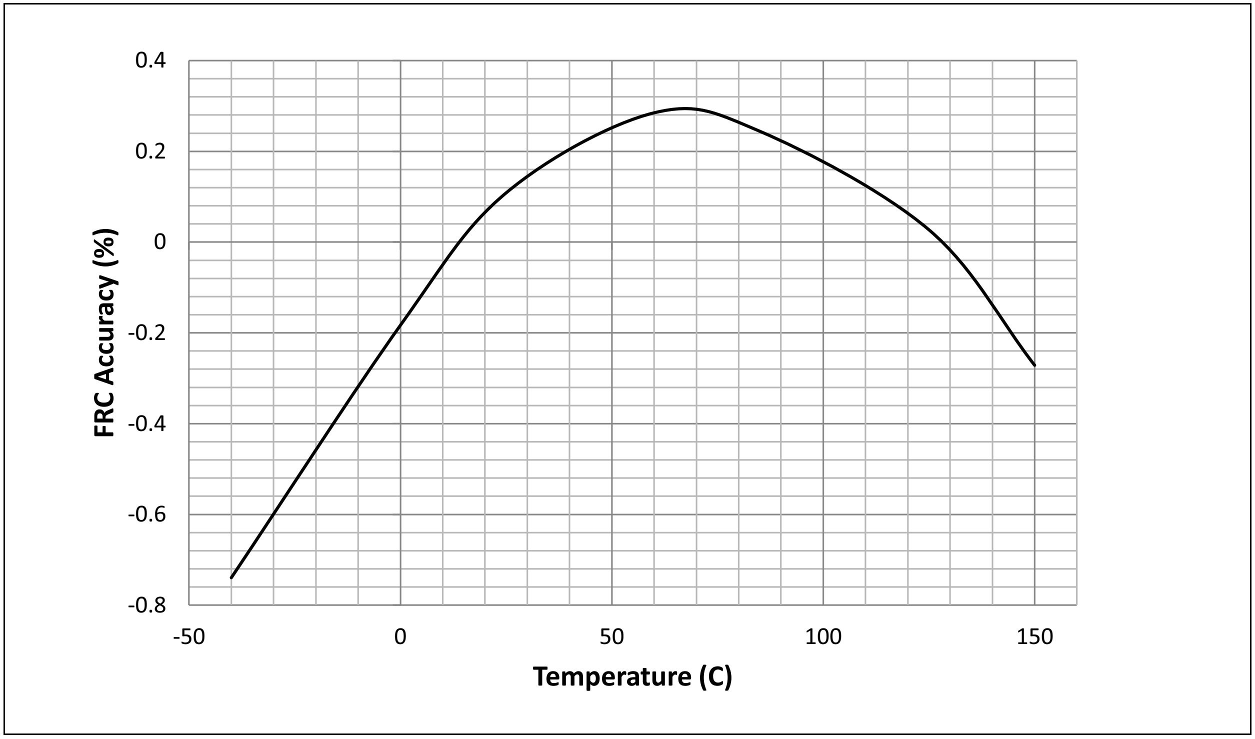
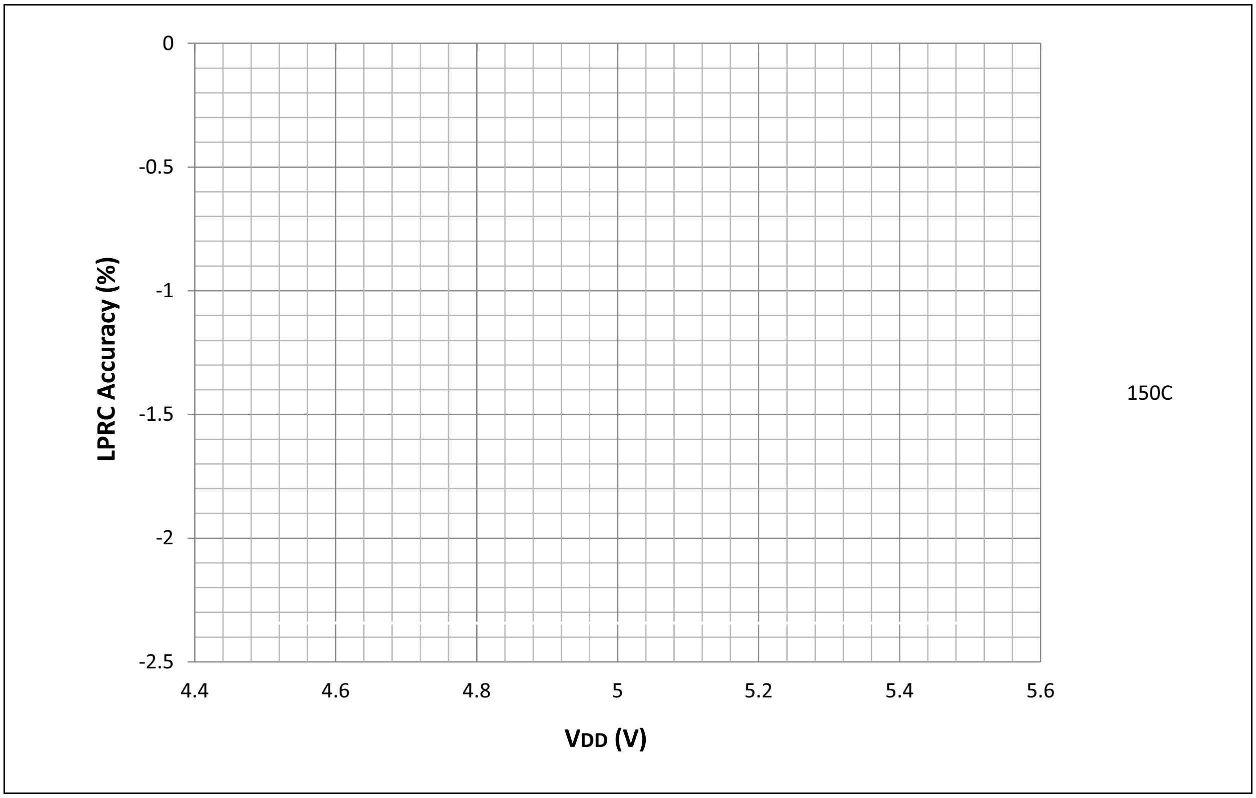


FIGURE 33-17: TYPICAL FRC ACCURACY vs. TEMPERATURE (5.5V VDD)



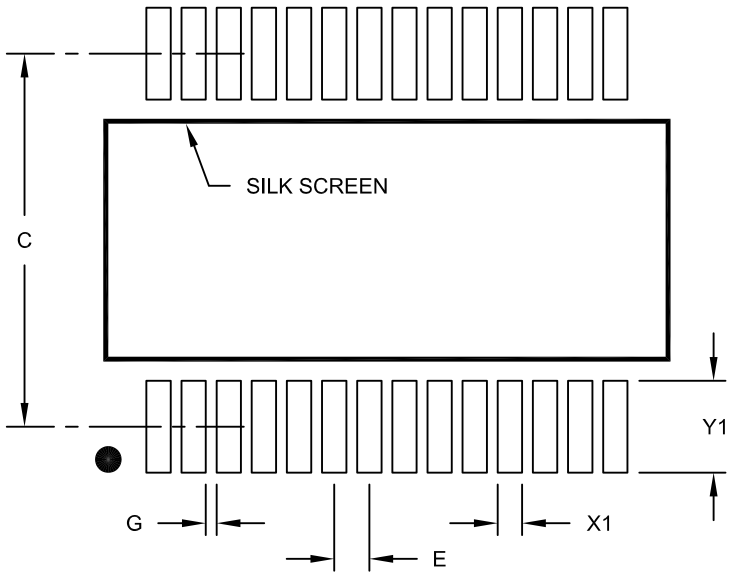
33.6 LPRC

FIGURE 33-18: TYPICAL LPRC ACCURACY vs. VDD



28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

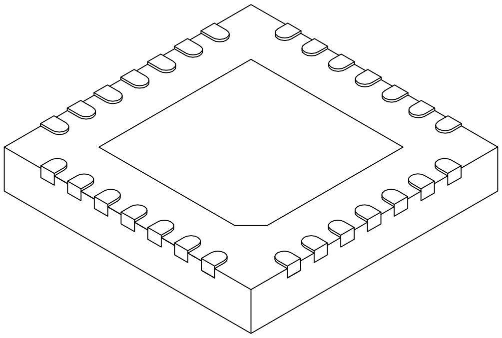
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2