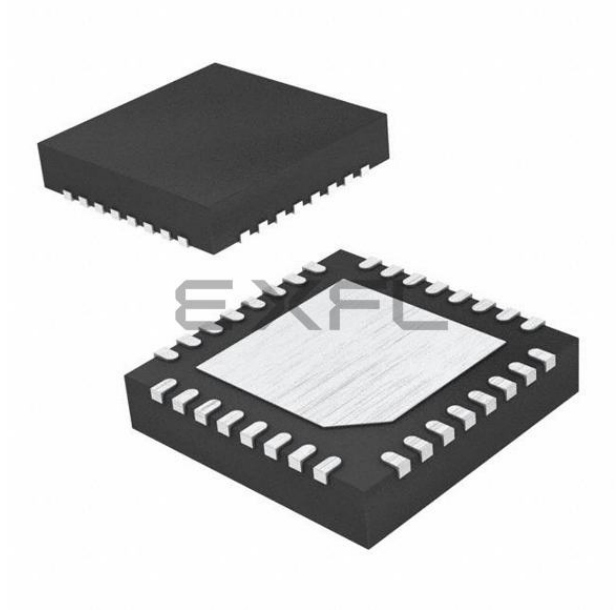
Microchip Technology - DSPIC33EV32GM102T-I/MM Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm102t-i-mm

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output
Analog = Analog input
P = Power
ST = Schmitt Trigger input with CMOS levels
O = Output
I = Input
PPS = Peripheral Pin Select
TTL = TTL input buffer

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the REFCLK pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep mode
0 = Reference oscillator output is disabled in Sleep mode

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP39R<5:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP38R<5:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R<5:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R<5:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = Reserved
11110 = Reserved
11101 = Reserved
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization(5)
11010 = Analog Comparator 3 is the source for the capture timer synchronization(5)
11001 = Analog Comparator 2 is the source for the capture timer synchronization(5)
11000 = Analog Comparator 1 is the source for the capture timer synchronization(5)
10111 = Analog Comparator 5 is the source for the capture timer synchronization(5)
10110 = Analog Comparator 4 is the source for the capture timer synchronization(5)
10101 = Reserved
10100 = Reserved
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = Reserved
01001 = Reserved
01000 = Input Capture 4 is the source for the capture timer synchronization(6)
00111 = Input Capture 3 is the source for the capture timer synchronization(6)
00110 = Input Capture 2 is the source for the capture timer synchronization(6)
00101 = Input Capture 1 is the source for the capture timer synchronization(6)
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Reserved

Note 1: The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own sync or trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, the SPIxTXB bit is full
0 = Transmit has started, the SPIxTXB bit is empty

Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in the hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, the SPIxRXB bit is full
0 = Receive is incomplete, the SPIxRXB bit is empty

Standard Buffer mode:
Automatically set in the hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

19.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit™ (I^2C™)"** (DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains one Inter-Integrated Circuit (I^2C) module, I2C1.

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard, with a 16-bit interface.

The I^2C module has the following 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I^2C module offers the following key features:

- I^2C Interface Supporting Both Master and Slave modes of Operation
- I^2C Slave mode Supports 7 and 10-Bit Addressing
- I^2C Master mode Supports 7 and 10-Bit Addressing
- I^2C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I^2C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- Support for Address Bit Masking up to Lower 7 Bits
- I^2C Slave Enhancements:
  - SDAx hold time selection of SMBus (300 ns or 150 ns)
  - Start/Stop bit interrupt enables

Figure 19-1 shows a block diagram of the I^2C module.

19.1 I^2C Baud Rate Generator

The Baud Rate Generator (BRG) used for I^2C mode operation is used to set the SCL clock frequency for 100 kHz, 400 kHz and 1 MHz. The BRG reload value is contained in the I2CxBRG register. The BRG will automatically begin counting on a write to the I2CxTRN register.

Equation 19-1 and Equation 19-2 provide the BRG reload formula and FSCL frequency, respectively.

EQUATION 19-1: BRG FORMULA

$$I2CxBRG = \left(\left(\frac{1}{F_{SCL}} - Delay\right) \times \frac{F_{CY}}{2}\right) - 2$$

Where:

Delay varies from 110 ns to 130 ns.

EQUATION 19-2: FSCL FREQUENCY

$$F_{SCL} = F_{CY}/((I2CxBRG + 2) * 2)$$

21.2 UART Control Registers

REGISTER 21-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN(1)	—	USIDL	IREN(2)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
- 0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when the device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(3)
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used(4)
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(4)
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLKx pins are controlled by PORT latches

bit 7 **WAKE:** UARTx Wake-up on Start bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
- 0 = Wake-up is not enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This feature is only available on 44-pin and 64-pin devices.

4: This feature is only available on 64-pin devices.

REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits 7-0, controls Buffer n.

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer, TRBm, is a transmit buffer
0 = Buffer, TRBm, is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI<1:0>:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQm is set.

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

REGISTER 24-3: ADxCON3: ADCx CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4(1)	SAMC3(1)	SAMC2(1)	SAMC1(1)	SAMC0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7(2)	ADCS6(2)	ADCS5(2)	ADCS4(2)	ADCS3(2)	ADCS2(2)	ADCS1(2)	ADCS0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** ADCx Conversion Clock Source bit
1 = ADCx internal RC clock
0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC<4:0>:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS<7:0>:** ADCx Conversion Clock Select bits(2)
11111111 = TP • (ADCS<7:0> + 1) = TP • 256 = TAD
•
•
•
00000010 = TP • (ADCS<7:0> + 1) = TP • 3 = TAD
00000001 = TP • (ADCS<7:0> + 1) = TP • 2 = TAD
00000000 = TP • (ADCS<7:0> + 1) = TP • 1 = TAD

Note 1: These bits are only used if SSRC<2:0> (ADxCON1<7:5>) = 111 and SSRCG (ADxCON1<4>) = 0.
2: These bits are not used if ADRC (ADxCON3<15>) = 1.

REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	CH0SB5(1,3)	CH0SB4(1,3)	CH0SB3(1,3)	CH0SB2(1,3)	CH0SB1(1,3)	CH0SB0(1,3)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	CH0SA5(1,3)	CH0SA4(1,3)	CH0SA3(1,3)	CH0SA2(1,3)	CH0SA1(1,3)	CH0SA0(1,3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUX B bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CH0SB<5:0>:** Channel 0 Positive Input Select for Sample MUX B bits(1,3)
111111 = Channel 0 positive input is AN63
111110 = Channel 0 positive input is AN62
111101 = Channel 0 positive input is AN61 (internal band gap voltage)
•
•
•
011111 = Channel 0 positive input is AN31
011110 = Channel 0 positive input is AN30
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 (Op Amp 2)(2)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUX A bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6 **Unimplemented:** Read as '0'

Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R-0
CON	COE	CPOL	—	—	OPAEN(2)	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(3)	EVPOL0(3)	—	CREF(1)	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Op Amp/Comparator x Enable bit
1 = Op Amp/Comparator x is enabled
0 = Op Amp/Comparator x is disabled

bit 14 **COE:** Comparator x Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator x Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPAEN:** Op Amp x Enable bit(2)
1 = Op Amp x is enabled
0 = Op Amp x is disabled

bit 9 **CEVT:** Comparator x Event bit
1 = Comparator event, according to EVPOL<1:0> settings, occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator x Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

Note 1: Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

2: The op amp and the comparator can be used simultaneously in these devices. The OPAEN bit only enables the op amp while the comparator is still functional.

3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator x Event bit, CEVT (CMxCON<9>), and the Comparator Interrupt Flag, CMPIF (IFS1<2>), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EVXXXGM00X/10X family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.0V
Voltage on V_{CAP} with respect to V_{SS} ..... 1.62V to 1.98V
Maximum current out of V_{SS} pin ..... 350 mA
Maximum current into V_{DD} pin(2) ..... 350 mA
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sourced/sunk by all ports(2) ..... 200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI10	VIL	**Input Low Voltage** I/O Pins	VSS	—	0.2 VDD	V	
DI20	VIH	**Input High Voltage** I/O Pins	0.75 VDD	—	5.5	V	
DI30	ICNPU	**Change Notification Pull-up Current**	200	375	600	μA	VDD = 5.0V, VPIN = VSS
DI31	ICNPD	**Change Notification Pull-Down Current(7)**	175	400	625	μA	VDD = 5.0V, VPIN = VDD
DI50	IIL	**Input Leakage Current(2,3)** I/O Pins	-100	—	100	nA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{\text{MCLR}}$	-700	—	700	nA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	-200	—	200	nA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI60a	IICL	**Input Low Injection Current**	0	—	-5(4,6)		All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(5,6)	mA	All pins except VDD, VSS, AVDD, AVSS, $\overline{\text{MCLR}}$, VCAP, RB7 and all 5V tolerant pins(5)
DI60c	∑IICT	**Total Input Injection Current** (sum of all I/O and control pins)	-20(7)	—	+20(7)		Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL |+ | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

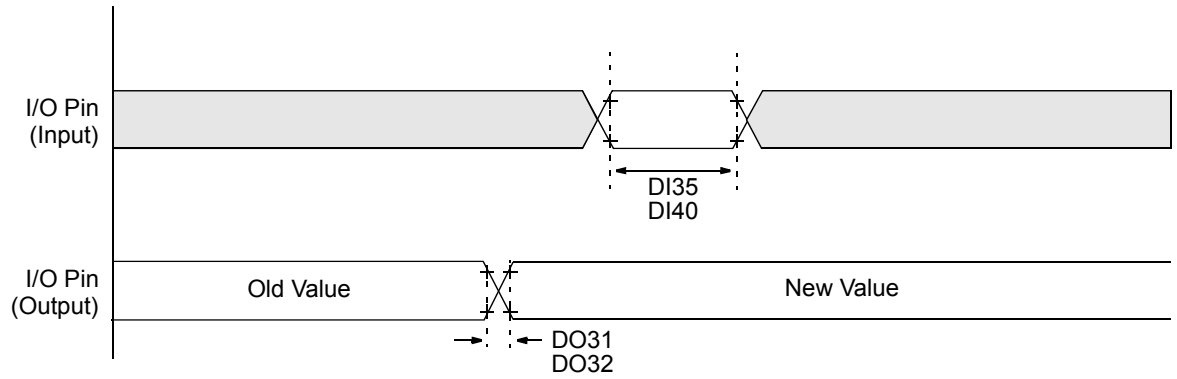
4: VIL source < (VSS – 0.3). Characterized but not tested.

5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

6: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-3: I/O TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS

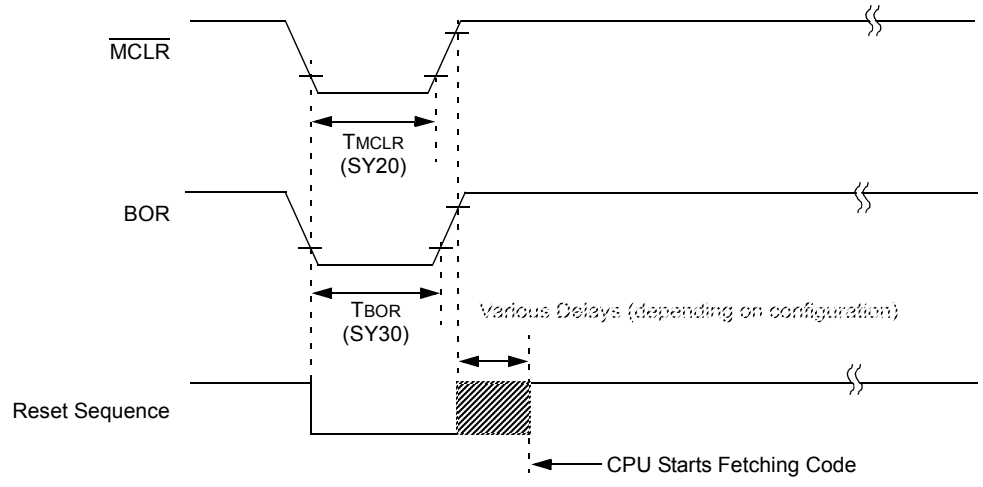
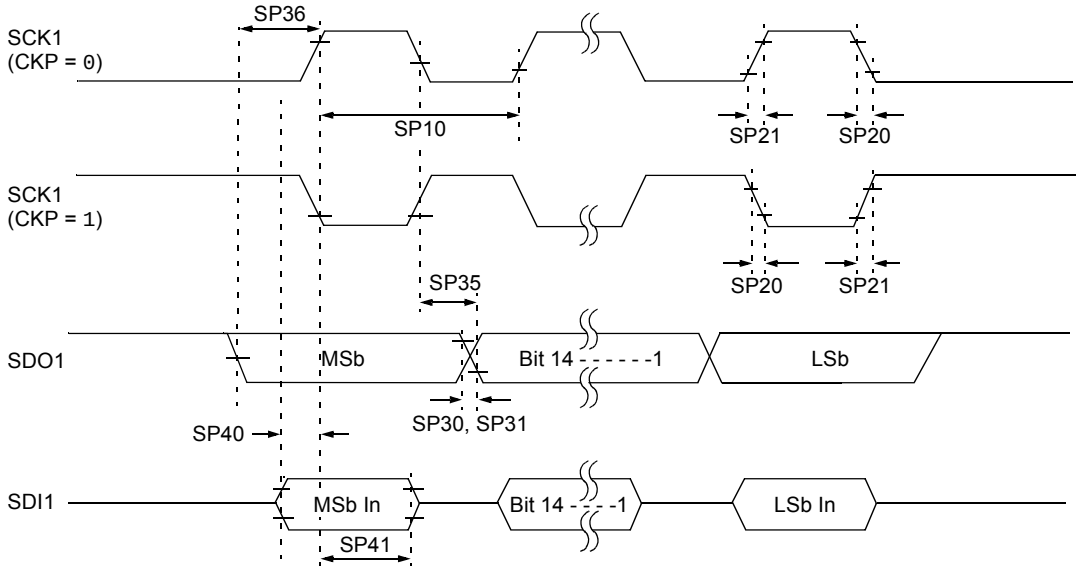


FIGURE 30-22: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-40: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	

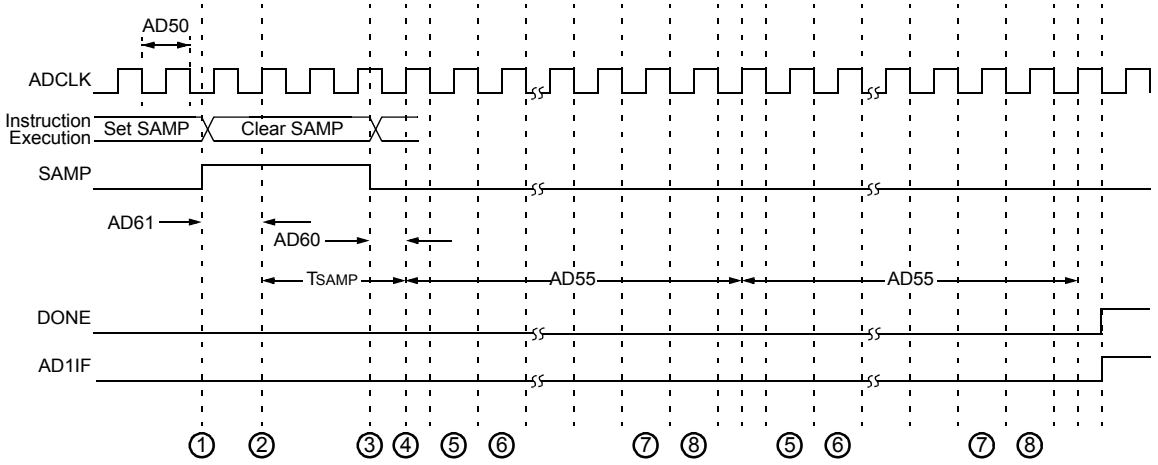
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-35: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)



① – Software sets ADxCON1. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Software clears ADxCON1. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

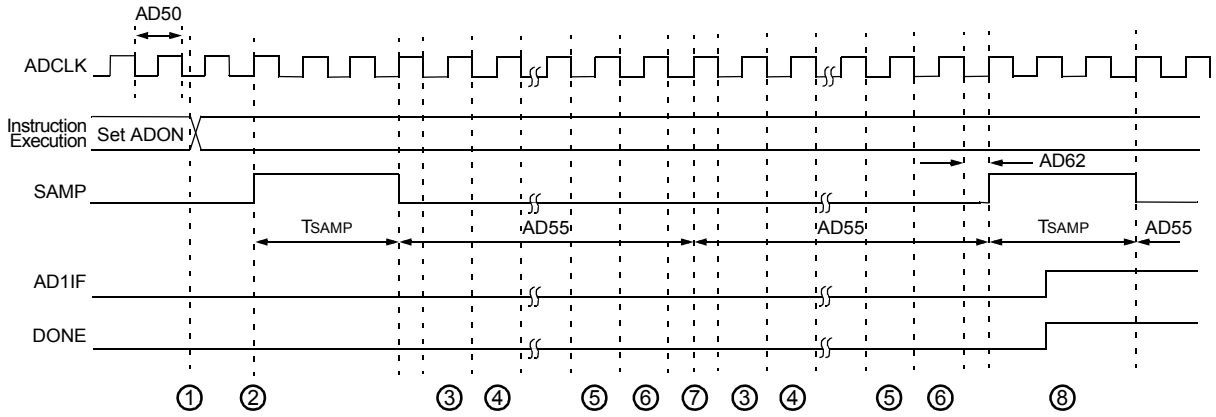
⑤ – Convert bit 9.

⑥ – Convert bit 8.

⑦ – Convert bit 0.

⑧ – One TAD for end of conversion.

FIGURE 30-36: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010)



① – Software sets ADxCON1. ADON to start ADC operation.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Convert bit 9.

④ – Convert bit 8.

⑤ – Convert bit 0.

⑥ – One TAD for end of conversion.

⑦ – Begin conversion of next channel.

⑧ – Sample for time specified by SAMC<4:0>.

32.8 Pull-up and Pull-Down Current

FIGURE 32-27: TYPICAL PULL-UP CURRENT ($V_{PIN} = V_{SS}$) vs. TEMPERATURE

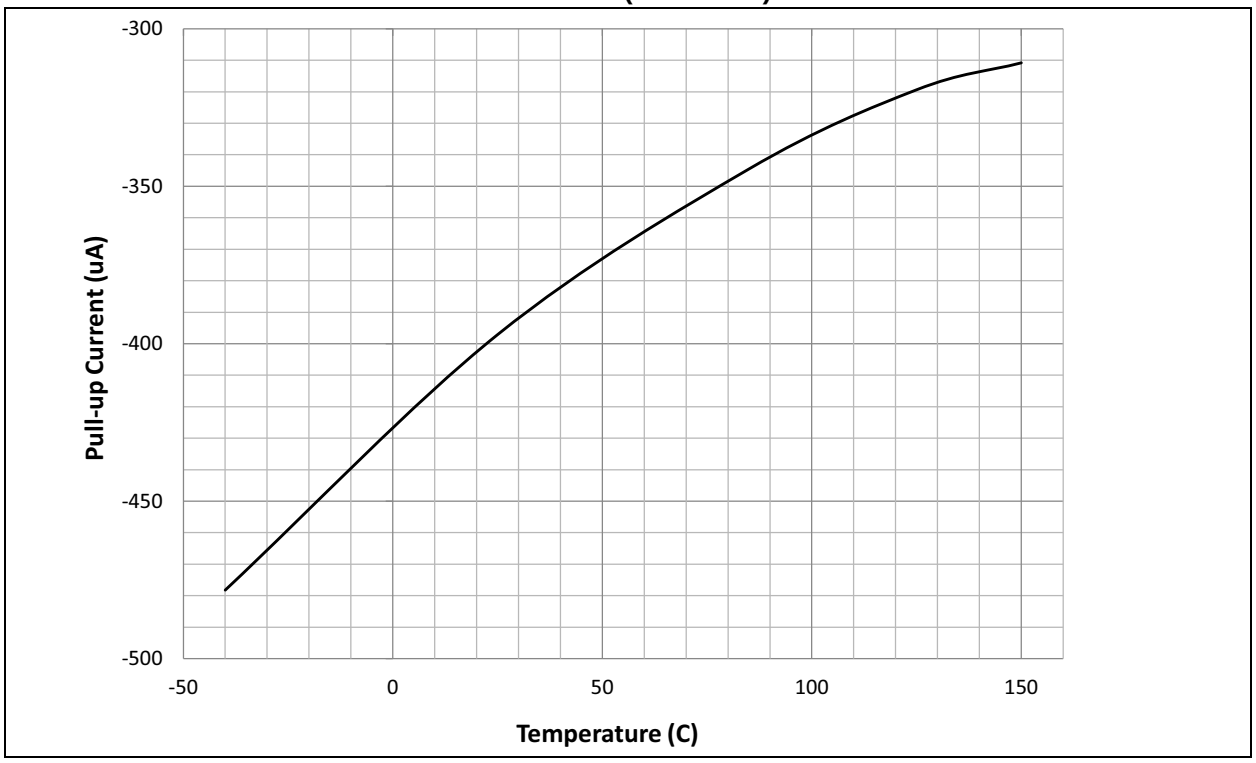
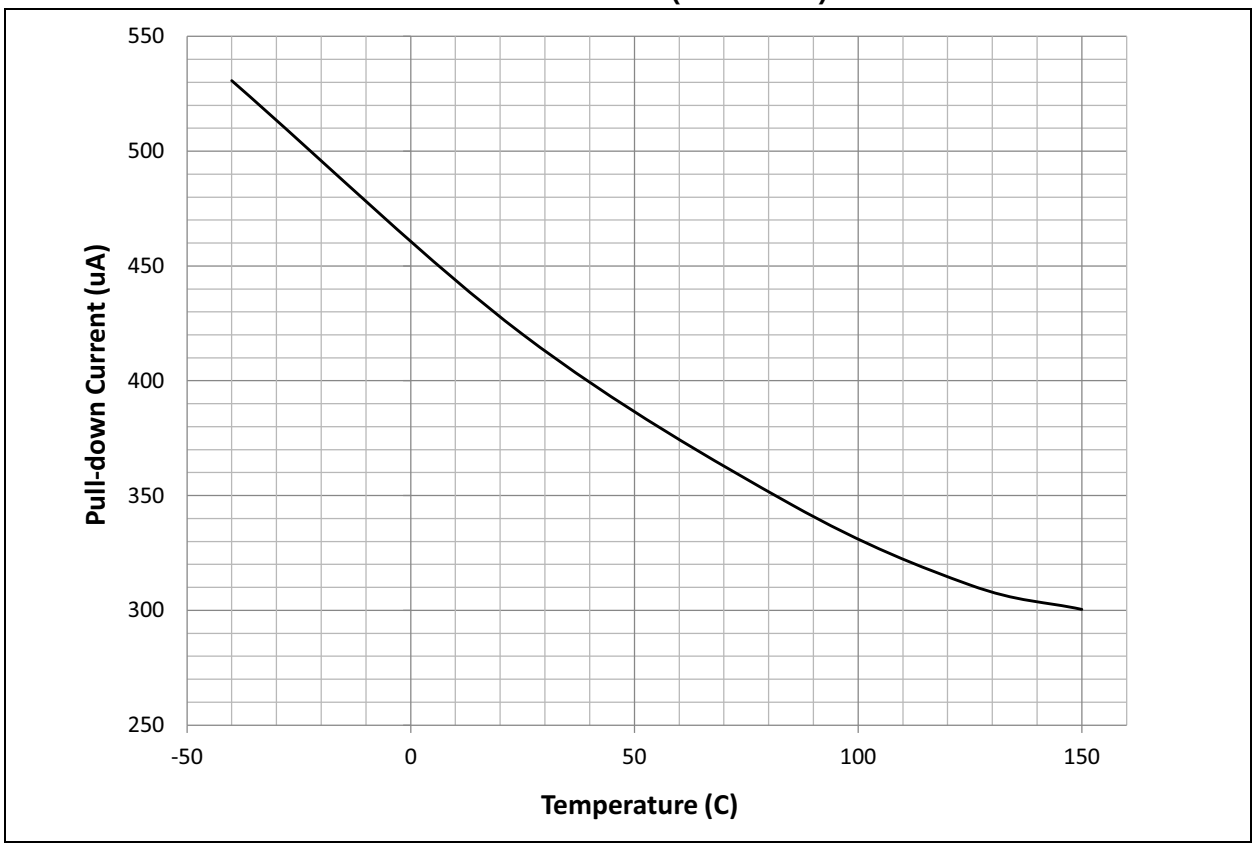


FIGURE 32-28: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE



33.8 Pull-up/Pull-Down Current

FIGURE 33-23: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE

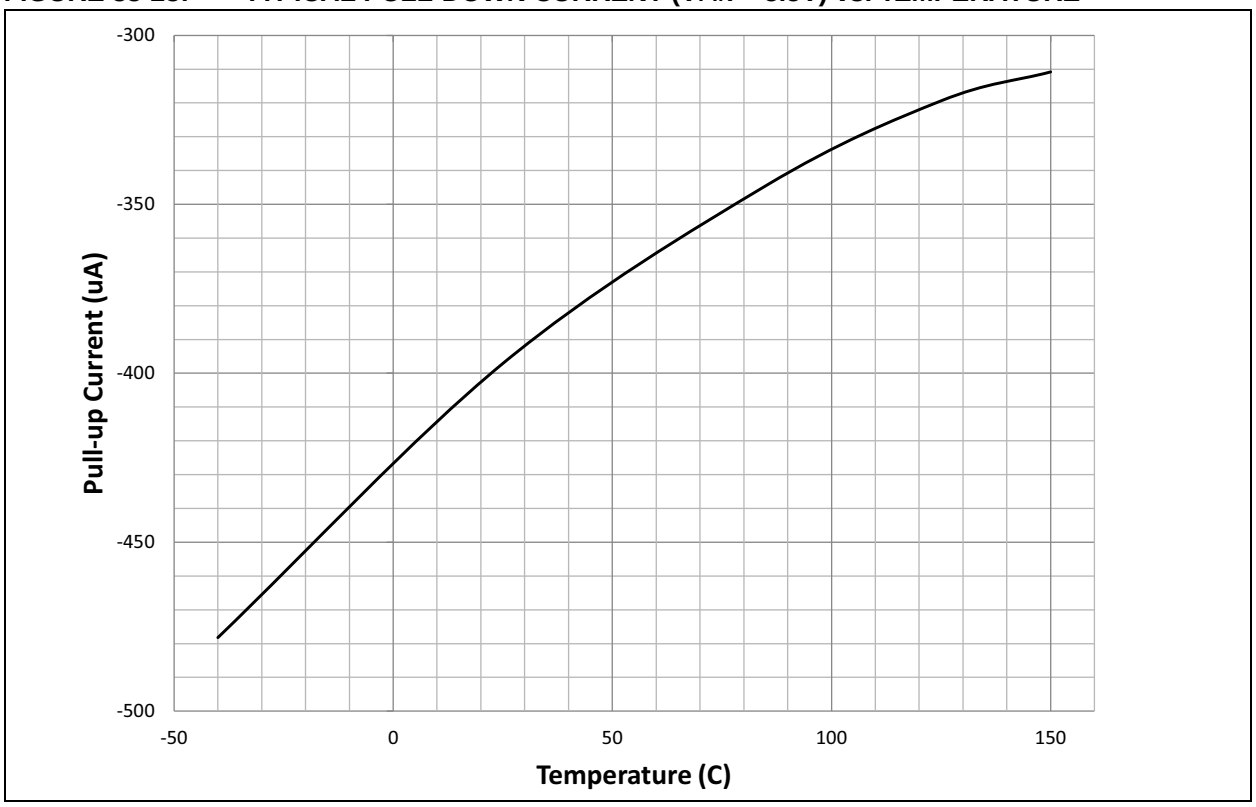
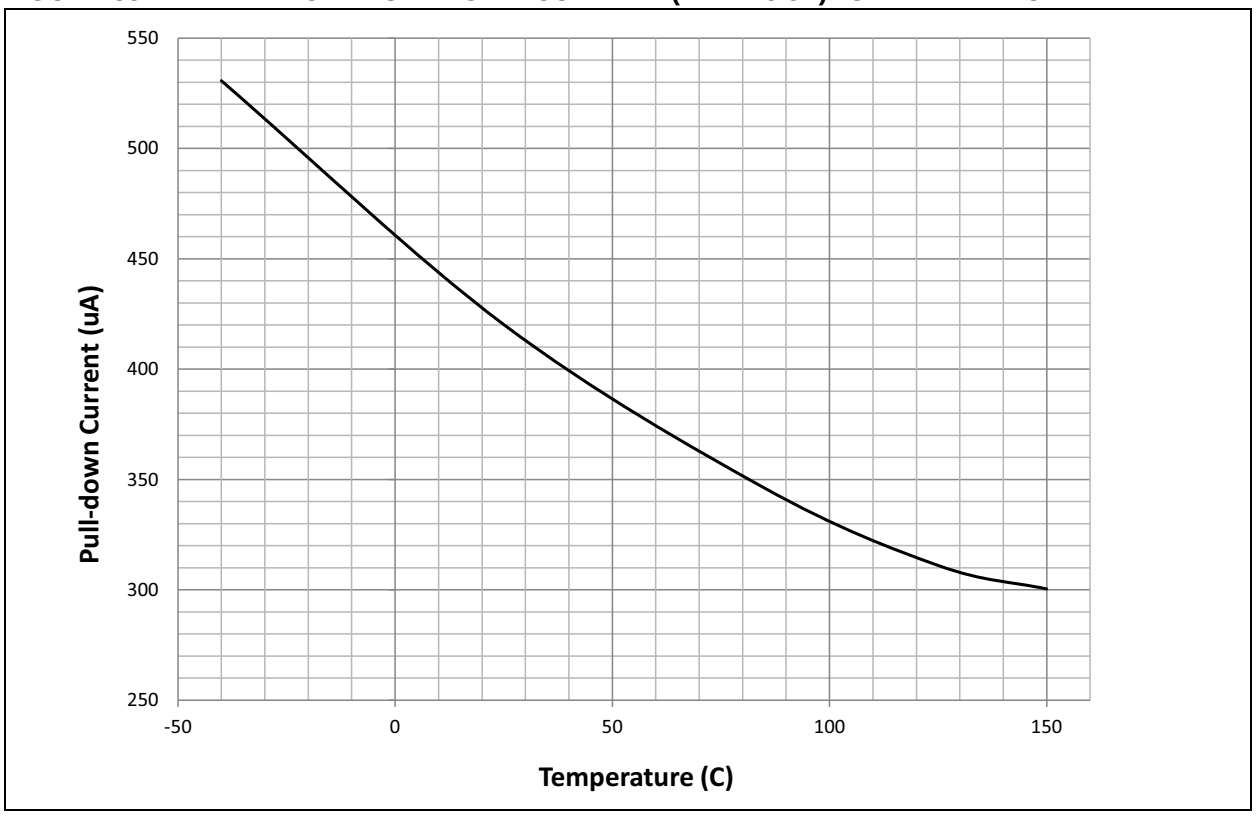


FIGURE 33-24: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE



33.14 Comparator Op Amp Offset

FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. VCM

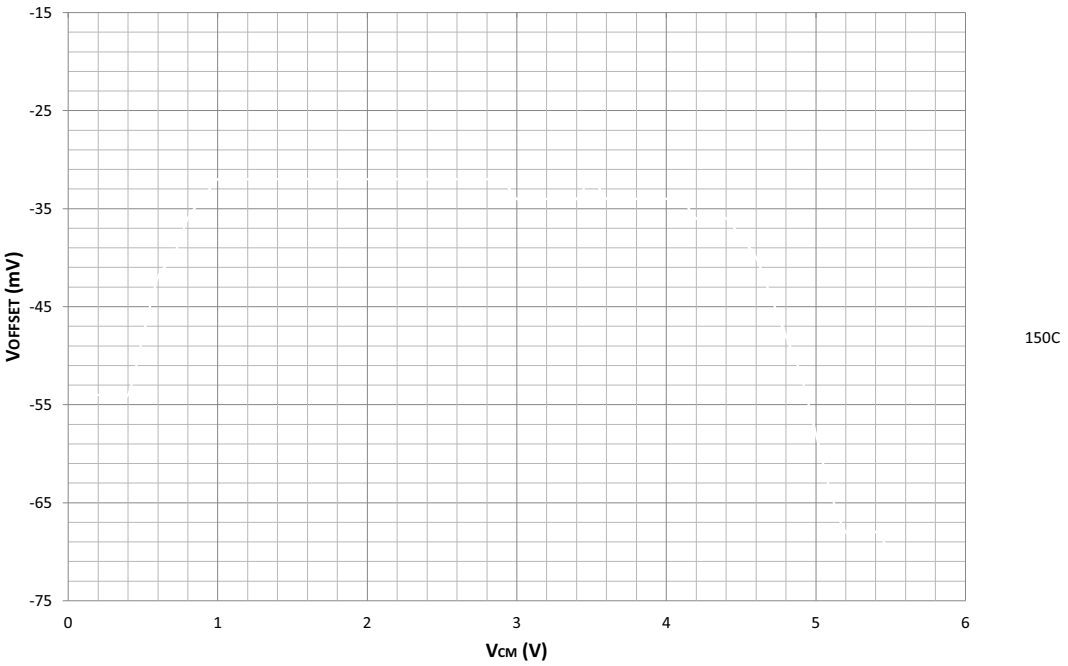
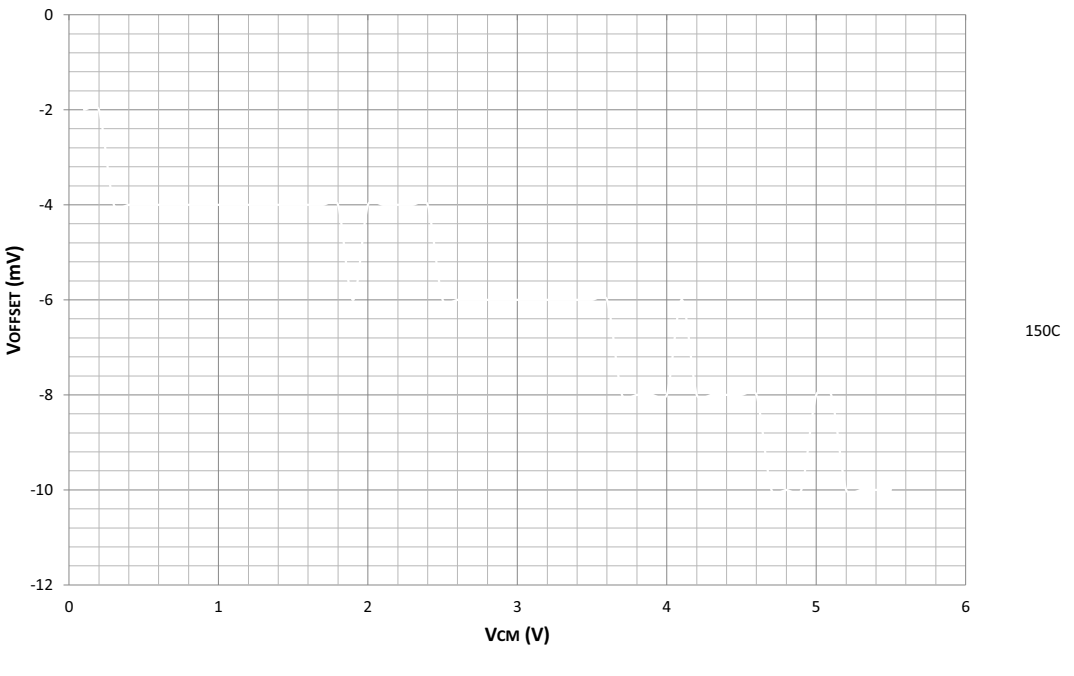
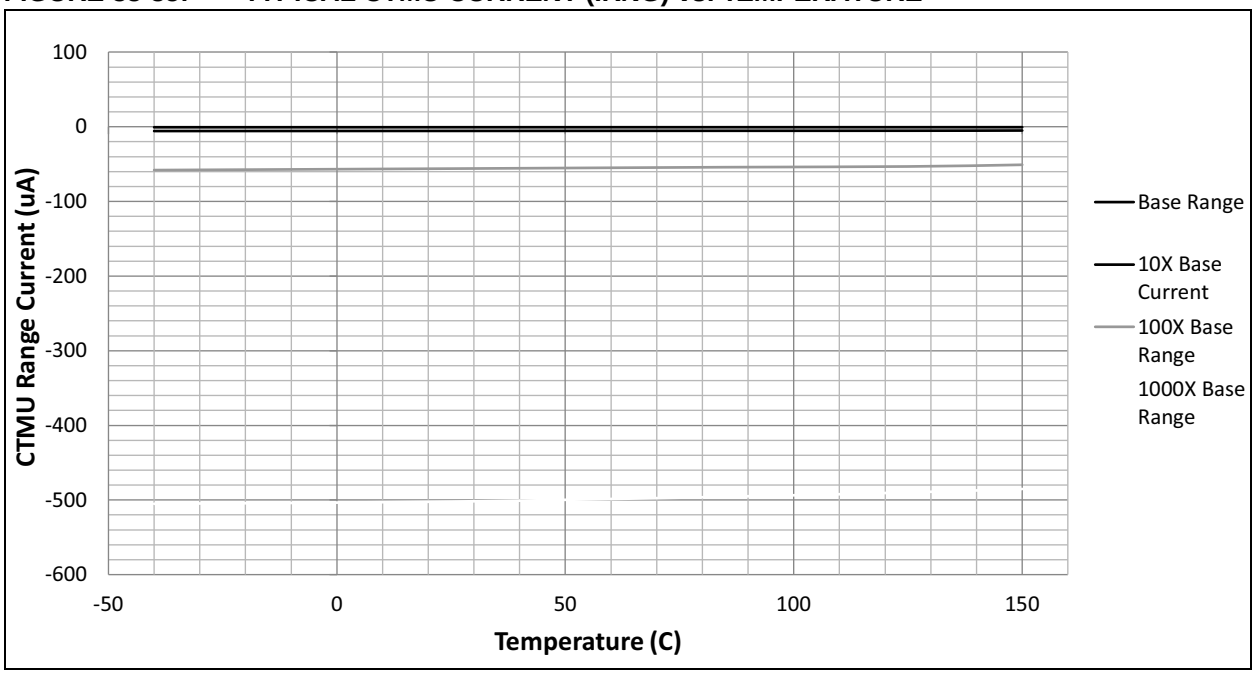


FIGURE 33-34: TYPICAL OP AMP OFFSET vs. VCM



33.15 CTMU Current V/S Temperature

FIGURE 33-35: TYPICAL CTMU CURRENT (IRNG) vs. TEMPERATURE



33.16 CTMU Temperature Forward Diode (V)

FIGURE 33-36: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE vs. TEMPERATURE