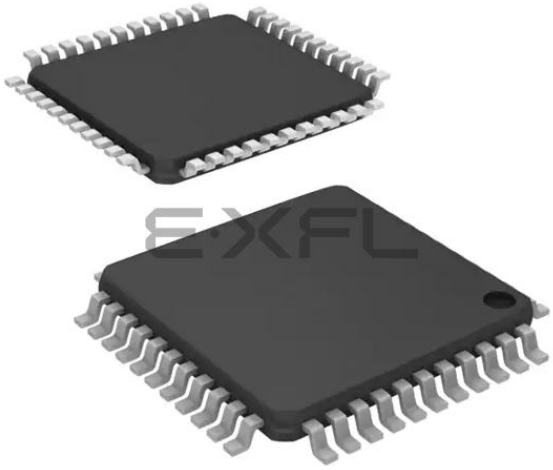
Microchip Technology - DSPIC33EV32GM104-E/PT Datasheet



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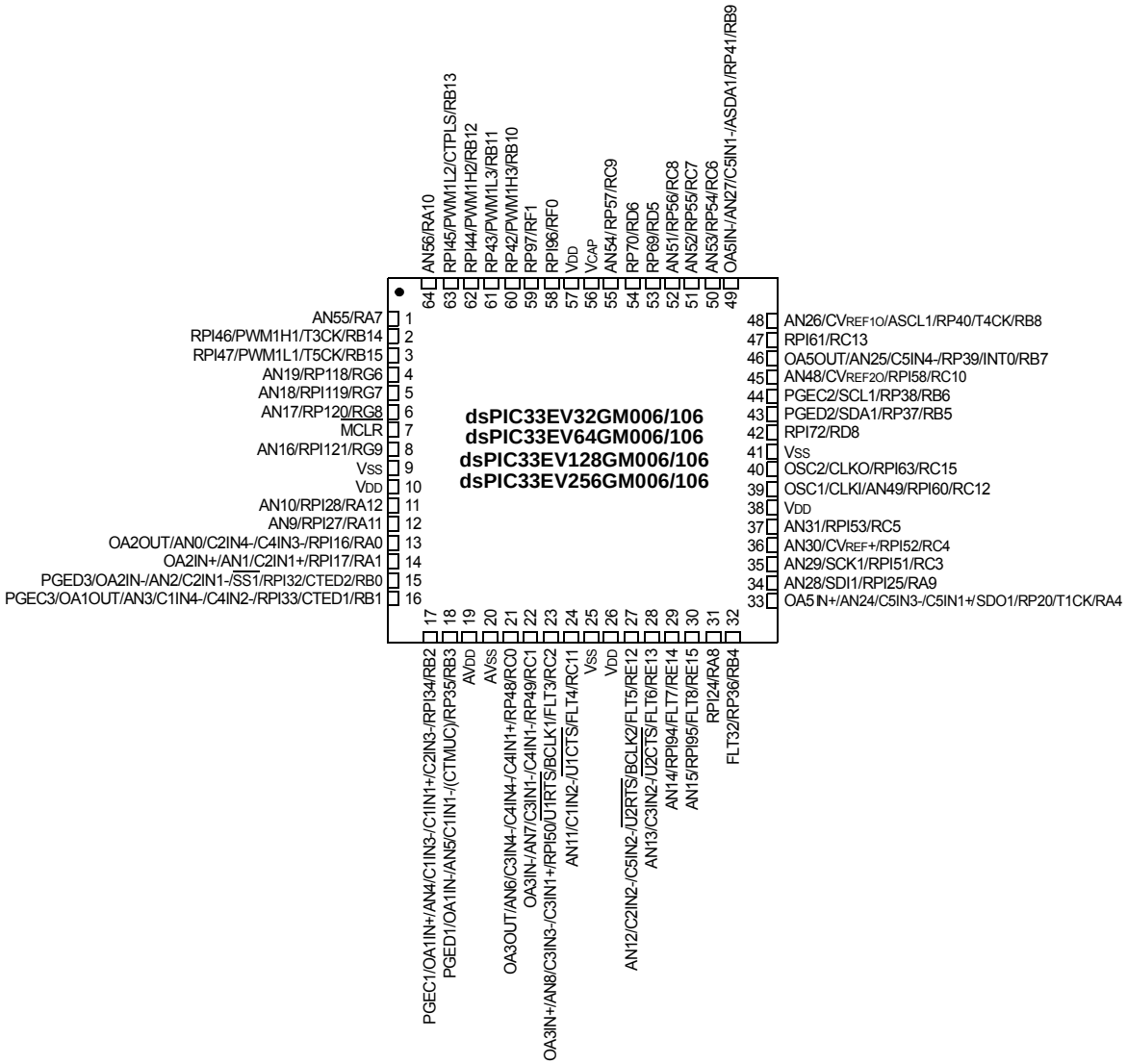
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm104-e-pt

Pin Diagrams (Continued)

64-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
C1RX	I	ST	Yes	CAN1 bus receive pin.
C1TX	O	—	Yes	CAN1 bus transmit pin.
SENT1TX	O	—	Yes	SENT1 transmit pin.
SENT1RX	I	—	Yes	SENT1 receive pin.
SENT2TX	O	—	Yes	SENT2 transmit pin.
SENT2RX	I	—	Yes	SENT2 receive pin.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs.
C1OUT	O	—	Yes	Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3-	I	Analog	No	Comparator 2 inputs.
C2OUT	O	—	Yes	Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3-	I	Analog	No	Comparator 3 inputs.
C3OUT	O	—	Yes	Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3-	I	Analog	No	Comparator 4 inputs.
C4OUT	O	—	Yes	Comparator 4 output.
C5IN1+, C5IN2-, C5IN1-, C5IN3-	I	Analog	No	Comparator 5 inputs.
C5OUT	O	—	Yes	Comparator 5 output.
FLT1-FLT2	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3-FLT8	I	ST	NO	PWM Fault Inputs 3 to 8.
FLT32	I	ST	NO	PWM Fault Input 32.
DTCMP1-DTCMP3	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 to 3.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 to 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 to 3.
SYNCI1	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1	O	—	Yes	PWM Synchronization Output 1.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
MCLR	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EVXXXGM00X/10X CPU. The Interrupt Vector Table (IVT) provides 246 interrupt sources (unused sources are reserved for future use) that can be programmed with different priority levels.

The interrupt controller has the following features:

- Interrupt Vector Table with up to 246 Vectors
- Alternate Interrupt Vector Table (AIVT)
- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Software can Generate any Peripheral Interrupt
- Alternate Interrupt Vector Table (AIVT) is available if Boot Security is Enabled and AIVTEN = 1

7.1 Interrupt Vector Table

The dsPIC33EVXXXGM00X/10X family IVT, shown in Figure 7-2, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 187 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-1, is available if the Boot Segment (BS) is defined, the AIVTEN bit is set in the INTCON2 register and if the AIVTDIS Configuration bit is set to '1'. The AIVT begins at the start of the last page of the Boot Segment.

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB<23:16>:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **STB<15:0>:** DMA Secondary Start Address bits (source or destination)

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the REFCLK pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep mode
0 = Reference oscillator output is disabled in Sleep mode

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

11.5.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one, and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
C1TX	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5
SENT1	111001	RPn tied to SENT Out 1
SENT2	111010	RPn tied to SENT Out 2

REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCFAR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **OCFAR<7:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER(2)

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1(1)	PMOD0(1)	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWMx module controls the PWMxH pin
0 = GPIO module controls the PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWMx module controls the PWMxL pin
0 = GPIO module controls the PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD<1:0>:** PWMx I/O Pin Mode bits(1)
11 = Reserved; do not use
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT1 controls the output on the PWMxH pin
0 = PWMx generator controls the PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT0 controls the output on the PWMxL pin
0 = PWMx generator controls the PWMxL pin

bit 7-6 **OVRDAT<1:0>:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT1.
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT0.

bit 5-4 **FLTDAT<1:0>:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
If Fault is active, PWMxH is driven to the state specified by FLTDAT1.
If Fault is active, PWMxL is driven to the state specified by FLTDAT0.

bit 3-2 **CLDAT<1:0>:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits
If current limit is active, PWMxH is driven to the state specified by CLDAT1.
If current limit is active, PWMxL is driven to the state specified by CLDAT0.

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER(2) (CONTINUED)

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pin; PWMxL output signal is connected to the PWMxH pin
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides through the OVRDAT<1:0> bits are synchronized to the PWMx time base
0 = Output overrides through the OVRDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOPT<0>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TRGCMP<15:0>:** Trigger Control Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

REGISTER 17-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH(1)	BCL(1)	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected Fault input
0 = Leading-Edge Blanking is not applied to the selected Fault input

bit 10 **CLLEBEN:** Current-Limit Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected current-limit input
0 = Leading-Edge Blanking is not applied to the selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when the selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when the selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is high
0 = No blanking when the PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is low
0 = No blanking when the PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
0 = No blanking when the PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
0 = No blanking when the PWMxL output is low

Note 1: The blanking signal is selected through the BLANKSEL<3:0> bits in the AUXCONx register.

REGISTER 22-22: CxRXFUL1: CANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<15:8>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<7:0>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<15:0>:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

REGISTER 22-23: CxRXFUL2: CANx RECEIVE BUFFER FULL REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<31:24>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL<23:16>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL<31:16>:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

TABLE 30-34: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	$\overline{SDO2}$ Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-43: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI10	VIL	**Input Low Voltage** Any I/O Pins	VSS	—	0.2 VDD	V	
DI20	VIH	**Input High Voltage** I/O Pins	0.75 VDD	—	5.5	V	
DI30	ICNPU	**Change Notification Pull-up Current**	200	375	600	μA	VDD = 5.0V, VPIN = VSS
DI31	ICNPD	**Change Notification Pull-Down Current(7)**	175	400	625	μA	VDD = 5.0V, VPIN = VDD
DI50	IIL	**Input Leakage Current(2,3)** I/O Pins	-200	—	200	nA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		MCLR	-1.5	—	1.5	μA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	-300	—	300	nA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI60a	IICL	**Input Low Injection Current**	0	—	-5(4,6)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(5,6)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins(5)
DI60c	∑IICT	**Total Input Injection Current** (sum of all I/O and control pins)	-20(7)	—	+20(7)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL | + | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: VIL source < (VSS – 0.3). Characterized but not tested.

5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

6: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 32-31: TYPICAL V_{OH} 4x DRIVER PINS vs. I_{OH} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

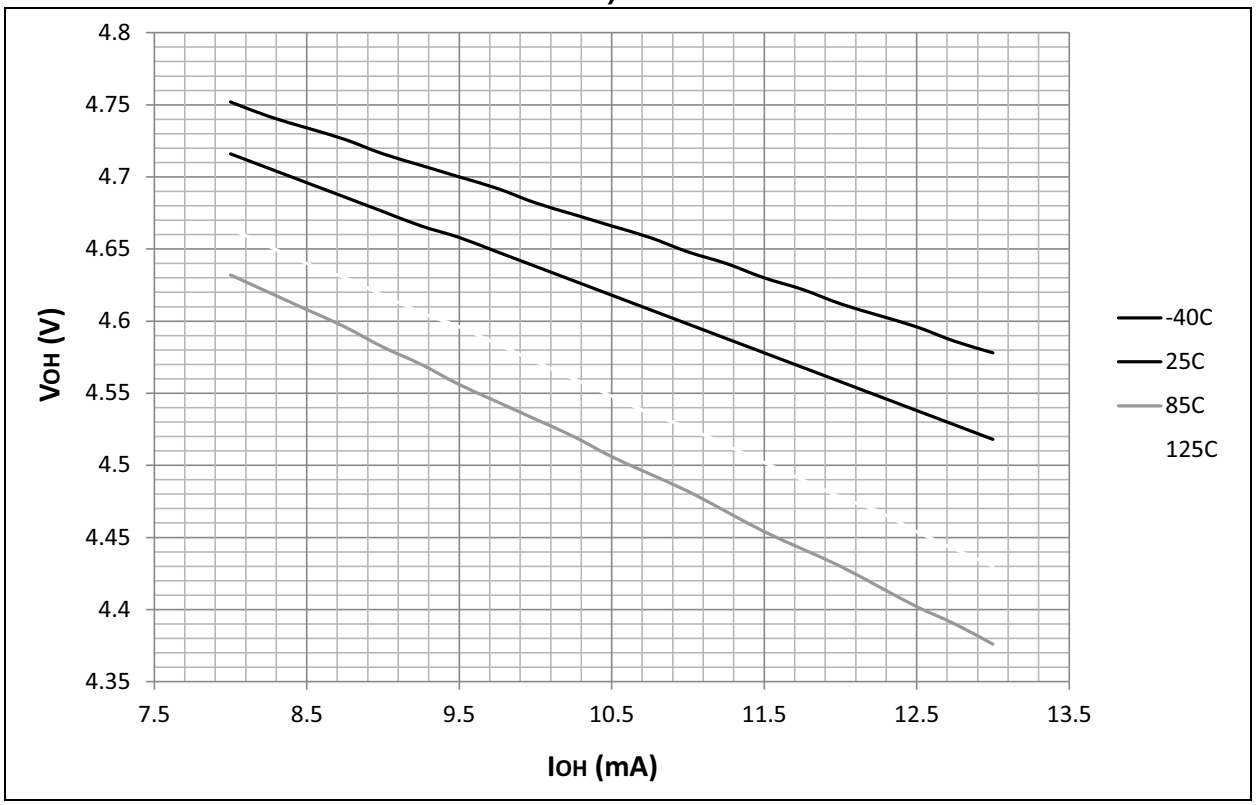


FIGURE 32-32: TYPICAL V_{OL} 8x DRIVER PINS vs. I_{OL} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

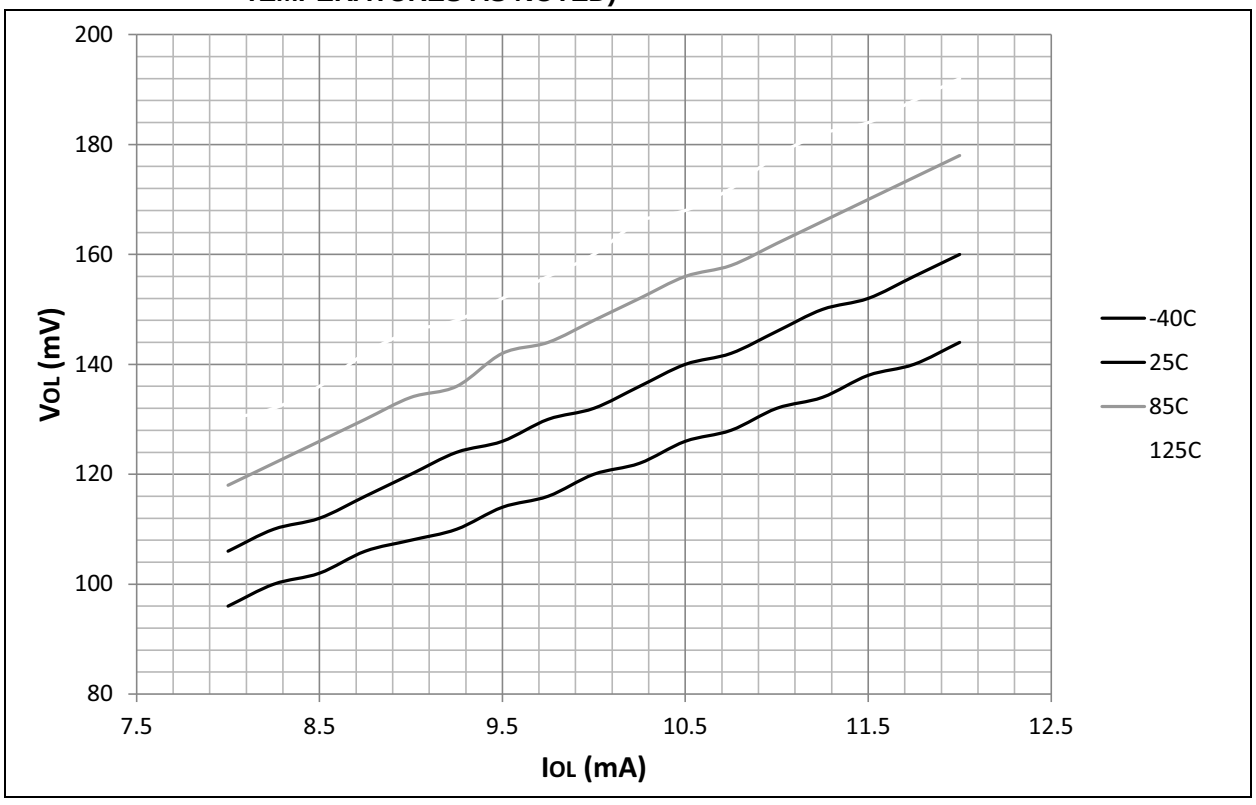
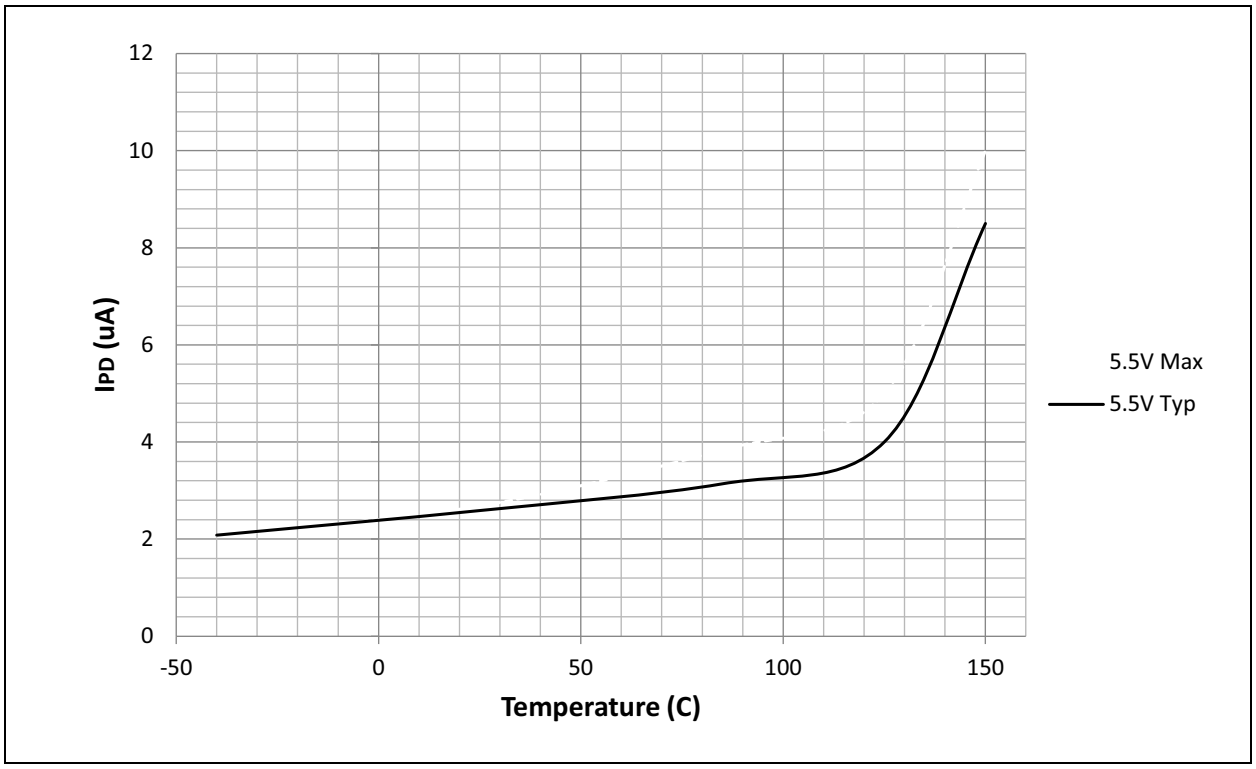


FIGURE 33-15: TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE



33.5 FRC

FIGURE 33-16: TYPICAL FRC ACCURACY vs. VDD

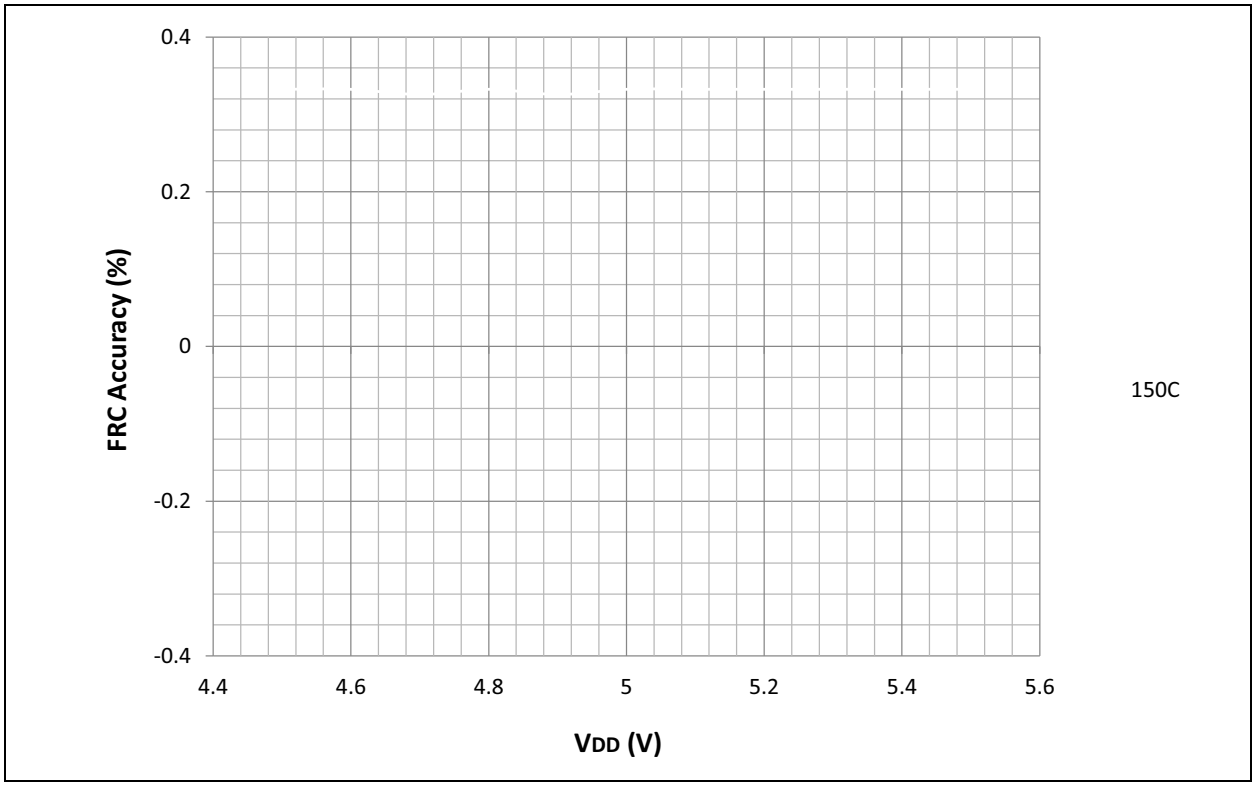
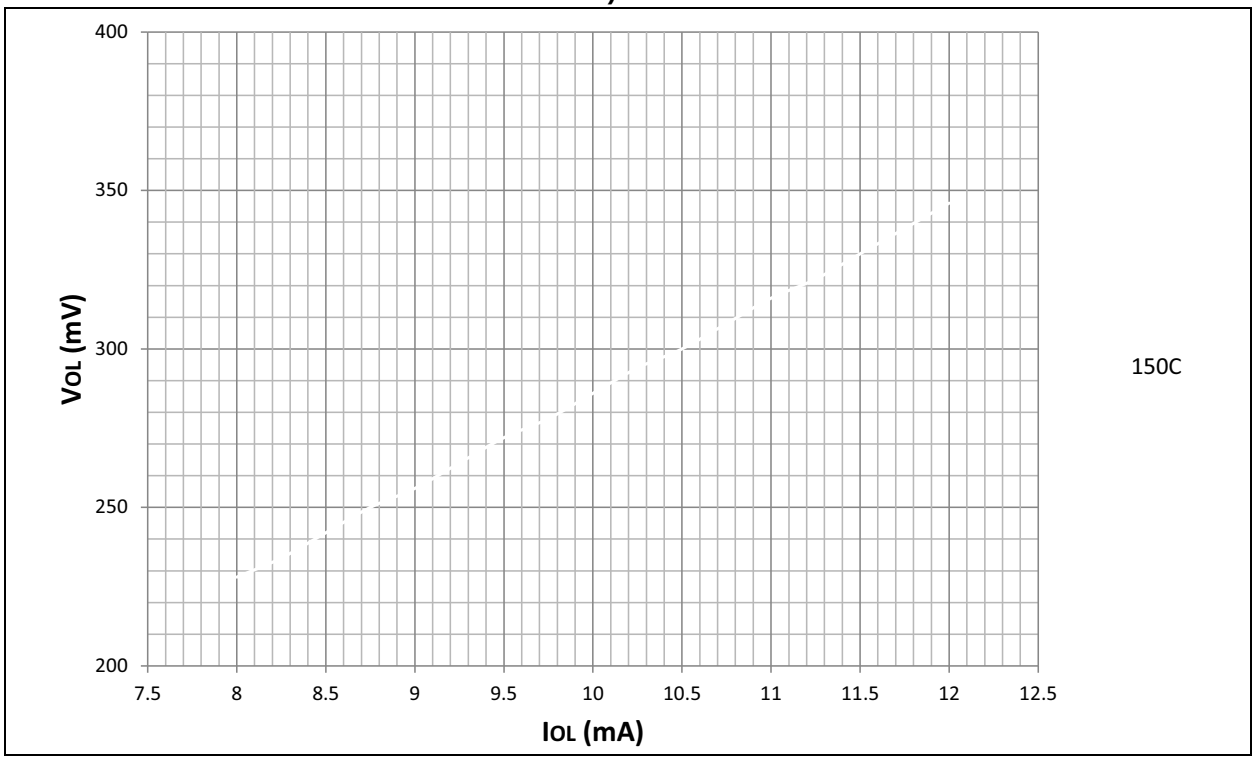
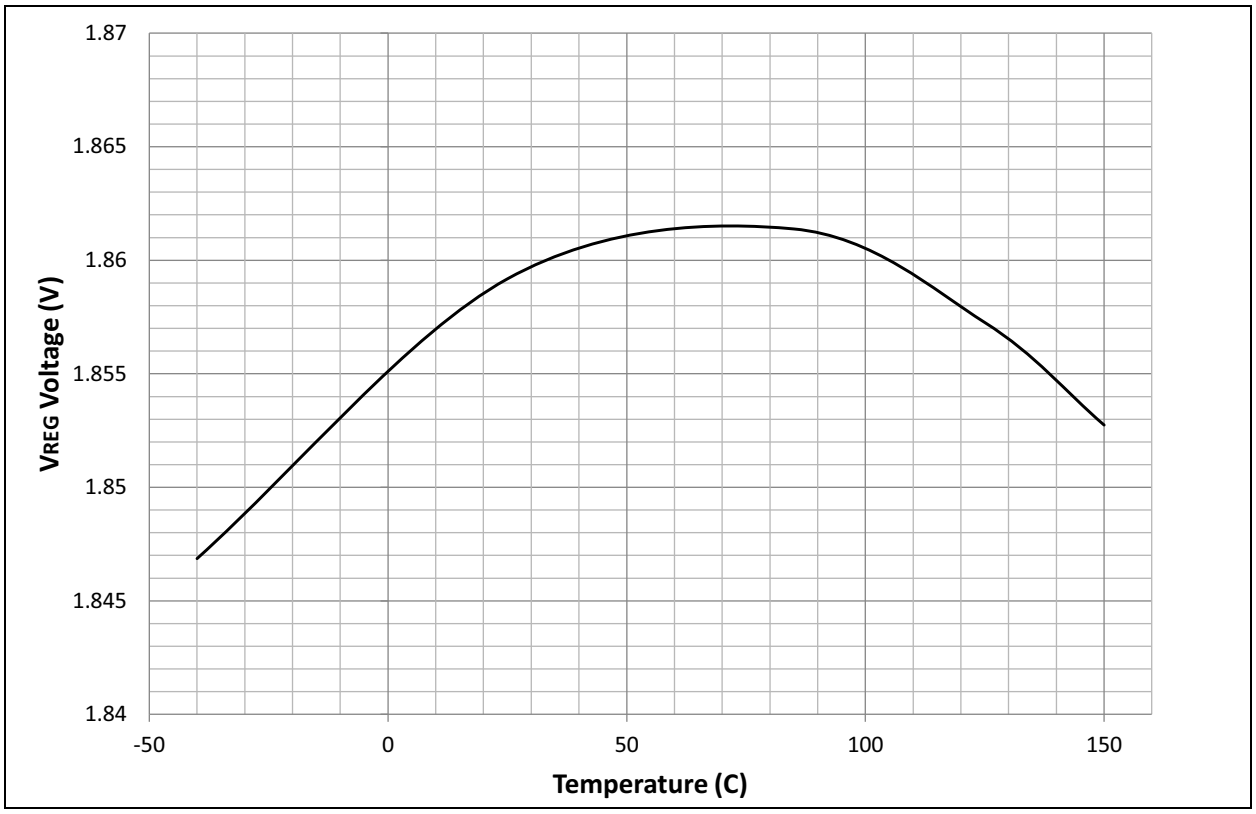


FIGURE 33-29: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



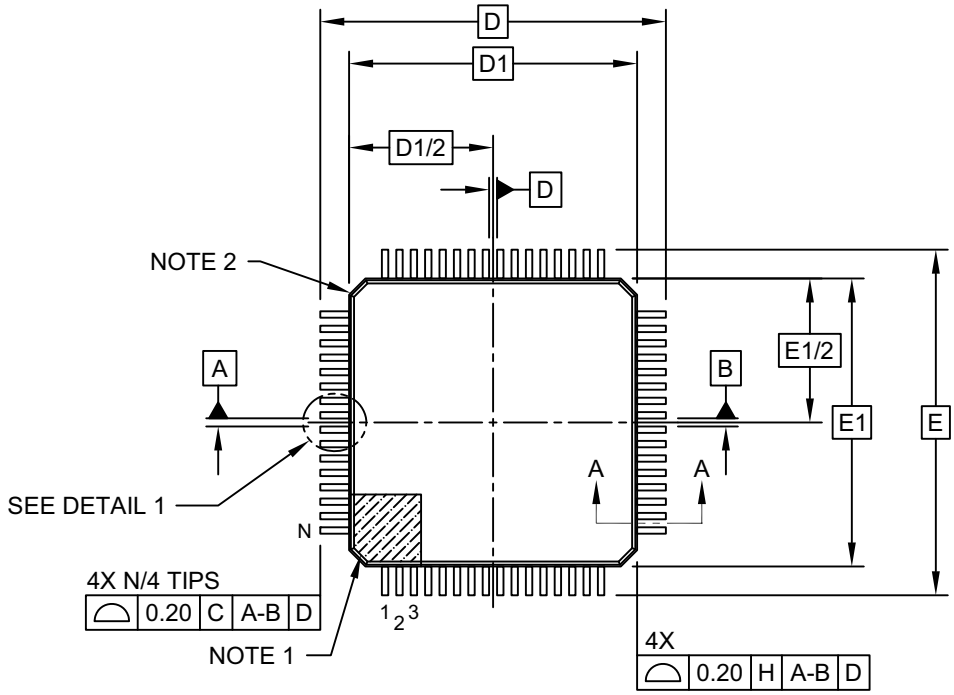
33.11 VREG

FIGURE 33-30: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE

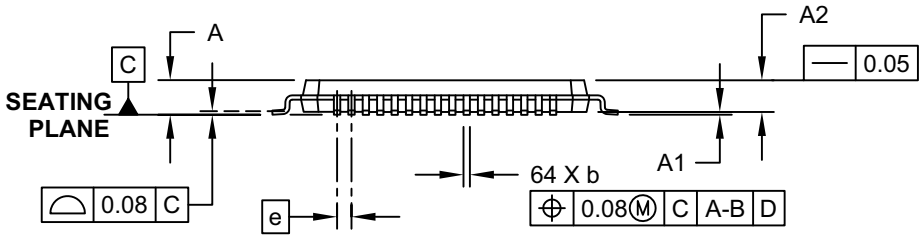


64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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