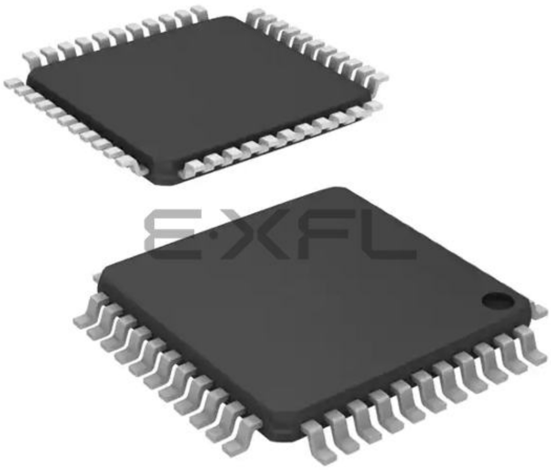

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	32KB (11K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev32gm104t-i-pt

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not exceeding 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the “Communication Channel Select” (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site (www.microchip.com).

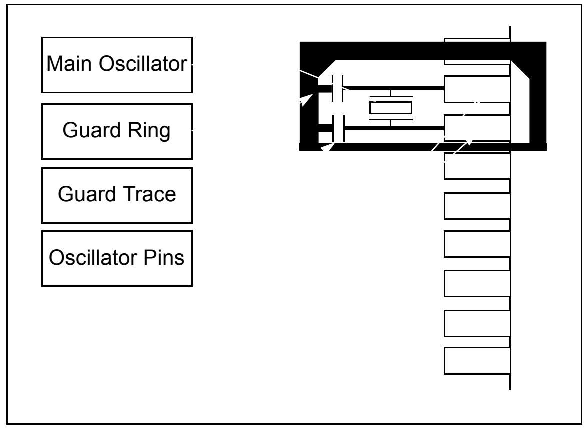
- *“Using MPLAB® ICD 3”* (poster) (DS51765)
- *“MPLAB® ICD 3 Design Advisory”* (DS51764)
- *“MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide”* (DS51616)
- *“Using MPLAB® REAL ICE™ In-Circuit Emulator”* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For more information, see **Section 9.0 “Oscillator Configuration”**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed as shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < F_{IN} < 13.6 MHz to comply with device PLL start-up conditions. This intends that, if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source.

Note:	Clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins, and drive the output to logic low.

3.0 CPU

> **Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CPU"** (DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EVXXXGM00X/10X family devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The sixteenth Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

In addition, the dsPIC33EVXXXGM00X/10X devices include two alternate Working register sets, which consist of W0 through W14. The alternate registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx<2:0> bits in the FALTREG Configuration register.

The alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction.

The CCTXI<2:0> and MCTXI<2:0> bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EV devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. For more information on EDS, PSV and table accesses, refer to **"Data Memory"** (DS70595) and **"dsPIC33E/PIC24E Program Memory"** (DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*.

On dsPIC33EV devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. Figure 3-1 illustrates the block diagram of the dsPIC33EVXXXGM00X/10X family devices.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

FIGURE 7-1: dsPIC33EVXXXGM00X/10X FAMILY ALTERNATE INTERRUPT VECTOR TABLE

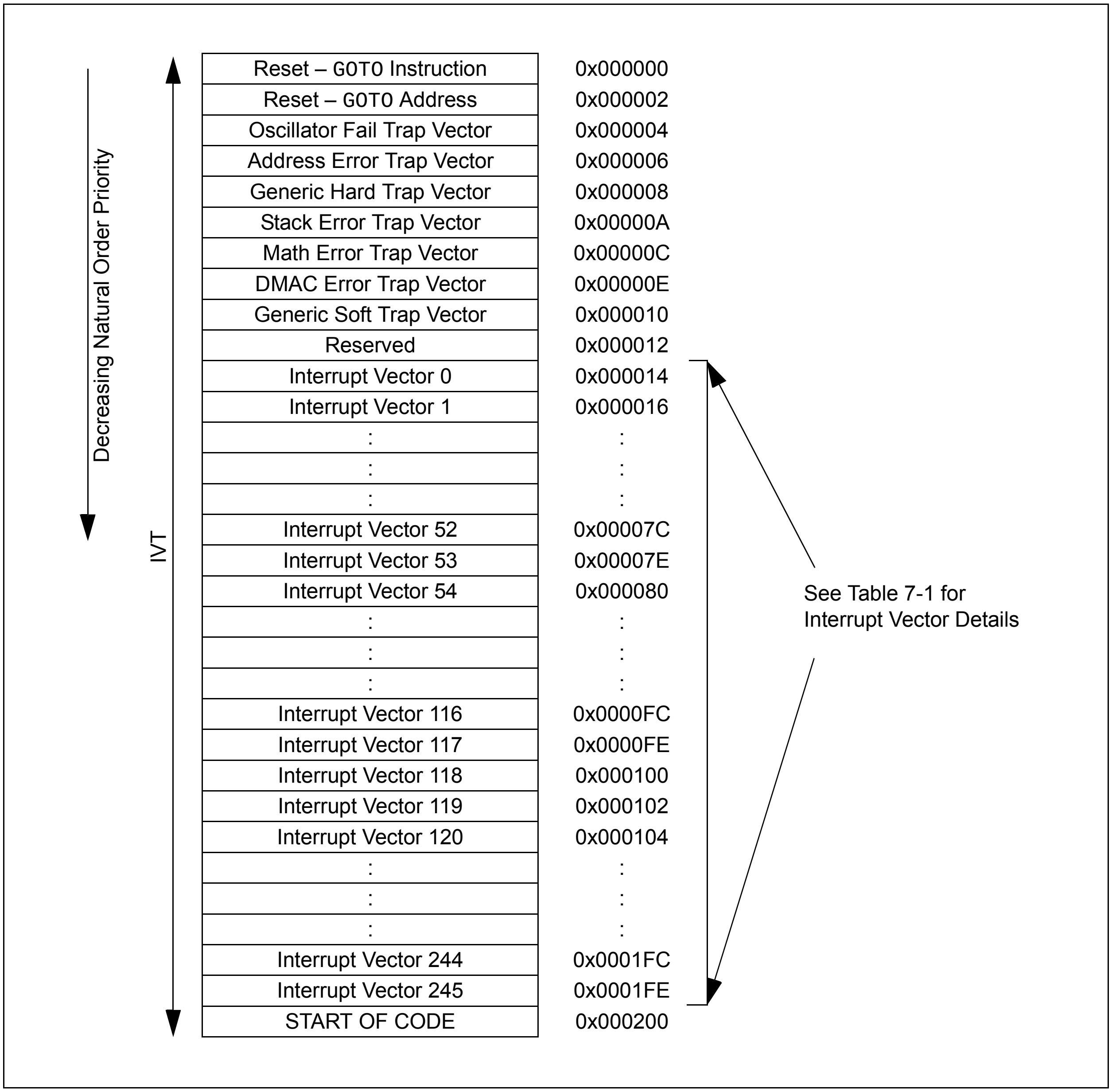
IVT

Reserved	BSLIM<12:0>(1) + 0x000000
Reserved	BSLIM<12:0>(1) + 0x000002
Oscillator Fail Trap Vector	BSLIM<12:0>(1) + 0x000004
Address Error Trap Vector	BSLIM<12:0>(1) + 0x000006
Generic Hard Trap Vector	BSLIM<12:0>(1) + 0x000008
Stack Error Trap Vector	BSLIM<12:0>(1) + 0x00000A
Math Error Trap Vector	BSLIM<12:0>(1) + 0x00000C
DMAC Error Trap Vector	BSLIM<12:0>(1) + 0x00000E
Generic Soft Trap Vector	BSLIM<12:0>(1) + 0x000010
Reserved	BSLIM<12:0>(1) + 0x000012
Interrupt Vector 0	BSLIM<12:0>(1) + 0x000014
Interrupt Vector 1	BSLIM<12:0>(1) + 0x000016
:	:
:	:
:	:
Interrupt Vector 52	BSLIM<12:0>(1) + 0x00007C
Interrupt Vector 53	BSLIM<12:0>(1) + 0x00007E
Interrupt Vector 54	BSLIM<12:0>(1) + 0x000080
:	:
:	:
:	:
Interrupt Vector 116	BSLIM<12:0>(1) + 0x0000FC
Interrupt Vector 117	BSLIM<12:0>(1) + 0x00007E
Interrupt Vector 118	BSLIM<12:0>(1) + 0x000100
Interrupt Vector 119	BSLIM<12:0>(1) + 0x000102
Interrupt Vector 120	BSLIM<12:0>(1) + 0x000104
:	:
:	:
:	:
Interrupt Vector 244	BSLIM<12:0>(1) + 0x0001FC
Interrupt Vector 245	BSLIM<12:0>(1) + 0x0001FE

See Table 7-1 for Interrupt Vector Details

Note 1: The address depends on the size of the Boot Segment defined by BSLIM<12:0>: [(BSLIM<12:0> – 1) x 0x400] + Offset.

FIGURE 7-2: dsPIC33EVXXXGM00X/10X FAMILY INTERRUPT VECTOR TABLE



REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 1 **PWCOL1:** Channel 1 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 0 **PWCOL0:** Channel 0 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
—	—	—	DMA0MD(1) DMA1MD(1) DMA2MD(1) DMA3MD(1)	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4 **DMA0MD:** DMA0 Module Disable bit(1)
1 = DMA0 module is disabled
0 = DMA0 module is enabled

DMA1MD: DMA1 Module Disable bit(1)
1 = DMA1 module is disabled
0 = DMA1 module is enabled

DMA2MD: DMA2 Module Disable bit(1)
1 = DMA2 module is disabled
0 = DMA2 module is enabled

DMA3MD: DMA3 Module Disable bit(1)
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: This single bit enables and disables all four DMA channels.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name(1)	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<7:0>
External Interrupt 2	INT2	RPINR1	INT2R<7:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<7:0>
Input Capture 1	IC1	RPINR7	IC1R<7:0>
Input Capture 2	IC2	RPINR7	IC2R<7:0>
Input Capture 3	IC3	RPINR8	IC3R<7:0>
Input Capture 4	IC4	RPINR8	IC4R<7:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<7:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<7:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<7:0>
UART1 Receive	U1RX	RPINR18	U1RXR<7:0>
UART2 Receive	U2RX	RPINR19	U2RXR<7:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<7:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<7:0>
SPI2 Slave Select	$\overline{\text{SS2}}$	RPINR23	SS2R<7:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<7:0>
PWM Sync Input 1	SYNCI1	RPINR37	SYNCI1R<7:0>
PWM Dead-Time Compensation 1	DTCMP1	RPINR38	DTCMP1R<7:0>
PWM Dead-Time Compensation 2	DTCMP2	RPINR39	DTCMP2R<7:0>
PWM Dead-Time Compensation 3	DTCMP3	RPINR39	DTCMP3R<7:0>
SENT1 Input	SENT1R	RPINR44	SENT1R<7:0>
SENT2 Input	SENT2R	RPINR45	SENT2R<7:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK2R<7:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to VSS

bit 7-0 **SDI2R<7:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to VSS

BUFFER 22-3: CANx MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-10 **EID<5:0>:** Extended Identifier bits

bit 9 **RTR:** Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.

bit 8 **RB1:** Reserved Bit 1
User must set this bit to ‘0’ per CAN protocol.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **RB0:** Reserved Bit 0
User must set this bit to ‘0’ per CAN protocol.

bit 3-0 **DLC<3:0>:** Data Length Code bits

BUFFER 22-4: CANx MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1<15:8>							
bit 15							bit 8

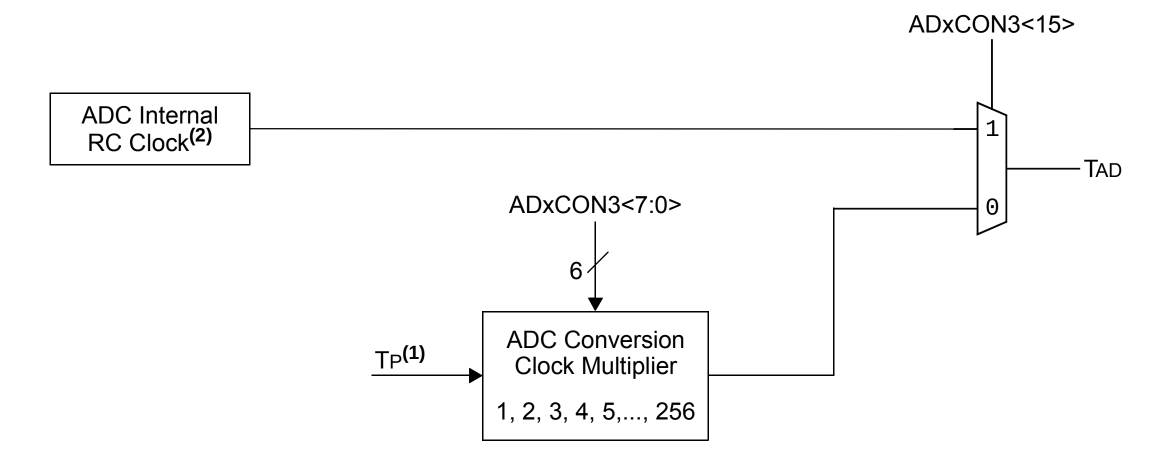
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 1<15:8>:** CANx Message Byte 1 bits

bit 7-0 **Byte 0<7:0>:** CANx Message Byte 0 bits

FIGURE 24-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM



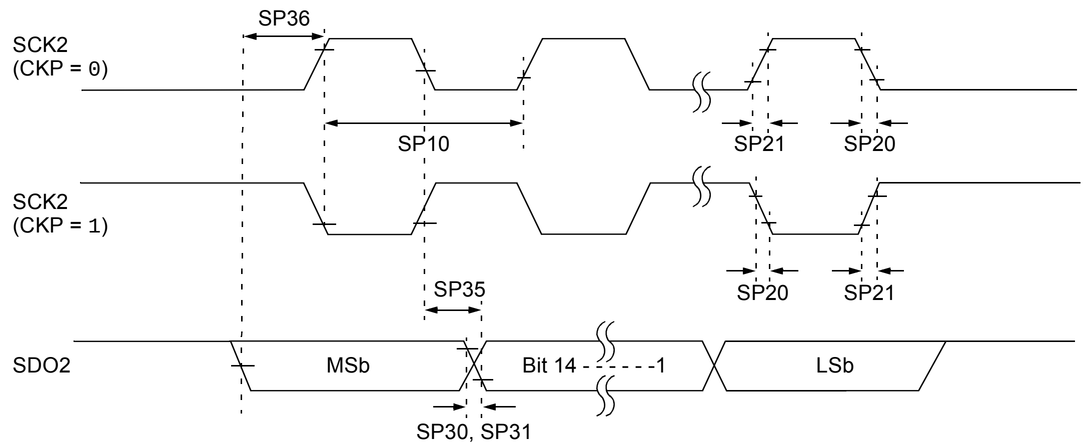
Note 1: TP = 1/FP.

2: Refer to the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

24.2 ADC Helpful Tips

1. The SMPIx control bits in the ADxCON2 registers:
   a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
   b) When the CSCNA bit in the ADxCON2 register is set to '1', this determines when the ADC analog scan channel list, defined in the ADxCSSL/ADxCSSH registers, starts over from the beginning.
   c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
   d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using the DMA peripheral.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1.c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADCxBUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUX A selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. For configuration examples, refer to **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 30-13: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-31: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK2 Frequency	—	—	15	MHz	See **Note 3**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.
2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.
3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.
4: Assumes 50 pF load on all SPI1 pins.

TABLE 31-13: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
HOS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
HOS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
HOS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
HOS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	

Note 1: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 31-14: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
HF20C	FRC	-3	1	+3	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

TABLE 31-15: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**	
LPRC @ 32.768 kHz(1,2)							
HF21C	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 27.5 “Watchdog Timer (WDT)”** for more information.

32.0 CHARACTERISTICS FOR INDUSTRIAL/EXTENDED TEMPERATURE DEVICES (-40°C TO +125°C)

32.1 IDD

FIGURE 32-1: TYPICAL/MAXIMUM IDD vs. FOSC (EC MODE, 10 MHz TO 70 MHz, 5.5V MAX)

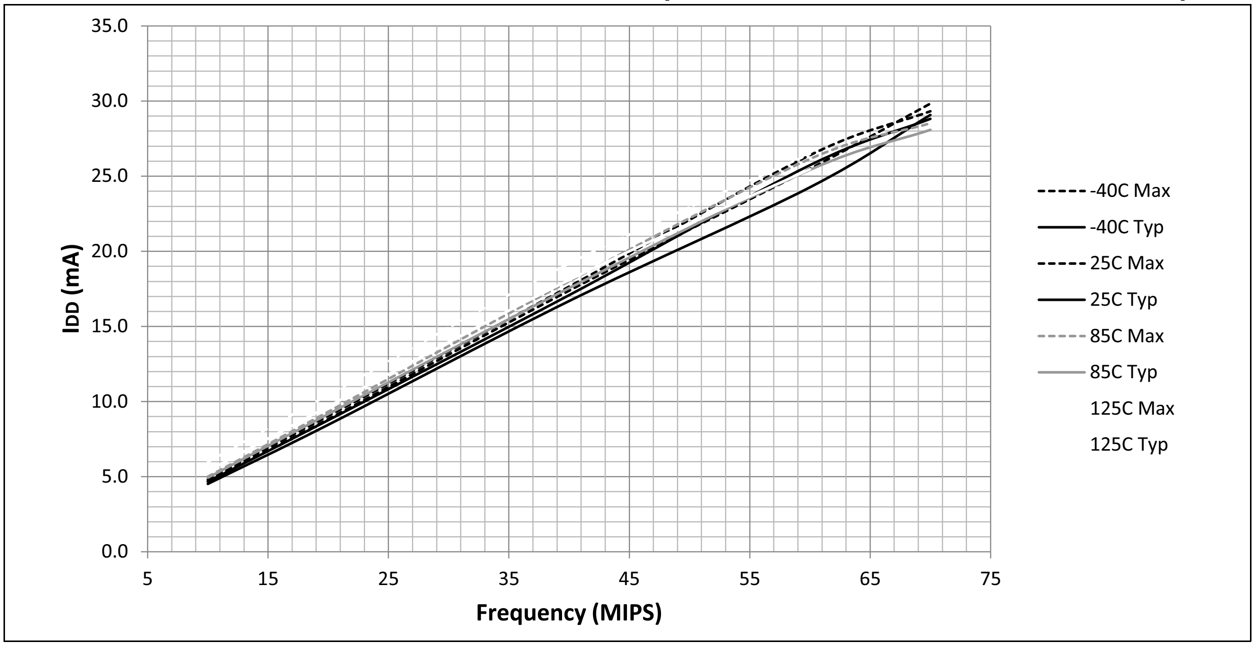
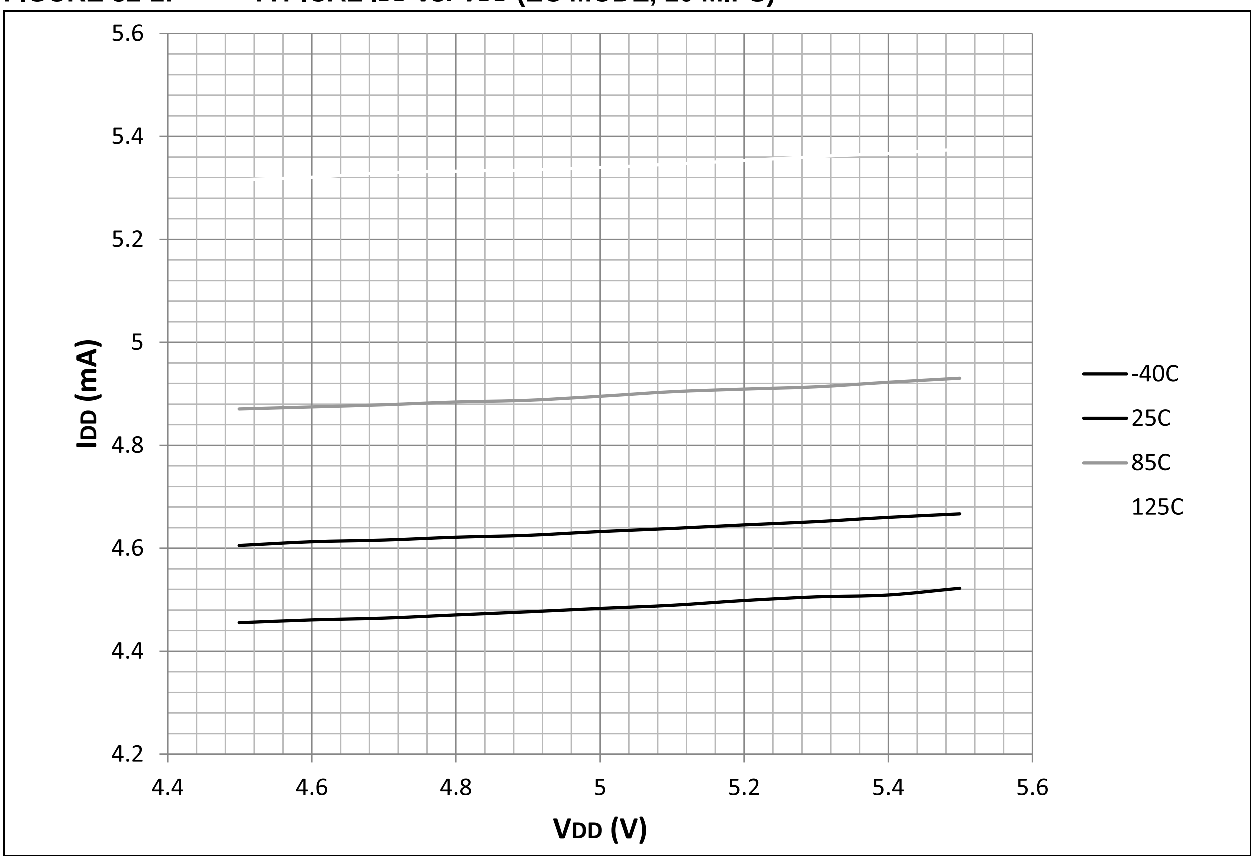


FIGURE 32-2: TYPICAL IDD vs. VDD (EC MODE, 10 MIPS)



32.2 IIDLE

FIGURE 32-7: TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 70 MHz, 5.5V MAX)

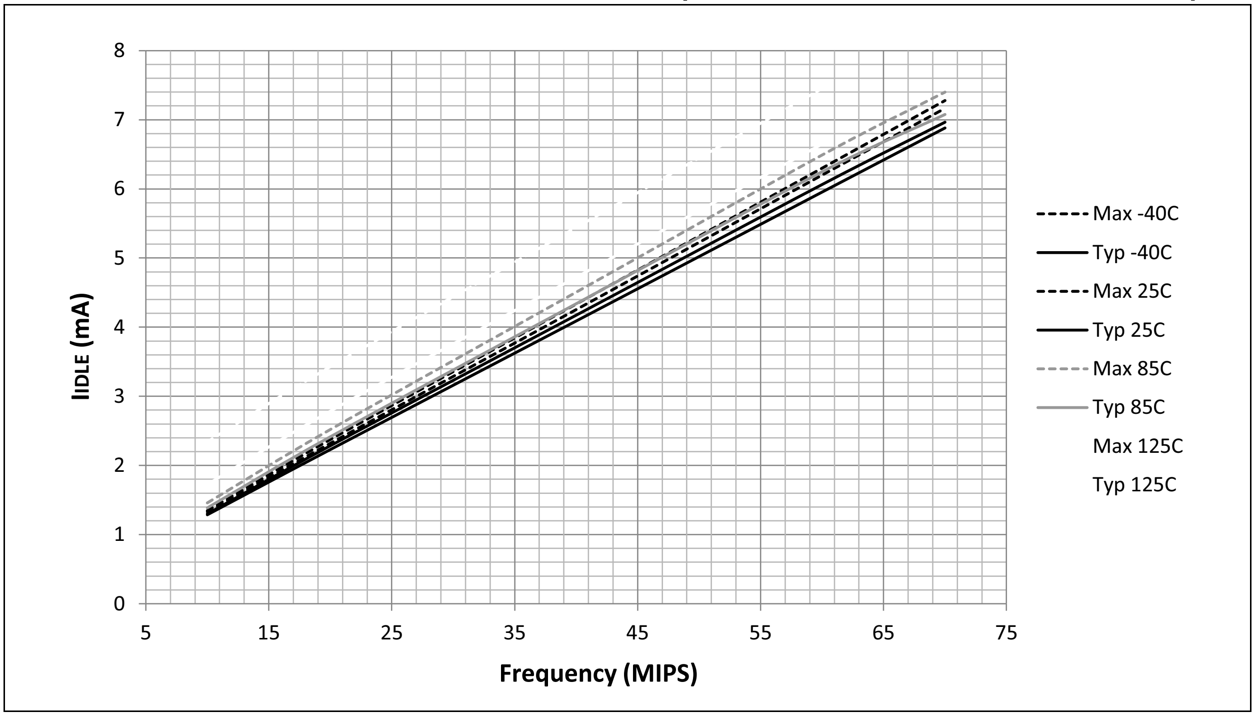


FIGURE 32-8: TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)

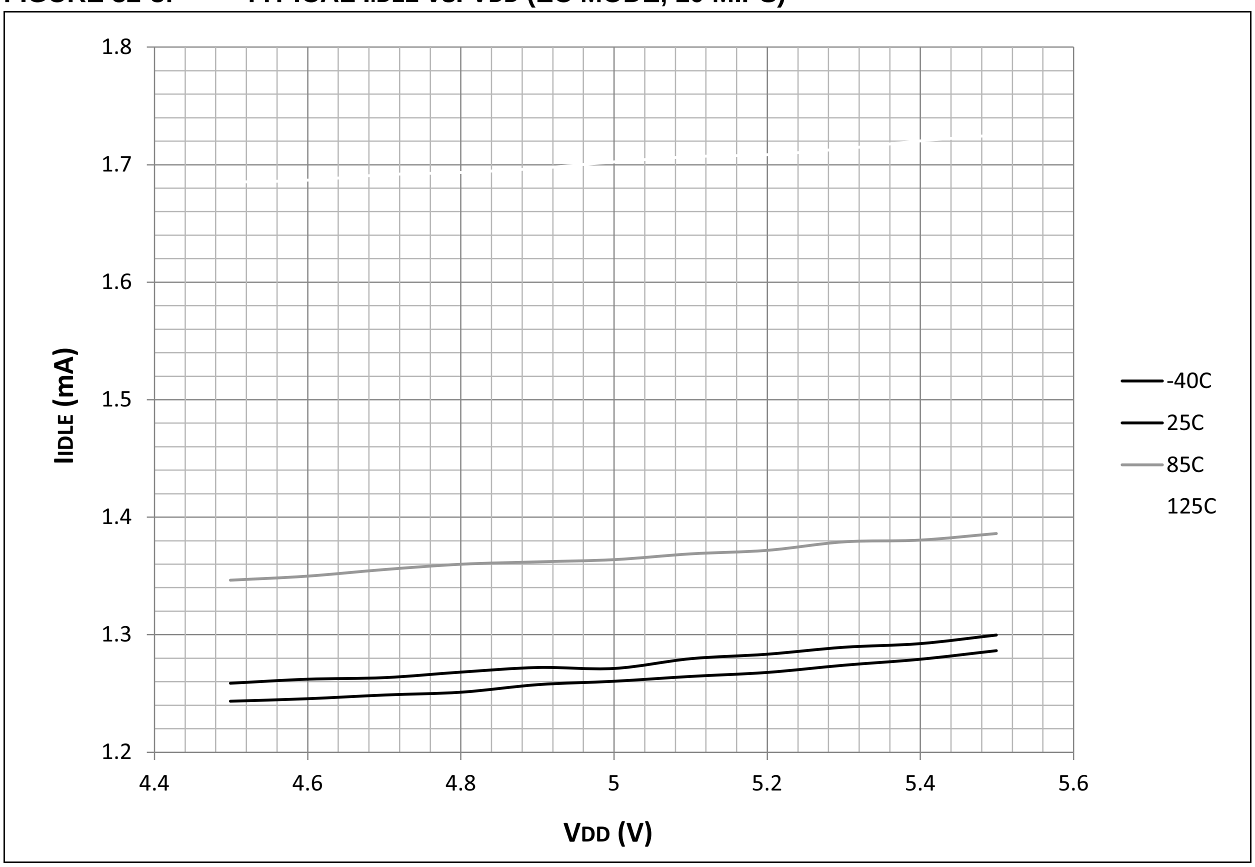
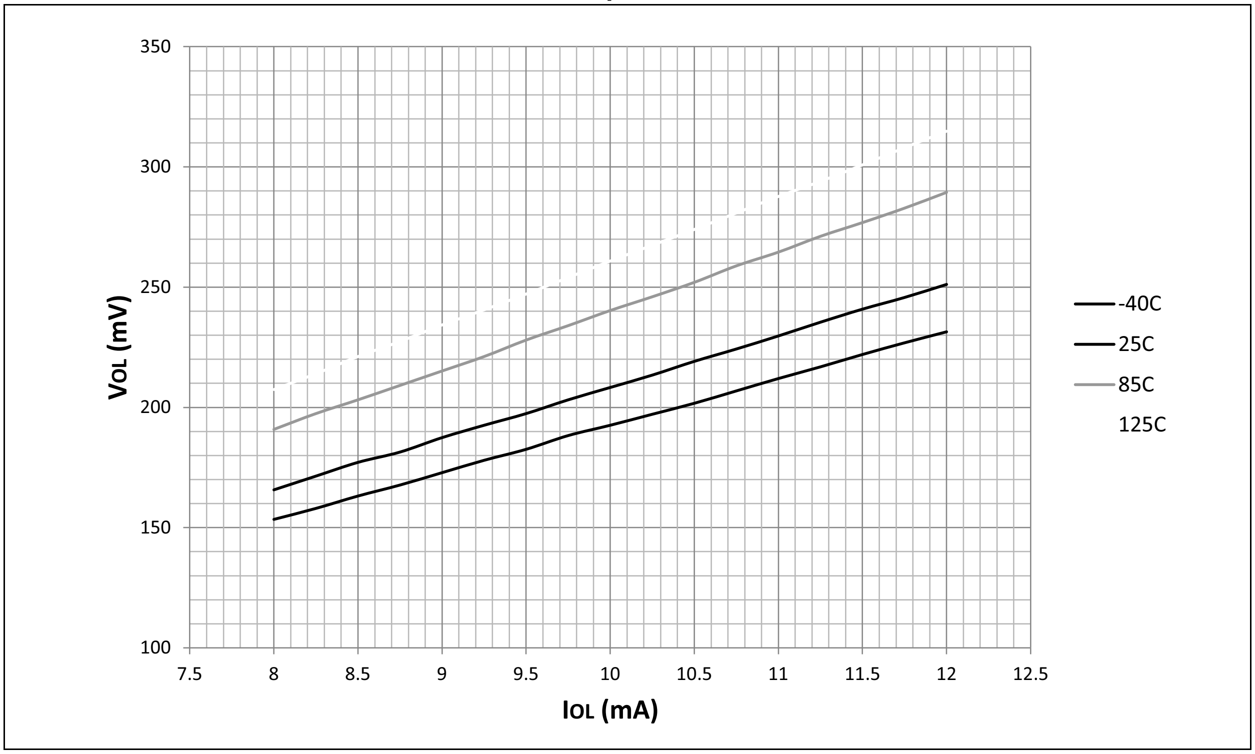


FIGURE 32-33: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



32.11 VREG

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE

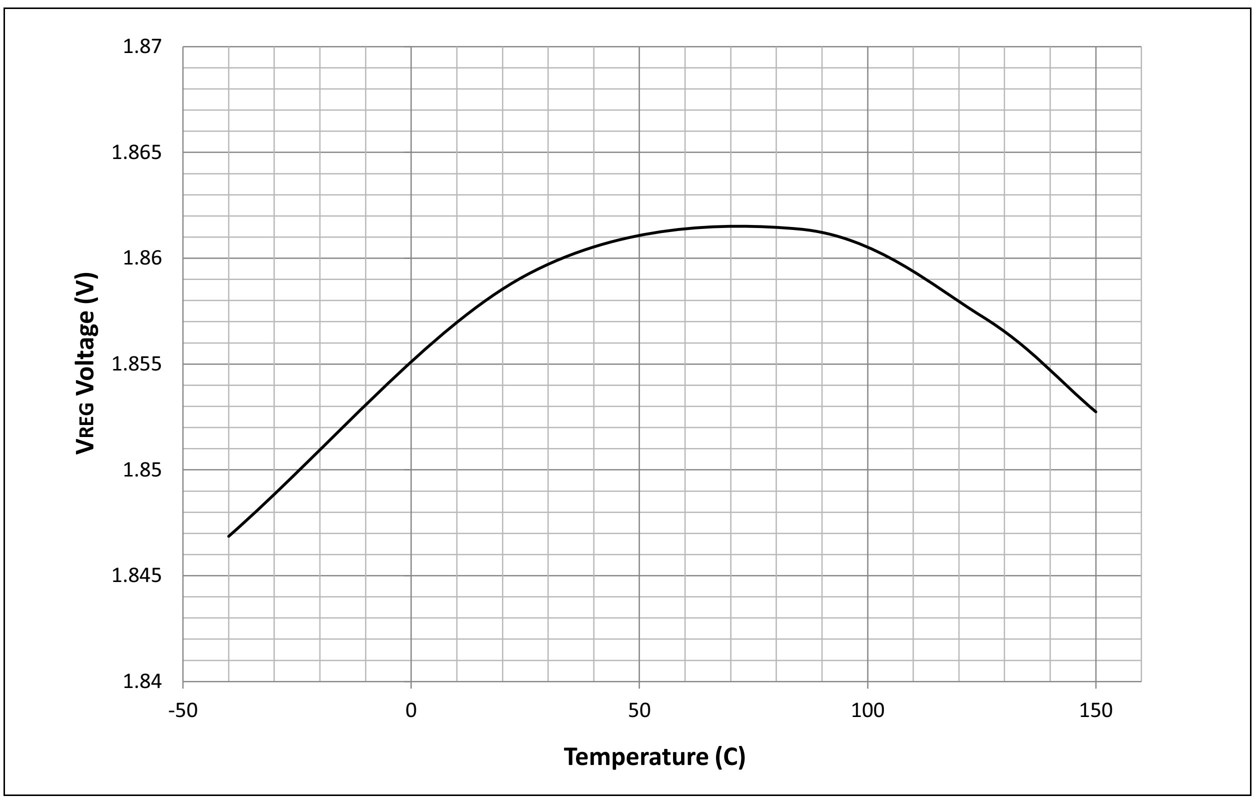


FIGURE 32-43: TYPICAL DNL (V_{DD} = 5.5V, +85°C)

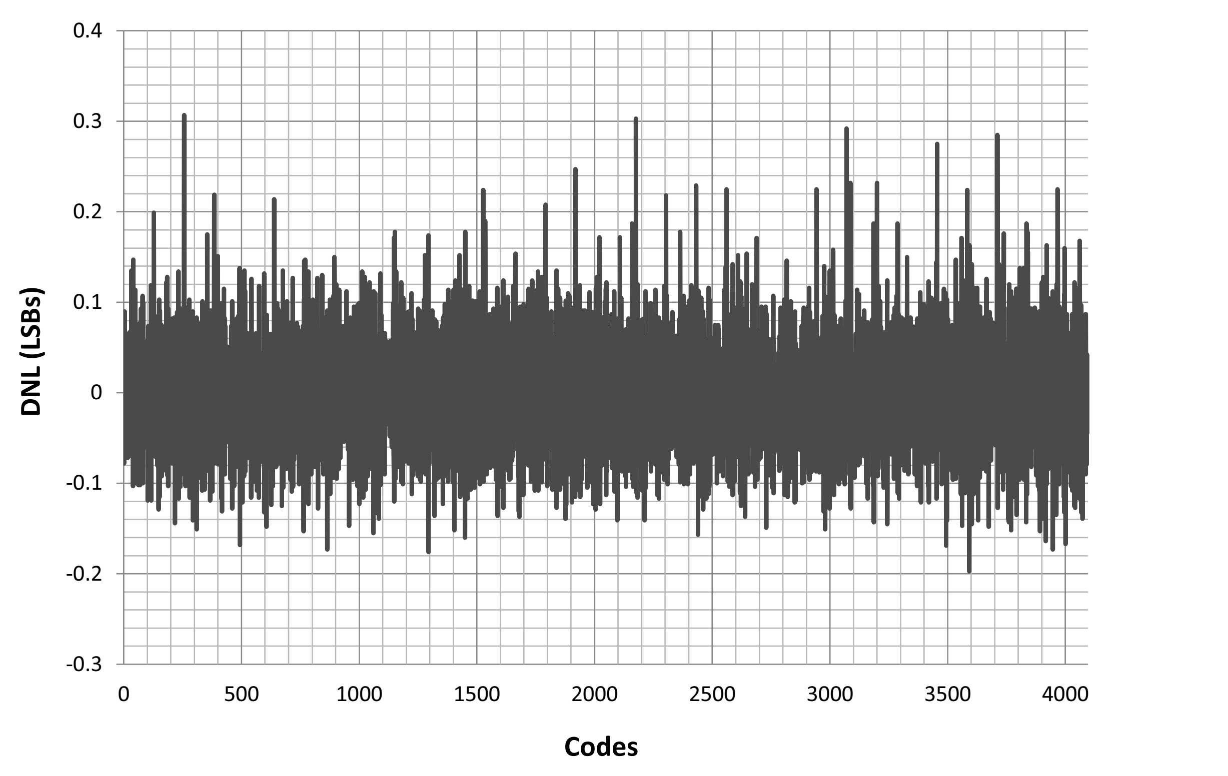


FIGURE 32-44: TYPICAL DNL (V_{DD} = 5.5V, +125°C)

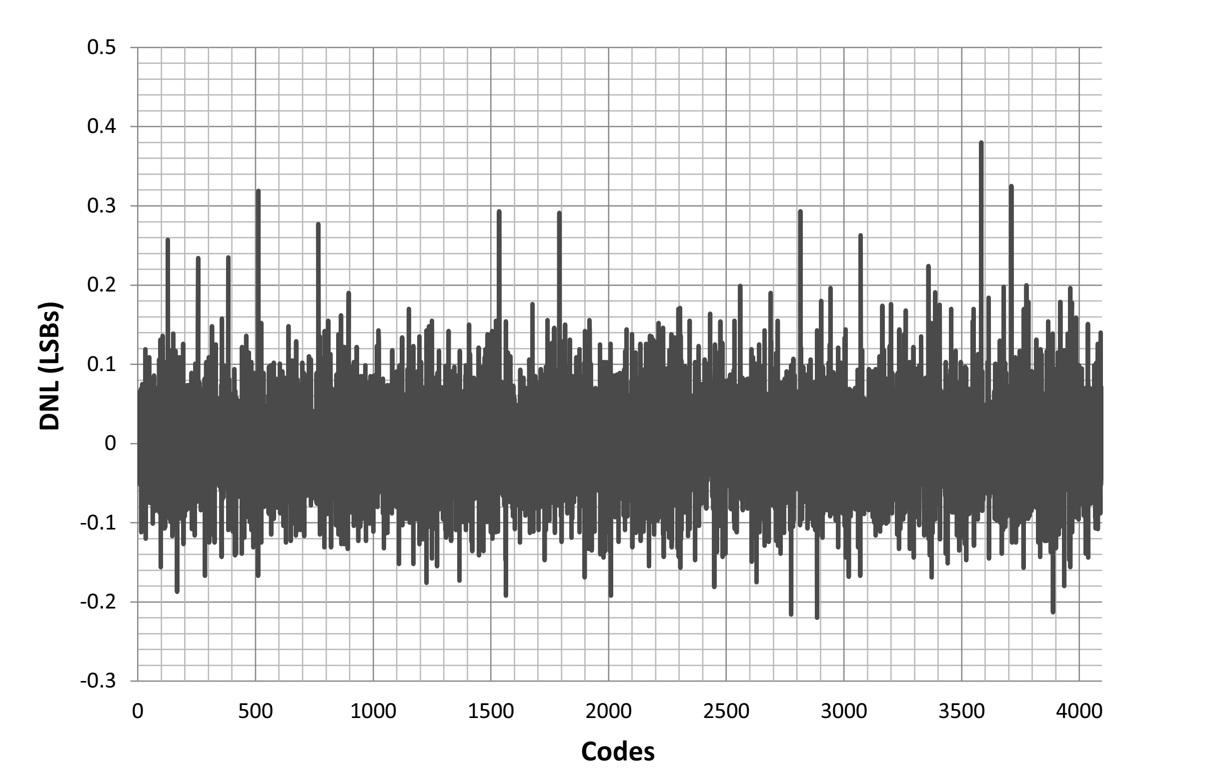


FIGURE 33-7: TYPICAL IIDLE vs. VDD (EC MODE, 20 MIPS)

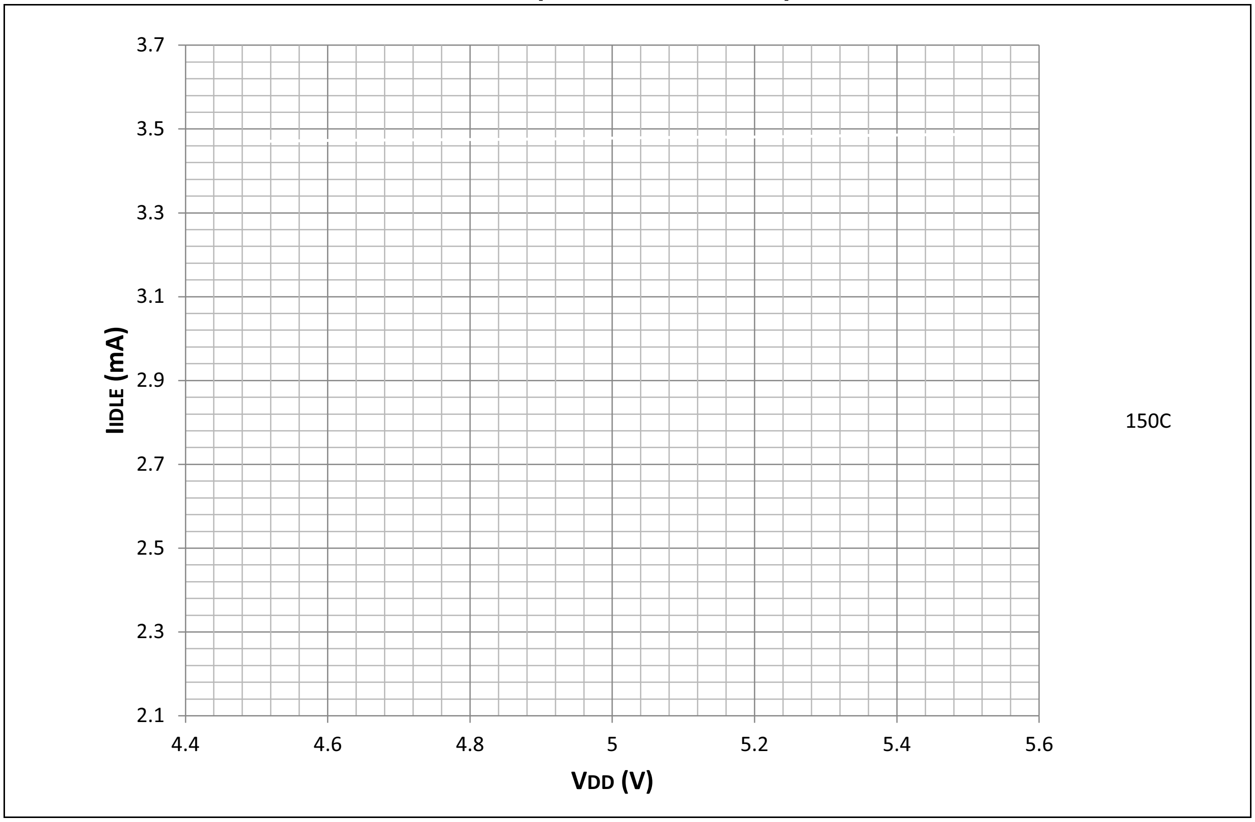
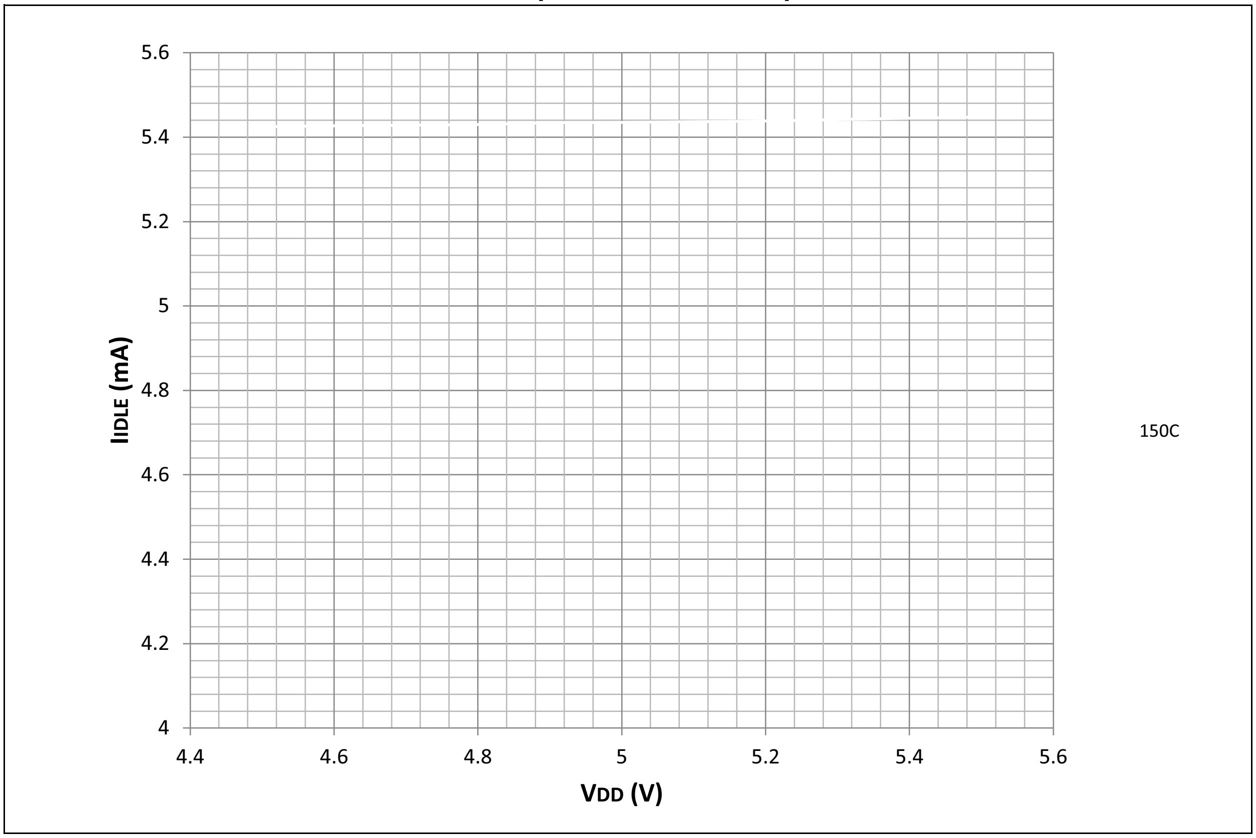
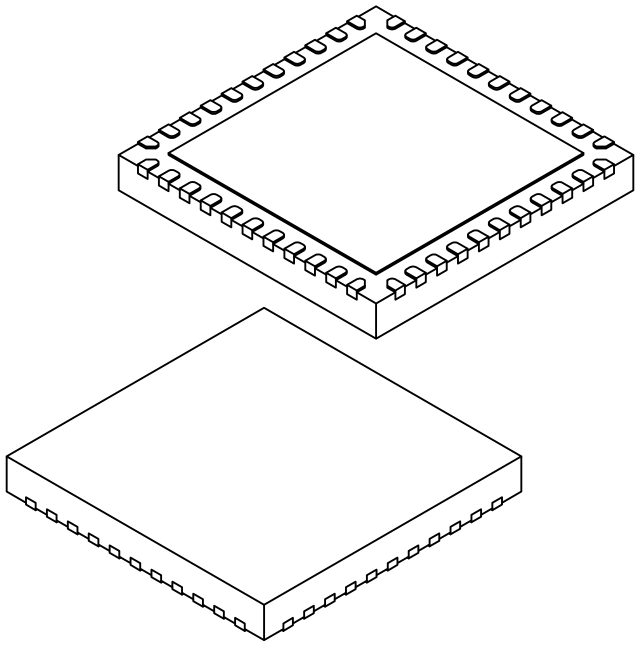


FIGURE 33-8: TYPICAL IIDLE vs. VDD (EC MODE, 40 MIPS)



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2