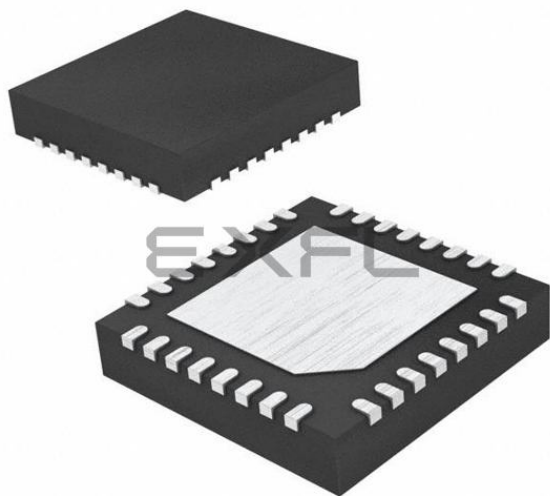




Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm002-e-mm

[illegible]

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 μF to 47 μF .

A low-ESR (<1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 μ F (10 μ F is recommended), with at least a 16V rating connected to the ground. The type can be ceramic or tantalum. See **Section 30.0 “Electrical Characteristics”** for additional information.

2.4 Master Clear (MCLR) Pin

- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (V_{IH} and V_{IL}) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-1, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

The diagram shows a circuit for the MCLR pin of a dsPIC33EV. The MCLR pin is connected to VDD through a resistor labeled R(1). It is also connected to an external capacitor C through a resistor labeled R(2). The capacitor C is connected to ground. The dsPIC33EV is represented by a box with the label MCLR and dsPIC33EV.

TABLE 4-5: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	UART1 Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	UART2 Baud Rate Generator Prescaler Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: PERIPHERAL INPUT REMAP REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	INT1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	INT2R<7:0>								0000
RPINR3	06A6	—	—	—	—	—	—	—	—	T2CKR<7:0>								0000
RPINR7	06AE	IC2R7	IC2R6	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0	IC1R7	IC1R6	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0	0000
RPINR8	06B0	IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0	IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0	0000
RPINR11	06B6	—	—	—	—	—	—	—	—	OCFAR<7:0>								0000
RPINR12	06B8	FLT2R7	FLT2R6	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0	FLT1R7	FLT1R6	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0	0000
RPINR18	06C4	—	—	—	—	—	—	—	—	U1RXR<7:0>								0000
RPINR19	06C6	—	—	—	—	—	—	—	—	U2RXR<7:0>								0000
RPINR22	06CC	SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0	SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0	0000
RPINR23	06CE	—	—	—	—	—	—	—	—	SS2R<7:0>								0000
RPINR26	06D4	—	—	—	—	—	—	—	—	C1RXR<7:0> ⁽¹⁾								0000
RPINR37	06EA	SYNC1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR38	06EC	DTCMP1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR39	06EE	DTCMP3R7	DTCMP3R6	DTCMP3R5	DTCMP3R4	DTCMP3R3	DTCMP3R2	DTCMP3R1	DTCMP3R0	DTCMP2R7	DTCMP2R6	DTCMP2R5	DTCMP2R4	DTCMP2R3	DTCMP2R2	DTCMP2R1	DTCMP2R0	0000
RPINR44	06F8	SENT1R<7:0>								—	—	—	—	—	—	—	—	0000
RPINR45	06FA	—	—	—	—	—	—	—	—	SENT2R<7:0>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXGM10X devices.

TABLE 4-18: DMT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
DMTCON	0700	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000	
DMTPRECLR	0704	STEP1<7:0>									—	—	—	—	—	—	—	—	0000
DMTCLR	0708	—	—	—	—	—	—	—	—	STEP2<7:0>								0000	
DMTSTAT	070C	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000	
DMTCNTL	0710	COUNTER<15:0>																	0000
DMTCNTH	0712	COUNTER<31:16>																	0000
DMTHOLDREG	0714	UPRCNT<15:0>																	0000
DMTPSCNTL	0718	PSCNT<15:0>																	0000
DMTPSCNTH	071A	PSCNT<31:16>																	0000
DMTPSINTVL	071C	PSINTV<15:0>																	0000
DMTPSINTVH	071E	PSINTV<31:16>																	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-24: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA<12:7>						—	—	TRISA4	—	—	TRISA<1:0>		1F93
PORTA	0E02	—	—	—	RA<12:7>						—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	—	—	—	LATA<12:7>						—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	—	—	—	ODCA<12:7>						—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	—	—	—	CNIEA<12:7>						—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	—	—	—	CNPUA<12:7>						—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	—	—	—	CNPDA<12:7>						—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	—	—	—	ANSA<12:9>				—	ANSA7	—	—	ANSA4	—	—	ANSA<1:0>		1E93
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA<10:7>				—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	RA<10:7>				—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	LATA<10:7>				—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	ODCA<10:7>				—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	CNIEA<10:7>				—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	CNPUA<10:7>				—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	CNPDA<10:7>				—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	ANSA<10:9>		—	ANSA7	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.3.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the MPLAB® ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the highest priority. The access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the MPLAB ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities

below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are listed in Table 4-44.

Figure 4-13 shows the arbiter architecture.

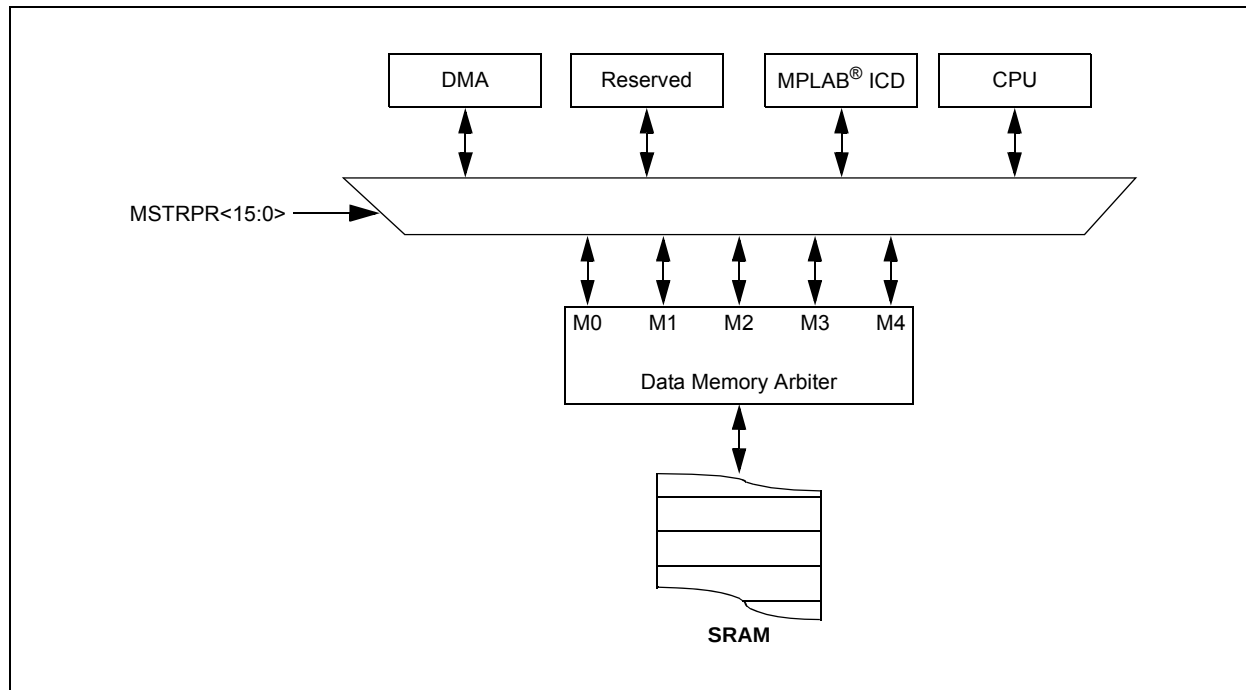
The bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-44: DATA MEMORY BUS ARBITER PRIORITY

Priority	MSTRPR<15:0> Bit Setting ⁽¹⁾	
	0x0000	0x0020
M0 (highest)	CPU	DMA
M1	Reserved	CPU
M2	Reserved	Reserved
M3	DMA	Reserved
M4 (lowest)	MPLAB® ICD	MPLAB ICD

Note 1: All other values of MSTRPR<15:0> are reserved.

FIGURE 4-13: ARBITER ARCHITECTURE



dsPIC33EVXXGM00X/10X FAMILY

4.3.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the SSP (for example, creating stack frames).

Note: To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EVXXGM00X/10X family devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within the Data Space.

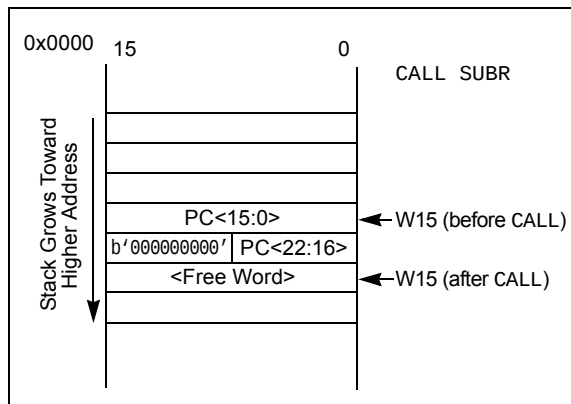
The SSP always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-14 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-14. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register (SR). This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1: To maintain system SSP (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).

2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a 'C' development environment.

FIGURE 4-14: CALL STACK FRAME



4.4 Instruction Addressing Modes

The addressing modes shown in Table 4-45 form the basis of the addressing modes optimized to support the specific features of the individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.4.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.4.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where, Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment
000 0000	I	Vss	011 0010	I	RPI50
000 0001	I	CMP1 ⁽¹⁾	011 0011	I	RPI51
000 0010	I	CMP2 ⁽¹⁾	011 0100	I	RPI52
000 0011	I	CMP3 ⁽¹⁾	011 0101	I	RPI53
000 0100	I	CMP4 ⁽¹⁾	011 0110	I/O	RP54
000 0101	—	—	011 0111	I/O	RP55
000 1100	I	CMP5 ⁽¹⁾	011 1000	I/O	RP56
000 1101	—	—	011 1001	I/O	RP57
000 1110	—	—	011 1010	I	RPI58
000 1111	—	—	011 1011	—	—
001 0000	I	RPI16	011 1100	I	RPI60
001 0001	I	RPI17	011 1101	I	RPI61
001 0010	I	RPI18	011 1110	—	—
001 0011	I	RPI19	011 1111	I	RPI 63
001 0100	I/O	RP20	100 0000	—	—
001 0101	—	—	100 0001	—	—
001 0110	—	—	100 0010	—	—
001 0111	—	—	100 0011	—	—
001 1000	I	RPI24	100 0100	—	—
001 1001	I	RPI25	100 0101	I/O	RP69
001 1010	—	—	100 0110	I/O	RP70
001 1011	I	RPI27	100 0111	—	—
001 1100	I	RPI28	100 1000	I	RPI72
001 1101	—	—	100 1001	—	—
001 1110	—	—	100 1010	—	—
001 1111	—	—	100 1011	—	—
010 0000	I	RPI32	100 1110	—	—
010 0001	I	RPI33	100 1111	—	—
010 0010	I	RPI34	101 0010	—	—
010 0011	I/O	RP35	101 0011	—	—
010 0100	I/O	RP36	101 0100	—	—
010 0101	I/O	RP37	010 1001	I/O	RP41
010 0110	I/O	RP38	010 1010	I/O	RP42
010 0111	I/O	RP39	010 1011	I/O	RP43
010 1000	I/O	RP40	101 1000	—	—
010 1100	I	RPI44	101 1001	—	—
010 1101	I	RPI45	101 1010	—	—
010 1110	I	RPI46	101 1011	—	—
010 1111	I	RPI47	101 1100	—	—
011 0000	I/O	RP48	101 1101	—	—

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

Note 1: These are virtual pins. See **Section 11.5.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT1R<7:0>							
bit 15							
bit 8							

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							
bit 0							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **SENT1R<7:0>**: Assign SENT Module Input 1 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•
•
•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

bit 7-0 **Unimplemented**: Read as '0'

REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT2R<7:0>							
bit 7							
bit 0							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented**: Read as '0'

bit 7-0 **SENT2R<7:0>**: Assign SENT Module Input 2 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•
•
•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTRx<13:0>:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx<13:8>					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **ALTDTRx<13:0>:** Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

FIGURE 20-1: SENTx MODULE BLOCK DIAGRAM

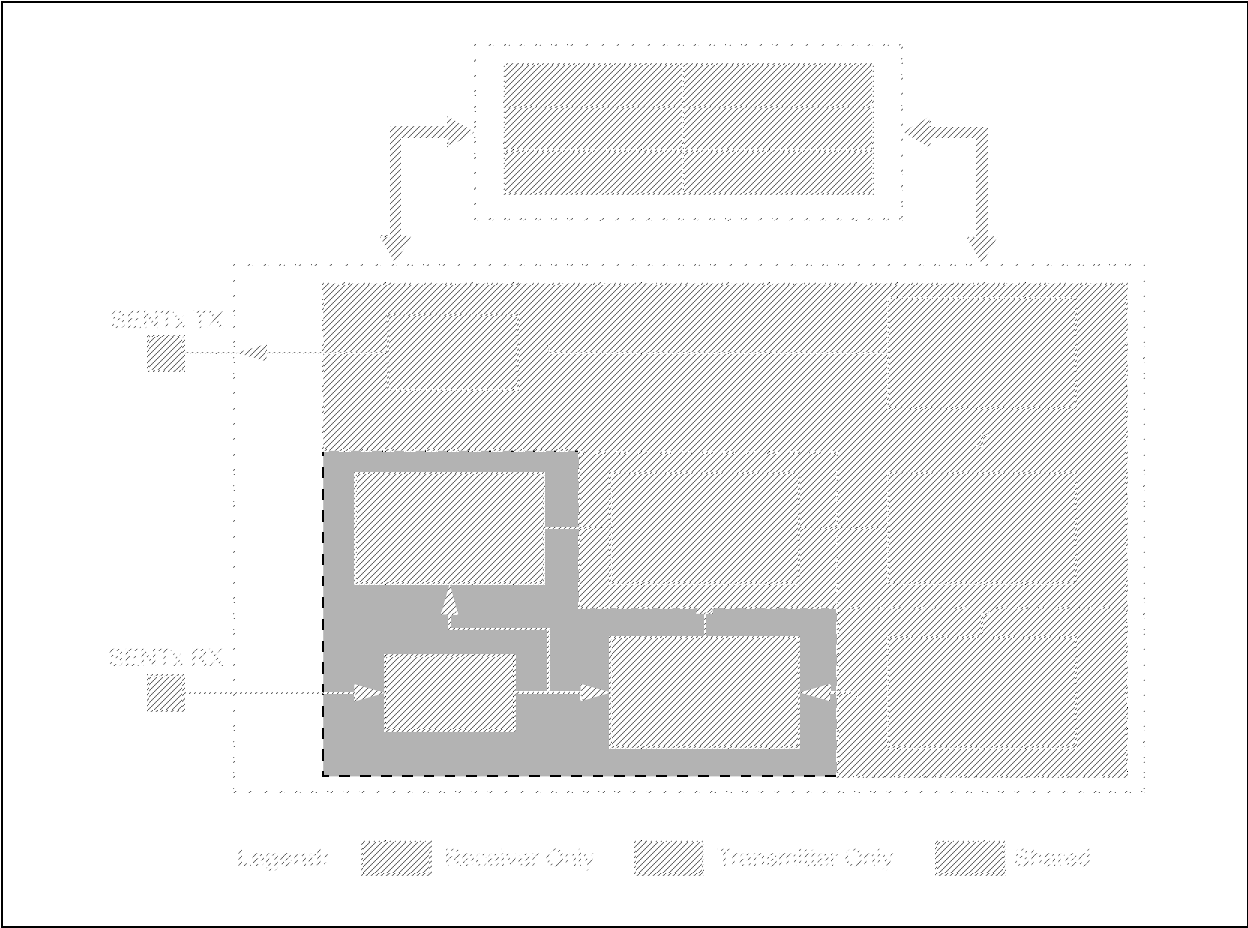
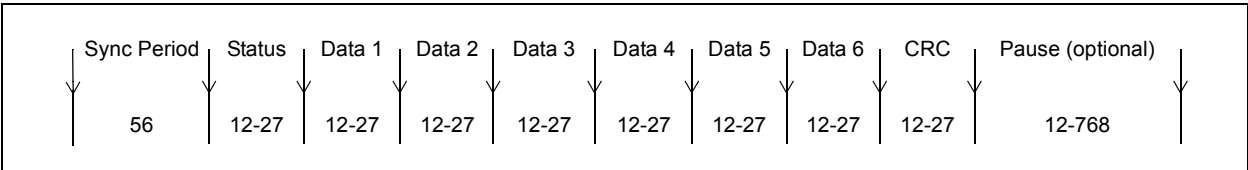


FIGURE 20-2: SENTx PROTOCOL DATA FRAMES



dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 21-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5	ABAU : Auto-Baud Enable bit 1 = Baud rate measurement on the next character is enabled – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion 0 = Baud rate measurement is disabled or has completed
bit 4	URXINV : UARTx Receive Polarity Inversion bit 1 = UxRX Idle state is '0' 0 = UxRX Idle state is '1'
bit 3	BRGH : High Baud Rate Enable bit 1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode) 0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)
bit 2-1	PDSEL<1:0> : Parity and Data Selection bits 11 = 9-bit data, no parity 10 = 8-bit data, odd parity 01 = 8-bit data, even parity 00 = 8-bit data, no parity
bit 0	STSEL : Stop Bit Selection bit 1 = Two Stop bits 0 = One Stop bit

Note 1: Refer to “**Universal Asynchronous Receiver Transmitter (UART)**” (DS70000582) in the “*dsPIC33/PIC24 Family Reference Manual*” for information on enabling the UART module for receive or transmit operation.

- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

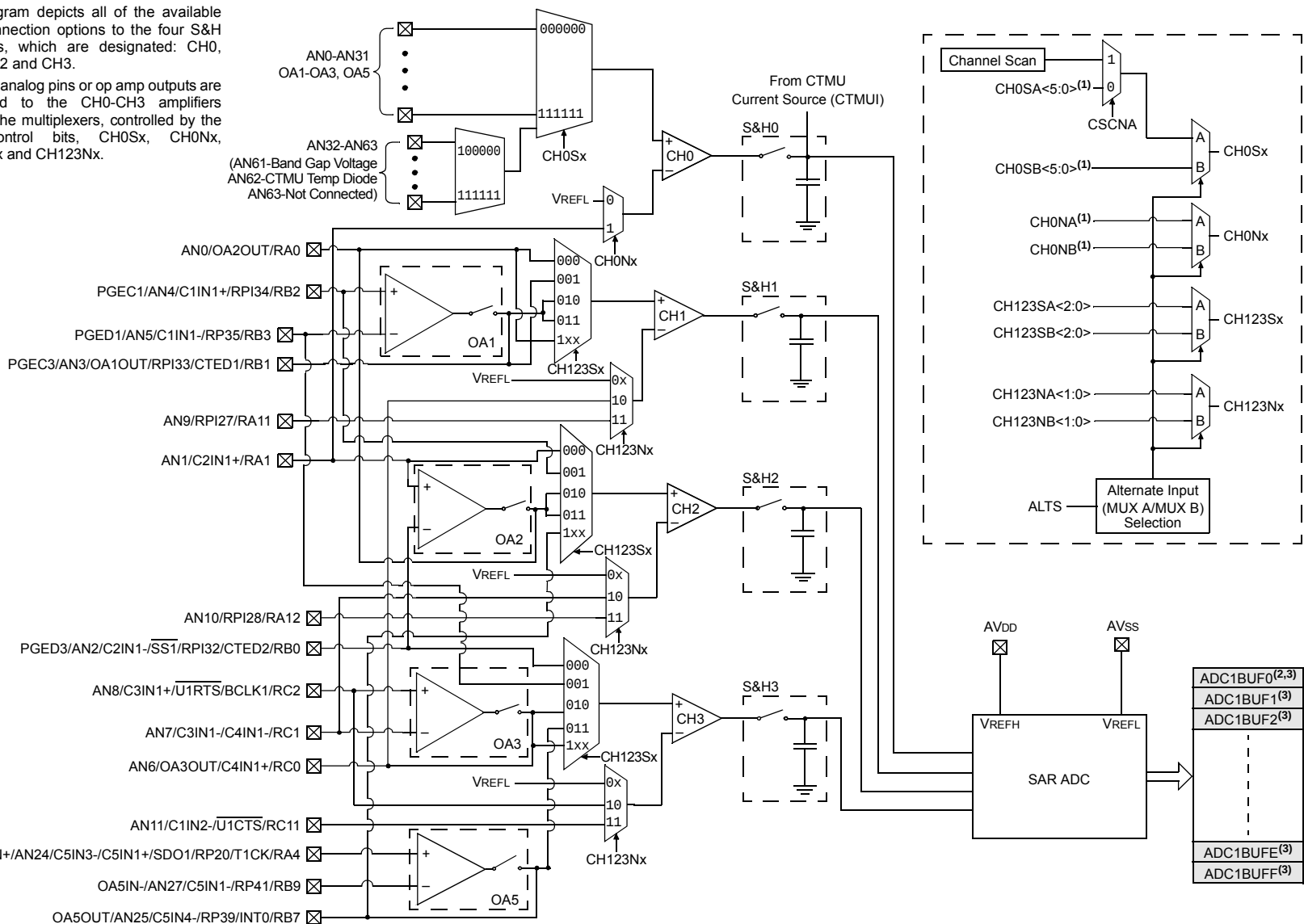
bit 5	ADDEN: Address Character Detect bit (bit 8 of received data = 1) 1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect 0 = Address Detect mode is disabled
bit 4	RIDLE: Receiver Idle bit (read-only) 1 = Receiver is Idle 0 = Receiver is active
bit 3	PERR: Parity Error Status bit (read-only) 1 = Parity error has been detected for the current character (character at the top of the receive FIFO) 0 = Parity error has not been detected
bit 2	FERR: Framing Error Status bit (read-only) 1 = Framing error has been detected for the current character (character at the top of the receive FIFO) 0 = Framing error has not been detected
bit 1	OERR: Receive Buffer Overrun Error Status bit (clear/read-only) 1 = Receive buffer has overflowed 0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receive buffer and the UxRSR to the empty state
bit 0	URXDA: UARTx Receive Buffer Data Available bit (read-only) 1 = Receive buffer has data, at least one more character can be read 0 = Receive buffer is empty

Note 1: Refer to “Universal Asynchronous Receiver Transmitter (UART)” (DS70000582) in the “dsPIC33/PIC24 Family Reference Manual” for information on enabling the UART module for transmit operation.

FIGURE 24-1: ADCx MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CH0Nx, CH123Sx and CH123Nx.



- Note 1:** Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
Note 2: When ADDMAEN (ADxCON4<8>) = 0, ADC1BUF0-ADC1BUFF are used.
Note 3: When ADDMAEN (ADxCON4<8>) = 1 enabling DMA, only ADC1BUF0 is used.

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3	ABEN: AND Gate B Input Enable bit 1 = MBI is connected to AND gate 0 = MBI is not connected to AND gate
bit 2	ABNEN: AND Gate B Input Inverted Enable bit 1 = Inverted MBI is connected to AND gate 0 = Inverted MBI is not connected to AND gate
bit 1	AAEN: AND Gate A Input Enable bit 1 = MAI is connected to AND gate 0 = MAI is not connected to AND gate
bit 0	AANEN: AND Gate A Input Inverted Enable bit 1 = Inverted MAI is connected to AND gate 0 = Inverted MAI is not connected to AND gate

dsPIC33EVXXXGM00X/10X FAMILY

**FIGURE 30-21: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1)
TIMING CHARACTERISTICS**

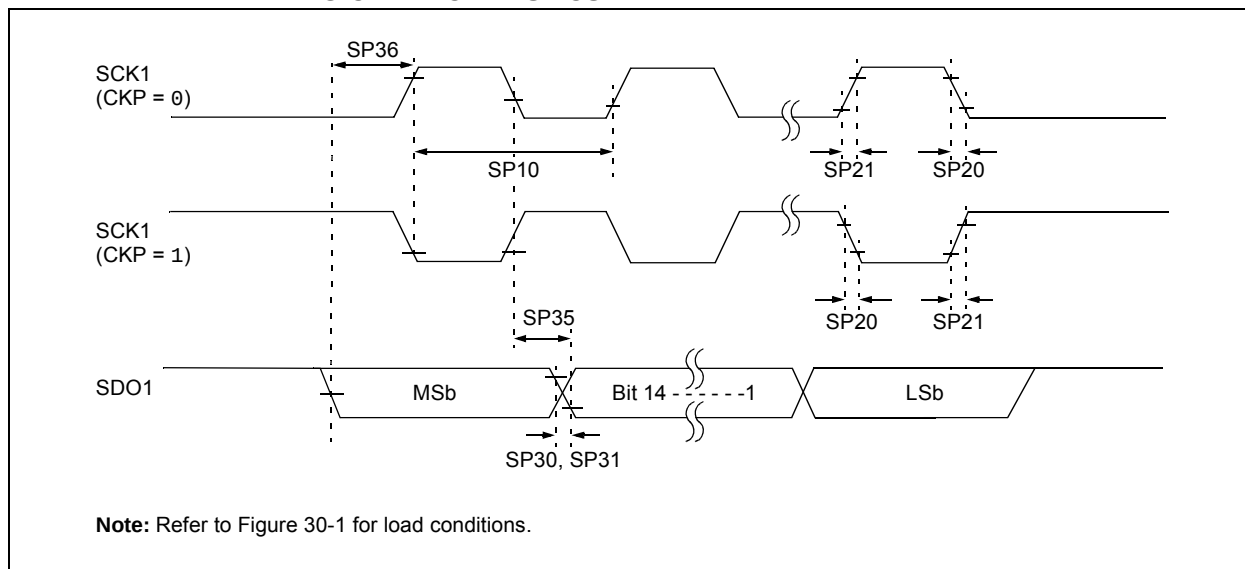


TABLE 30-39: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See Note 3
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2sch, TdiV2scl	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	

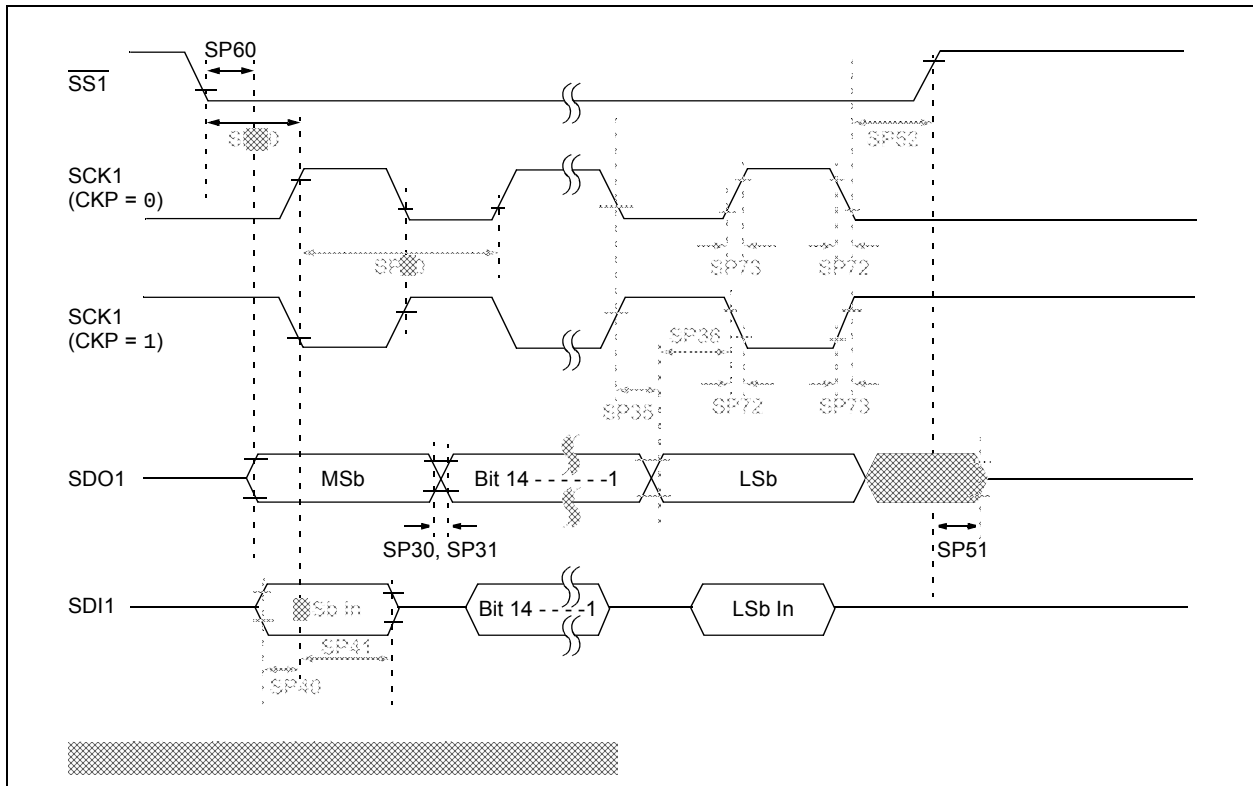
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-24: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



APPENDIX A: REVISION HISTORY

Revision A (December 2013)

This is the initial version of this document.

Revision B (June 2014)

This revision incorporates the following updates:

- Sections:
 - Added **Section 31.0 “High-Temperature Electrical Characteristics”**
 - Updated the “**Power Management**” section, the “**Input/Output**” section, **Section 3.3 “Data Space Addressing”**, **Section 4.2 “Data Address Space”**, **Section 4.3.2 “Extended X Data Space”**, **Section 4.6.1 “Bit-Reversed Addressing Implementation”**, **Section 7.4.1 “INTCON1 through INTCON4”**, **Section 11.7 “I/O Helpful Tips”**
 - Updated note in **Section 17.0 “High-Speed PWM Module”**, **Section 18.0 “Serial Peripheral Interface (SPI)”**, **Section 27.8 “Code Protection and CodeGuard™ Security”**
 - Updated title of **Section 20.0 “Single-Edge Nibble Transmission (SENT)”**
 - Updated **Section 34.0 “Packaging Information”**. Deleted e3, Pb-free and Industrial (I) temperature range indication throughout the section, and updated the packaging diagrams
 - Updated the “**Product Identification System**” section
- Registers:
 - Updated Register 3-2, Register 7-2, Register 7-6, Register 9-2, Register 11-3, Register 14-1, Register 14-3, Register 14-11, Register 15-1, Register 22-4
- Figures:
 - Added Figure 4-6, Figure 4-8, Figure 4-14, Figure 4-15, Figure 14-1, Figure 16-1, Figure 17-2, Figure 23-1, Figure 24-1
- Tables:
 - Updated Table 1, Table 27-1, Table 27-2, Table 30-6, Table 30-7, Table 30-8, Table 30-9, Table 30-10, Table 30-11, Table 30-12, Table 30-38, Table 30-50, Table 30-53 and added Table 31-11,
- Changes to text and formatting were incorporated throughout the document

Revision C (November 2014)

This revision incorporates the following updates:

- Sections:
 - Added note in **Section 5.2 “RTSP Operation”**
 - Updated “**Section 5.4 “Error Correcting Code (ECC)”**”
 - Deleted 44-Terminal Very Thin Leadless Array Package (TL) - 6x6x0.9 mm Body With Exposed Pad (VTLA).
- Registers
 - Updated Register 7-6
- Figures:
 - Updated Figure 4-1, Figure 4-3, Figure 4-4
- Tables:
 - Updated Table 27-2, Table 31-13, Table 31-14, Table 31-15
 - Added Table 31-16, Table 31-17

Revision D (April 2015)

This revision incorporates the following updates:

- Sections:
 - Updated the Clock Management, Timers/ Output Compare/Input Capture, Communication Interfaces and Input/Output sections at the beginning of the data sheet (Page 1 and Page 2).
 - Updated all pin diagrams at the beginning of the data sheet (Page 4 through Page 9).
 - Added **Section 11.6 “High-Voltage Detect (HVD)”**
 - Updated **Section 13.0 “Timer2/3 and Timer4/5”**
 - Corrects all Buffer heading numbers in **Section 22.4 “CAN Message Buffers”**
- Registers
 - Updated Register 3-2, Register 25-2, Register 26-2
- Figures
 - Updated Figure 26-1, Figure 30-5, Figure 30-32
- Tables
 - Updated Table 1, Table 4-25, Table 30-10, Table 30-22, Table 30-53 and Table 31-8
- Changes to text and formatting were incorporated throughout the document

dsPIC33EVXXXGM00X/10X FAMILY

SENTx Module	238
Shared I/O Port Structure	143
SPlx Module	222
Type B Timer (Timer2 and Timer4)	176
Type B/Type C Timer Pair (32-Bit Timer)	177
Type C Timer (Timer3 and Timer5)	176
UARTx Module	247
User-Programmable Blanking Function	302
Watchdog Timer (WDT)	325
Brown-out Reset (BOR)	324

C

C Compilers	
MPLAB XC	338
CAN	
CAN Module	
Control Registers	255
Message Buffers	275
Word 0	275
Word 1	275
Word 2	276
Word 3	276
Word 4	277
Word 5	277
Word 6	278
Word 7	278
Modes of Operation	254
Overview	253
Characteristics for High-Temperature	
Devices (+150°C)	439
Characteristics for Industrial/Extended Temperature	
Devices (-40°C to +125°C)	413
Charge Time Measurement Unit (CTMU)	279
Charge Time Measurement Unit. See CTMU.	
Code Examples	
Port Write/Read	144
PORTA Slew Selections	145
PWM1 Write-Protected Register	
Unlock Sequence	200
PWSAV Instruction Syntax	133
Code Protection	317, 326
CodeGuard Security	317, 326
Comparator Voltage Reference	
Configuring	313
Control Registers	315
Configuration Bits	317
Description	320
Controller Area Network (CAN)	253
Controller Area Network. See CAN.	
CPU	21
Addressing Modes	21
Arithmetic Logic Unit (ALU)	30
Control Registers	25
Data Space Addressing	21
DSP Engine	30
Instruction Set	21
Programmer's Model	23
CTMU	
Control Registers	281
Customer Change Notification Service	493
Customer Notification Service	493
Customer Support	493

D

Data Address Space	36
Alignment	36
Memory Map for 256-Kbyte Devices	39
Memory Map for 32-Kbyte Devices	37
Memory Map for 64/128-Kbyte Devices	38
Near Data Space	36
SFR Space	36
Width	36
Data Space	
Extended X	72
Memory Arbitration, Bus Master Priority	73
Paged Memory Scheme	68
DC Characteristics	342
Brown-out Reset (BOR)	349
CTMU Current Source	394
Doze Current (IDOZE)	347
Filter Capacitor (CEFC) Specifications	343
High Temperature	404
Brown-out Reset (BOR)	407
CTMU Current Source	410
I/O Pin Input Specifications	406
I/O Pin Output Specifications	407
Idle Current (IDLE)	405
Op Amp/ Comparator x	411
Operating Current (IDD)	405
Operating MIPS vs. Voltage	404
Power-Down Current (IPD)	405
Program Memory	407
Temperature and Voltage Specifications	404
Doze Current (IDOZE)	405
I/O Pin Input Specifications	348
I/O Pin Output Specifications	349
Idle Current (IDLE)	345
Internal Band Gap Reference Voltage	350
Op Amp/Comparator x Specifications	392
Op Amp/Comparator x Voltage Reference	
Specifications	393
Operating Current (IDD)	344
Operating MIPS vs. Voltage	342
Power-Down Current (IPD)	346
Program Memory	350
Temperature and Voltage Specifications	343
Thermal Operating Conditions	342
Deadman Timer (DMT)	181
Control Registers	182
Deadman Timer. See DMT.	
Development Support	337
Direct Memory Access. See DMA.	
DMA Controller	
Channel to Peripheral Associations	110
Control Registers	111
Supported Peripherals	109
DMAC Registers	
DMAxCNT	111
DMAxCON	111
DMAxPAD	111
DMAxREQ	111
DMAxSTAHL	111
DMAxSTBHL	111
DMT	
Doze Mode	135

dsPIC33EVXXXGM00X/10X FAMILY

CxFMSKSEL1 (CANx Filters 7-0 Mask Selection 1).....	269
CxFMSKSEL2 (CANx Filters 15-8 Mask Selection 2).....	270
CxINTE (CANx Interrupt Enable).....	261
CxINTF (CANx Interrupt Flag).....	260
CxRXFnEID (CANx Acceptance Filter n Extended Identifier).....	268
CxRXFnSID (CANx Acceptance Filter n Standard Identifier).....	268
CxRXFUL1 (CANx Receive Buffer Full 1).....	272
CxRXFUL2 (CANx Receive Buffer Full 2).....	272
CxRXMnEID (CANx Acceptance Filter Mask n Extended Identifier).....	271
CxRXMnSID (CANx Acceptance Filter Mask n Standard Identifier).....	271
CxRXOVF1 (CANx Receive Buffer Overflow 1).....	273
CxRXOVF2 (CANx Receive Buffer Overflow 2).....	273
CxTRmnCON (CANx TX/RX Buffer mn Control).....	274
CxVEC (CANx Interrupt Code).....	257
DEVID (Device ID).....	323
DEVREV (Device Revision).....	323
DMALCA (DMA Last Channel Active Status).....	120
DMA PPS (DMA Ping-Pong Status).....	121
DMA PWC (DMA Peripheral Write Collision Status).....	118
DMA RQC (DMA Request Collision Status).....	119
DMAxCNT (DMA Channel x Transfer Count).....	116
DMAxCON (DMA Channel x Control).....	112
DMAxPAD (DMA Channel x Peripheral Address).....	116
DMAxREQ (DMA Channel x IRQ Select).....	113
DMAxSTAH (DMA Channel x Start Address A, High).....	114
DMAxSTAL (DMA Channel x Start Address A, Low).....	114
DMAxSTBH (DMA Channel x Start Address B, High).....	115
DMAxSTBL (DMA Channel x Start Address B, Low).....	115
DMTCLR (Deadman Timer Clear).....	183
DMTCNTH (Deadman Timer Count High).....	185
DMTCNTL (Deadman Timer Count Low).....	185
DMTCON (Deadman Timer Control).....	182
DMTHOLDREG (DMT Hold).....	188
DMTPRECLR (Deadman Timer Preclear).....	182
DMTPSCNTH (DMT Post Configure Count Status High).....	186
DMTPSCNTL (DMT Post Configure Count Status Low).....	186
DMTPSINTVH (DMT Post Configure Interval Status High).....	187
DMTPSINTVL (DMT Post Configure Interval Status Low).....	187
DMTSTAT (Deadman Timer Status).....	184
DSADRH (DMA Most Recent RAM High Address).....	117
DSADRL (DMA Most Recent RAM Low Address).....	117
DTRx (PWMx Dead-Time).....	211
FCLCONx (PWMx Fault Current-Limit Control).....	215
I2CxCON1 (I2Cx Control 1).....	231
I2CxCON2 (I2Cx Control 2).....	233

I2CxMSK (I2Cx Slave Mode Address Mask).....	235
I2CxSTAT (I2Cx Status).....	234
ICxCON1 (Input Capture x Control 1).....	190
ICxCON2 (Input Capture x Control 2).....	191
INTCON1 (Interrupt Control 1).....	103
INTCON2 (Interrupt Control 2).....	105
INTCON3 (Interrupt Control 3).....	106
INTCON4 (Interrupt Control 4).....	107
INTTREG (Interrupt Control and Status).....	108
IOCONx (PWMx I/O Control).....	213
LEBCONx (PWMx Leading-Edge Blanking Control).....	217
LEBDLYx (PWMx Leading-Edge Blanking Delay).....	218
MDC (PWMx Master Duty Cycle).....	207
NVMADR (NVM Lower Address).....	88
NVMADRU (NVM Upper Address).....	88
NVMCON (NVM Control).....	86
NVMKEY (NVM Key).....	89
NVMSRCADRH (NVM Data Memory Upper Address).....	90
NVMSRCADRL (NVM Data Memory Lower Address).....	90
OCxCON1 (Output Compare x Control 1).....	194
OCxCON2 (Output Compare x Control 2).....	196
OSCCON (Oscillator Control).....	126
OSCTUN (FRC Oscillator Tuning).....	131
PDCx (PWMx Generator Duty Cycle).....	210
PHASEx (PWMx Primary Phase-Shift).....	210
PLLFBF (PLL Feedback Divisor).....	130
PMD1 (Peripheral Module Disable Control 1).....	136
PMD2 (Peripheral Module Disable Control 2).....	137
PMD3 (Peripheral Module Disable Control 3).....	138
PMD4 (Peripheral Module Disable Control 4).....	138
PMD6 (Peripheral Module Disable Control 6).....	139
PMD7 (Peripheral Module Disable Control 7).....	140
PMD8 (Peripheral Module Disable Control 8).....	141
PTCON (PWMx Time Base Control).....	204
PTCON2 (PWMx Primary Master Clock Divider Select).....	205
PTPER (PWMx Primary Master Time Base Period).....	206
PWMCONx (PWMx Control).....	208
RCON (Reset Control).....	93
REFOCON (Reference Oscillator Control).....	132
RPINR0 (Peripheral Pin Select Input 0).....	153
RPINR1 (Peripheral Pin Select Input 1).....	153
RPINR11 (Peripheral Pin Select Input 11).....	157
RPINR12 (Peripheral Pin Select Input 12).....	158
RPINR18 (Peripheral Pin Select Input 18).....	159
RPINR19 (Peripheral Pin Select Input 19).....	159
RPINR22 (Peripheral Pin Select Input 22).....	160
RPINR23 (Peripheral Pin Select Input 23).....	161
RPINR26 (Peripheral Pin Select Input 26).....	161
RPINR3 (Peripheral Pin Select Input 3).....	154
RPINR37 (Peripheral Pin Select Input 37).....	162
RPINR38 (Peripheral Pin Select Input 38).....	162
RPINR39 (Peripheral Pin Select Input 39).....	163
RPINR44 (Peripheral Pin Select Input 44).....	164
RPINR45 (Peripheral Pin Select Input 45).....	164
RPINR7 (Peripheral Pin Select Input 7).....	155
RPINR8 (Peripheral Pin Select Input 8).....	156
RPOR0 (Peripheral Pin Select Output 0).....	165
RPOR1 (Peripheral Pin Select Output 1).....	165
RPOR10 (Peripheral Pin Select Output 10).....	170