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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm002-e-ss

TABLE 4-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM006/106 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR5	067A	—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0	0000
RPOR6	067C	—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0	0000
RPOR7	067E	—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0	0000
RPOR8	0680	—	—	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0	—	—	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0	0000
RPOR9	0682	—	—	RP118R5	RP118R4	RP118R3	RP118R2	RP118R1	RP118R0	—	—	RP97R5	RP97R4	RP97R3	RP97R2	RP97R1	RP97R0	0000
RPOR10	0684	—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0	—	—	RP120R5	RP120R4	RP120R3	RP120R2	RP120R1	RP120R0	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-22: PMD REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD ⁽¹⁾	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	—	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	—	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					
PMD8	076E	—	—	—	SENT2MD	SENT1MD	—	—	DMTMD	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

TABLE 4-25: OP AMP/COMPARATOR REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	C5EVT	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVR1CON	0A82	CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—	—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM1MSKSR	0A86	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBENEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM2MSKSR	0A8E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBENEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM3CON	0A94	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM3MSKSR	0A96	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBENEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM4MSKSR	0A9E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBENEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM5CON	0AA4	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM5MSKSR	0AA6	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM5MSKCON	0AA8	HLMS	—	OCEN	OCNEN	OBEN	OBENEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM5FLTR	0AAA	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CVR2CON	0AB4	CVREN	CVROE ⁽¹⁾	—	—	CVRSS	VREFSEL	—	—	—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: CVROE (CVR2CON<14>) is not available on 28-pin devices.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE ⁽¹⁾	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0
bit 7							bit 0

Legend:	S = Settable bit
R = Readable bit	W = Writable bit
-n = Value at POR	'1' = Bit is set
	'0' = Bit is cleared
	x = Bit is unknown

- bit 15 **FORCE:** Force DMA Transfer bit⁽¹⁾
 1 = Forces a single DMA transfer (Manual mode)
 0 = Automatic DMA transfer initiation by DMA request
- bit 14-8 **Unimplemented:** Read as '0'
- bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits
 01000110 = TX data request (CAN1)⁽²⁾
 00100110 = Input Capture 4 (IC4)
 00100101 = Input Capture 3 (IC3)
 00100010 = RX data ready (CAN1)
 00100001 = SPI2 transfer done (SPI2)
 00011111 = UART2 Transmitter (UART2TX)
 00011110 = UART2 Receiver (UART2RX)
 00011100 = Timer5 (TMR5)
 00011011 = Timer4 (TMR4)
 00011010 = Output Compare 4 (OC4)
 00011001 = Output Compare 3 (OC3)
 00001101 = ADC1 convert done (ADC1)
 00001100 = UART1 Transmitter (UART1TX)
 00001011 = UART1 Receiver (UART1RX)
 00001010 = SPI1 transfer done (SPI1)
 00001000 = Timer3 (TMR3)
 00000111 = Timer2 (TMR2)
 00000110 = Output Compare 2 (OC2)
 00000101 = Input Capture 2 (IC2)
 00000010 = Output Compare 1 (OC1)
 00000001 = Input Capture 1 (IC1)
 00000000 = External Interrupt 0 (INT0)

- Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).
- 2:** This select bit is only available on dsPIC33EVXXXGM10X devices.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH<3:0>			
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4

Unimplemented: Read as '0'

bit 3-0

LSTCH<3:0>: Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset

1110 = Reserved

•

•

•

0100 = Reserved

0011 = Last data transfer was handled by Channel 3

0010 = Last data transfer was handled by Channel 2

0001 = Last data transfer was handled by Channel 1

0000 = Last data transfer was handled by Channel 0

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit

1 = DMA3STB register is selected

0 = DMA3STA register is selected

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit

1 = DMA2STB register is selected

0 = DMA2STA register is selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit

1 = DMA1STB register is selected

0 = DMA1STA register is selected

bit 0 **PPST0:** Channel 0 Ping-Pong mode Status Flag bit

1 = DMA0STB register is selected

0 = DMA0STA register is selected

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment
000 0000	I	Vss	011 0010	I	RPI50
000 0001	I	CMP1 ⁽¹⁾	011 0011	I	RPI51
000 0010	I	CMP2 ⁽¹⁾	011 0100	I	RPI52
000 0011	I	CMP3 ⁽¹⁾	011 0101	I	RPI53
000 0100	I	CMP4 ⁽¹⁾	011 0110	I/O	RP54
000 0101	—	—	011 0111	I/O	RP55
000 1100	I	CMP5 ⁽¹⁾	011 1000	I/O	RP56
000 1101	—	—	011 1001	I/O	RP57
000 1110	—	—	011 1010	I	RPI58
000 1111	—	—	011 1011	—	—
001 0000	I	RPI16	011 1100	I	RPI60
001 0001	I	RPI17	011 1101	I	RPI61
001 0010	I	RPI18	011 1110	—	—
001 0011	I	RPI19	011 1111	I	RPI 63
001 0100	I/O	RP20	100 0000	—	—
001 0101	—	—	100 0001	—	—
001 0110	—	—	100 0010	—	—
001 0111	—	—	100 0011	—	—
001 1000	I	RPI24	100 0100	—	—
001 1001	I	RPI25	100 0101	I/O	RP69
001 1010	—	—	100 0110	I/O	RP70
001 1011	I	RPI27	100 0111	—	—
001 1100	I	RPI28	100 1000	I	RPI72
001 1101	—	—	100 1001	—	—
001 1110	—	—	100 1010	—	—
001 1111	—	—	100 1011	—	—
010 0000	I	RPI32	100 1110	—	—
010 0001	I	RPI33	100 1111	—	—
010 0010	I	RPI34	101 0010	—	—
010 0011	I/O	RP35	101 0011	—	—
010 0100	I/O	RP36	101 0100	—	—
010 0101	I/O	RP37	010 1001	I/O	RP41
010 0110	I/O	RP38	010 1010	I/O	RP42
010 0111	I/O	RP39	010 1011	I/O	RP43
010 1000	I/O	RP40	101 1000	—	—
010 1100	I	RPI44	101 1001	—	—
010 1101	I	RPI45	101 1010	—	—
010 1110	I	RPI46	101 1011	—	—
010 1111	I	RPI47	101 1100	—	—
011 0000	I/O	RP48	101 1101	—	—

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

Note 1: These are virtual pins. See **Section 11.5.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

dsPIC33EVXXXGM00X/10X FAMILY

13.1 Timer2/3 and Timer4/5 Control Registers

REGISTER 13-1: TxCON (T2CON AND T4CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS ⁽¹⁾	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **TON:** Timerx On bit
 When T32 = 1:
 1 = Starts 32-bit Timerx/y
 0 = Stops 32-bit Timerx/y
 When T32 = 0:
 1 = Starts 16-bit Timerx
 0 = Stops 16-bit Timerx
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
 1 = Discontinues module operation when the device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12-7 **Unimplemented:** Read as '0'
- bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
 When TCS = 1:
 This bit is ignored.
 When TCS = 0:
 1 = Gated time accumulation is enabled
 0 = Gated time accumulation is disabled
- bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits
 11 = 1:256
 10 = 1:64
 01 = 1:8
 00 = 1:1
- bit 3 **T32:** 32-Bit Timer Mode Select bit
 1 = Timerx and Timery form a single 32-bit timer
 0 = Timerx and Timery act as two 16-bit timers
- bit 2 **Unimplemented:** Read as '0'
- bit 1 **TCS:** Timerx Clock Source Select bit⁽¹⁾
 1 = External clock is from pin, TxCK (on the rising edge)
 0 = Internal clock (Fp)
- bit 0 **Unimplemented:** Read as '0'

Note 1: The TxCK pin is not available on all timers. Refer to the “Pin Diagrams” section for the available pins.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 **SWAP**: SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pin; PWMxL output signal is connected to the PWMxH pin
0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 **OSYNC**: Output Override Synchronization bit
1 = Output overrides through the OVRDAT<1:0> bits are synchronized to the PWMx time base
0 = Output overrides through the OVRDAT<1:0> bits occur on the next CPU clock boundary

- Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOP<0>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 15-0 **TRGCMP<15:0>**: Trigger Control Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

20.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)

Note 1: This data sheet summarizes the features of this group of dsPIC33EVXXXGM00X/10X family devices. It is not intended to be a comprehensive reference source. For more information on Single-Edge Nibble Transmission, refer to “**Single-Edge Nibble Transmission (SENT) Module**” (DS70005145) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

20.1 Module Introduction

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, “*SENT – Single-Edge Nibble Transmission for Automotive Applications*”. The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- Selectable Transmit or Receive mode
- Synchronous or Asynchronous Transmit modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive mode
- Optional Hardware Calculation of CRC in Transmit mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive from 3 to 6 Nibbles
- Automatic Detection of Framing Errors

SENT protocol timing is based on a predetermined time unit, T_{TICK} . Both the transmitter and receiver must be preconfigured for T_{TICK} , which can vary from 3 to 90 μs . A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in T_{TICK} . This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are 4 bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 20-1 shows a block diagram of the SENTx module.

Figure 20-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SNTEN	—	SNTSIDL	—	RCVEN	TXM ⁽¹⁾	TXPOL ⁽¹⁾	CRCCEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PPP	SPCEN ⁽²⁾	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **SNTEN:** SENTx Enable bit
1 = SENTx is enabled
0 = SENTx is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **SNTSIDL:** SENTx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **Unimplemented:** Read as '0'
- bit 11 **RCVEN:** SENTx Receive Enable bit
1 = SENTx operates as a receiver
0 = SENTx operates as a transmitter (sensor)
- bit 10 **TXM:** SENTx Transmit Mode bit⁽¹⁾
1 = SENTx transmits data frame only when triggered using the SYNCTXEN status bit
0 = SENTx transmits data frames continuously while SNTEN = 1
- bit 9 **TXPOL:** SENTx Transmit Polarity bit⁽¹⁾
1 = SENTx data output pin is low in the Idle state
0 = SENTx data output pin is high in the Idle state
- bit 8 **CRCCEN:** CRC Enable bit
Module in Receive Mode (RCVEN = 1):
1 = SENTx performs CRC verification on received data using the preferred J2716 method
0 = SENTx does not perform CRC verification on received data
Module in Transmit Mode (RCVEN = 1):
1 = SENTx automatically calculates CRC using the preferred J2716 method
0 = SENTx does not calculate CRC
- bit 7 **PPP:** Pause Pulse Present bit
1 = SENTx is configured to transmit/receive SENT messages with pause pulse
0 = SENTx is configured to transmit/receive SENT messages without pause pulse
- bit 6 **SPCEN:** Short PWM Code Enable bit⁽²⁾
1 = SPC control from external source is enabled
0 = SPC control from external source is disabled
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **PS:** SENTx Module Clock Prescaler (divider) bits
1 = Divide-by-4
0 = Divide-by-1

Note 1: This bit has no function in Receive mode (RCVEN = 1).
2: This bit has no function in Transmit mode (RCVEN = 0).

21.2 UART Control Registers

REGISTER 21-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN ⁽¹⁾	—	USIDL	IREN ⁽²⁾	RTSMD	—	UEN1	UEN0
bit 15						bit 8	

R/W-0, HC	R/W-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **UARTEN:** UARTx Enable bit⁽¹⁾
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽²⁾
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches⁽³⁾
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and UxRTS pins are enabled and used⁽⁴⁾
01 = UxTX, UxRX and UxRTS pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches⁽⁴⁾
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ /BCLKx pins are controlled by PORT latches
- bit 7 **WAKE:** UARTx Wake-up on Start bit Detect During Sleep Mode Enable bit
1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
0 = Wake-up is not enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Loopback mode is enabled
0 = Loopback mode is disabled

Note 1: Refer to “Universal Asynchronous Receiver Transmitter (UART)” (DS70000582) in the “dsPIC33/PIC24 Family Reference Manual” for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This feature is only available on 44-pin and 64-pin devices.

4: This feature is only available on 64-pin devices.

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REGISTER 22-13: CxBUFPNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits 15-12)

bit 7-4 **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits 15-12)

bit 3-0 **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

26.2 Comparator Voltage Reference Registers

REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **CVREN:** Comparator Voltage Reference Enable bit
 1 = Comparator voltage reference circuit is powered on
 0 = Comparator voltage reference circuit is powered down
- bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF10 Pin) bit
 1 = Voltage level is output on the CVREF10 pin
 0 = Voltage level is disconnected from the CVREF10 pin
- bit 13-12 **Unimplemented:** Read as '0'
- bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
 1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
 0 = Comparator reference source, CVRSRC = AVDD – AVSS
- bit 10 **VREFSEL:** Voltage Reference Select bit
 1 = CVREFIN = CVREF+
 0 = CVREFIN is generated by the resistor network
- bit 9-7 **Unimplemented:** Read as '0'
- bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits
 1111111 = 127/128 x VREF input voltage
 •
 •
 •
 0000000 = 0.0 volts

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FIGURE 30-14: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS

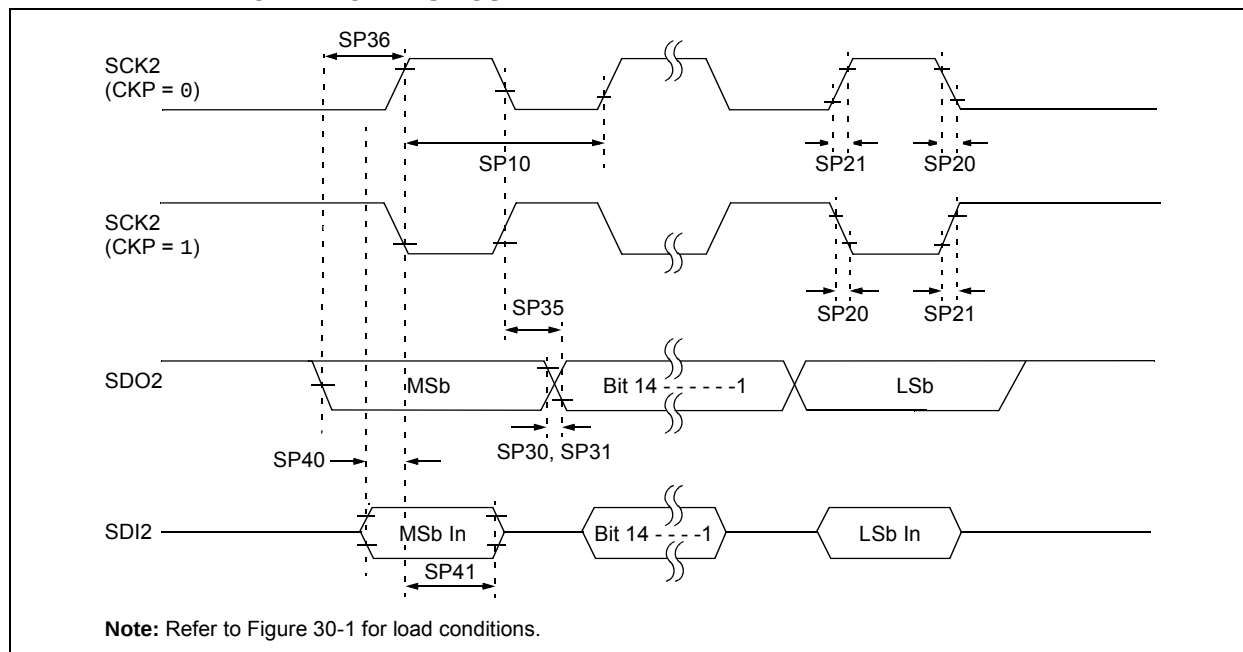


TABLE 30-32: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	See Note 3
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

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**TABLE 30-35: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	See Note 3
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2} \downarrow$ to SCK2 $\uparrow$ or SCK2 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2} \uparrow$ to SDO2 Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH TscL2ssH	$\overline{SS2} \uparrow$ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

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**TABLE 30-42: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See Note 3
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See Note 4
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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TABLE 30-47: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param. No.	Symbol	Characteristic ⁽³⁾		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	μs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	Device must operate at a minimum of 10 MHz
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽¹⁾	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽¹⁾	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽¹⁾	0	0.3	μs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.6	—	μs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	μs	
			400 kHz mode	0.6	—	μs	
			1 MHz mode ⁽¹⁾	0.25	—	μs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode ⁽¹⁾	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽¹⁾	0.5	—	μs	
IS50	Cb	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See Note 2

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

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CxFMSKSEL1 (CANx Filters 7-0 Mask Selection 1).....	269	I2CxMSK (I2Cx Slave Mode Address Mask).....	235
CxFMSKSEL2 (CANx Filters 15-8 Mask Selection 2).....	270	I2CxSTAT (I2Cx Status).....	234
CxINTE (CANx Interrupt Enable).....	261	ICxCON1 (Input Capture x Control 1).....	190
CxINTF (CANx Interrupt Flag).....	260	ICxCON2 (Input Capture x Control 2).....	191
CxRXFnEID (CANx Acceptance Filter n Extended Identifier).....	268	INTCON1 (Interrupt Control 1).....	103
CxRXFnSID (CANx Acceptance Filter n Standard Identifier).....	268	INTCON2 (Interrupt Control 2).....	105
CxRXFUL1 (CANx Receive Buffer Full 1).....	272	INTCON3 (Interrupt Control 3).....	106
CxRXFUL2 (CANx Receive Buffer Full 2).....	272	INTCON4 (Interrupt Control 4).....	107
CxRXMnEID (CANx Acceptance Filter Mask n Extended Identifier).....	271	INTTREG (Interrupt Control and Status).....	108
CxRXMnSID (CANx Acceptance Filter Mask n Standard Identifier).....	271	IOCONx (PWMx I/O Control).....	213
CxRXOVF1 (CANx Receive Buffer Overflow 1).....	273	LEBCONx (PWMx Leading-Edge Blanking Control).....	217
CxRXOVF2 (CANx Receive Buffer Overflow 2).....	273	LEBDLYx (PWMx Leading-Edge Blanking Delay).....	218
CxTRmnCON (CANx TX/RX Buffer mn Control).....	274	MDC (PWMx Master Duty Cycle).....	207
CxVEC (CANx Interrupt Code).....	257	NVMADR (NVM Lower Address).....	88
DEVID (Device ID).....	323	NVMADRU (NVM Upper Address).....	88
DEVREV (Device Revision).....	323	NVMCON (NVM Control).....	86
DMALCA (DMA Last Channel Active Status).....	120	NVMKEY (NVM Key).....	89
DMA PPS (DMA Ping-Pong Status).....	121	NVMSRCADRH (NVM Data Memory Upper Address).....	90
DMA PWC (DMA Peripheral Write Collision Status).....	118	NVMSRCADRL (NVM Data Memory Lower Address).....	90
DMA RQC (DMA Request Collision Status).....	119	OCxCON1 (Output Compare x Control 1).....	194
DMAxCNT (DMA Channel x Transfer Count).....	116	OCxCON2 (Output Compare x Control 2).....	196
DMAxCON (DMA Channel x Control).....	112	OSCCON (Oscillator Control).....	126
DMAxPAD (DMA Channel x Peripheral Address).....	116	OSCTUN (FRC Oscillator Tuning).....	131
DMAxREQ (DMA Channel x IRQ Select).....	113	PDCx (PWMx Generator Duty Cycle).....	210
DMAxSTAH (DMA Channel x Start Address A, High).....	114	PHASEx (PWMx Primary Phase-Shift).....	210
DMAxSTAL (DMA Channel x Start Address A, Low).....	114	PLLFBF (PLL Feedback Divisor).....	130
DMAxSTBH (DMA Channel x Start Address B, High).....	115	PMD1 (Peripheral Module Disable Control 1).....	136
DMAxSTBL (DMA Channel x Start Address B, Low).....	115	PMD2 (Peripheral Module Disable Control 2).....	137
DMTCLR (Deadman Timer Clear).....	183	PMD3 (Peripheral Module Disable Control 3).....	138
DMTCNTH (Deadman Timer Count High).....	185	PMD4 (Peripheral Module Disable Control 4).....	138
DMTCNTL (Deadman Timer Count Low).....	185	PMD6 (Peripheral Module Disable Control 6).....	139
DMTCON (Deadman Timer Control).....	182	PMD7 (Peripheral Module Disable Control 7).....	140
DMTHOLDREG (DMT Hold).....	188	PMD8 (Peripheral Module Disable Control 8).....	141
DMTPRECLR (Deadman Timer Preclear).....	182	PTCON (PWMx Time Base Control).....	204
DMTPSCNTH (DMT Post Configure Count Status High).....	186	PTCON2 (PWMx Primary Master Clock Divider Select).....	205
DMTPSCNTL (DMT Post Configure Count Status Low).....	186	PTPER (PWMx Primary Master Time Base Period).....	206
DMTPSINTVH (DMT Post Configure Interval Status High).....	187	PWMCONx (PWMx Control).....	208
DMTPSINTVL (DMT Post Configure Interval Status Low).....	187	RCON (Reset Control).....	93
DMTSTAT (Deadman Timer Status).....	184	REFOCON (Reference Oscillator Control).....	132
DSADRH (DMA Most Recent RAM High Address).....	117	RPINR0 (Peripheral Pin Select Input 0).....	153
DSADRL (DMA Most Recent RAM Low Address).....	117	RPINR1 (Peripheral Pin Select Input 1).....	153
DTRx (PWMx Dead-Time).....	211	RPINR11 (Peripheral Pin Select Input 11).....	157
FCLCONx (PWMx Fault Current-Limit Control).....	215	RPINR12 (Peripheral Pin Select Input 12).....	158
I2CxCON1 (I2Cx Control 1).....	231	RPINR18 (Peripheral Pin Select Input 18).....	159
I2CxCON2 (I2Cx Control 2).....	233	RPINR19 (Peripheral Pin Select Input 19).....	159
		RPINR22 (Peripheral Pin Select Input 22).....	160
		RPINR23 (Peripheral Pin Select Input 23).....	161
		RPINR26 (Peripheral Pin Select Input 26).....	161
		RPINR3 (Peripheral Pin Select Input 3).....	154
		RPINR37 (Peripheral Pin Select Input 37).....	162
		RPINR38 (Peripheral Pin Select Input 38).....	162
		RPINR39 (Peripheral Pin Select Input 39).....	163
		RPINR44 (Peripheral Pin Select Input 44).....	164
		RPINR45 (Peripheral Pin Select Input 45).....	164
		RPINR7 (Peripheral Pin Select Input 7).....	155
		RPINR8 (Peripheral Pin Select Input 8).....	156
		RPOR0 (Peripheral Pin Select Output 0).....	165
		RPOR1 (Peripheral Pin Select Output 1).....	165
		RPOR10 (Peripheral Pin Select Output 10).....	170