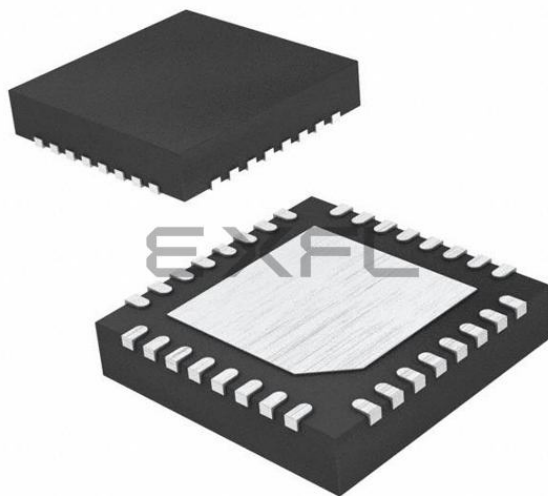




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

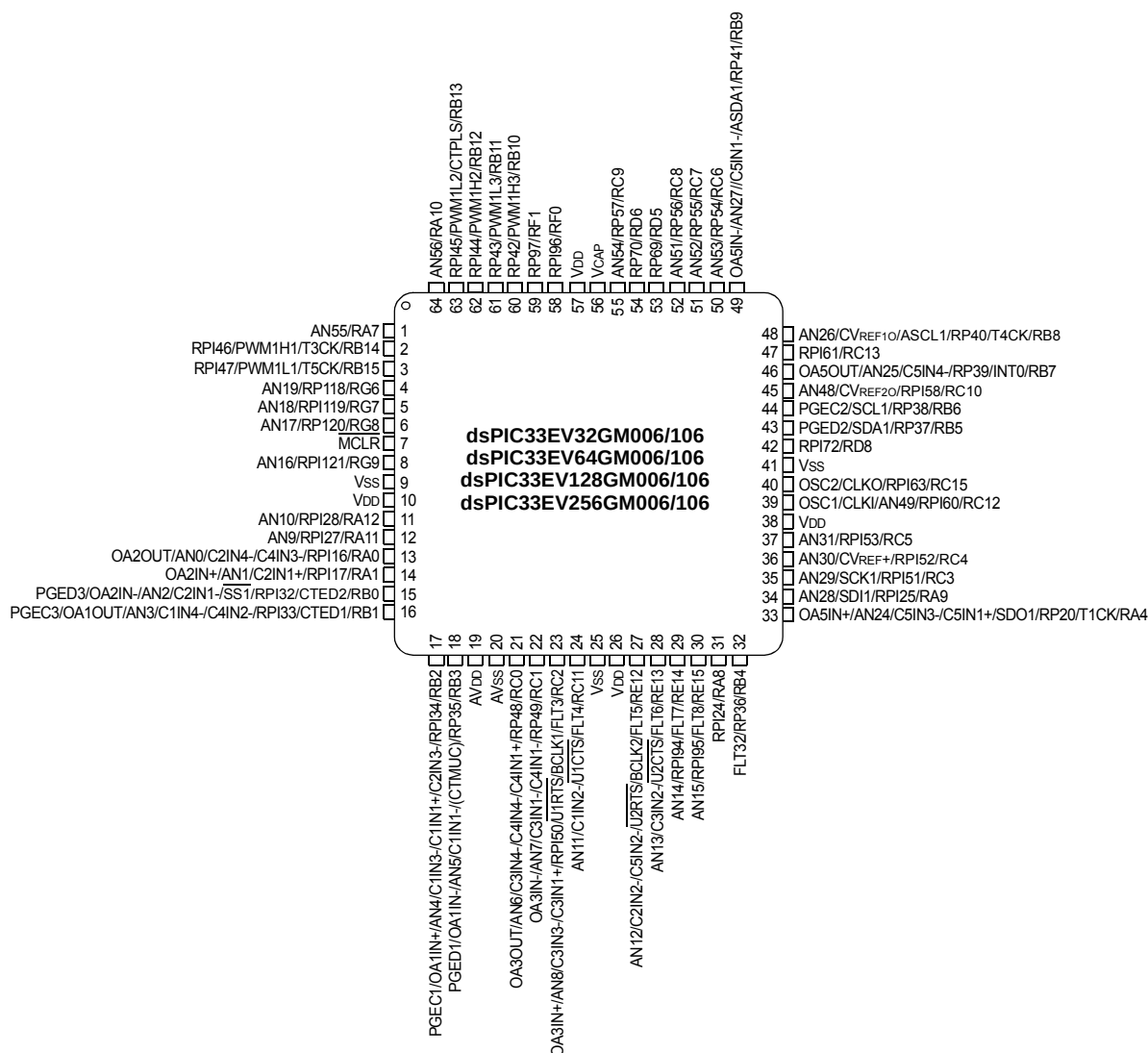
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm002-i-mm

dsPIC33EVXXXGM00X/10X FAMILY

Pin Diagrams (Continued)

64-Pin TQFP^(1,2,3)



- Note 1:** The RPN/RPI pins can be used by any remappable peripheral with some limitation. See **Section 11.5 “Peripheral Pin Select (PPS)”** for available peripherals and information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
W0	0000	W0 (WREG)																0000	
W1	0002	W1																0000	
W2	0004	W2																0000	
W3	0006	W3																0000	
W4	0008	W4																0000	
W5	000A	W5																0000	
W6	000C	W6																0000	
W7	000E	W7																0000	
W8	0010	W8																0000	
W9	0012	W9																0000	
W10	0014	W10																0000	
W11	0016	W11																0000	
W12	0018	W12																0000	
W13	001A	W13																0000	
W14	001C	W14																0000	
W15	001E	W15																0800	
SPLIM	0020	SPLIM																xxxx	
ACCAL	0022	ACCAL																xxxx	
ACCAH	0024	ACCAH																xxxx	
ACCAU	0026	Sign Extension of ACCA<39>									ACCAU							xxxx	
ACCBH	0028	ACCBH																xxxx	
ACCBH	002A	ACCBH																xxxx	
ACCBU	002C	Sign Extension of ACCB<39>									ACCBU							xxxx	
PCL	002E	Program Counter Low Word Register																—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register							0000	
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										0001	
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register										0001
RCOUNT	0036	REPEAT Loop Counter Register																0	xxxx
DCOUNT	0038	DCOUNT<15:1>																0	xxxx
DOSTARTL	003A	DOSTARTL<15:1>																0	xxxx
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH<5:0>					00xx		
DOENDL	003E	DOENDL<15:1>																—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11SID	046C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF11EID	046E	EID<15:0>																xxxx
C1RXF12SID	0470	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF12EID	0472	EID<15:0>																xxxx
C1RXF13SID	0474	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF13EID	0476	EID<15:0>																xxxx
C1RXF14SID	0478	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF14EID	047A	EID<15:0>																xxxx
C1RXF15SID	047C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF15EID	047E	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: SENT1 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT1CON1	0500	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT1CON2	0504	TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode)																FFFF
SENT1CON3	0508	FRAMETIME<15:0> (Transmit modes) or SYNCMIN<15:0> (Receive mode)																FFFF
SENT1STAT	050C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT1SYNC	0510	Synchronization Time Period Register (Transmit mode)																0000
SENT1DATL	0514	DATA4<3:0>				DATA5<3:0>				DATA6<3:0>				CRC<3:0>				0000
SENT1DATH	0516	STAT<3:0>				DATA1<3:0>				DATA2<3:0>				DATA3<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: SENT2 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT2CON1	0520	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT2CON2	0524	TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode)																FFFF
SENT2CON3	0528	FRAMETIME<15:0> (Transmit modes) or SYNCMIN<15:0> (Receive mode)																FFFF
SENT2STAT	052C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT2SYNC	0530	Synchronization Time Period Register (Transmit mode)																0000
SENT2DATL	0534	DATA4<3:0>				DATA5<3:0>				DATA6<3:0>				CRC<3:0>				0000
SENT2DATH	0536	STAT<3:0>				DATA1<3:0>				DATA2<3:0>				DATA3<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-26: DMAC REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA0REQ	0B02	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA0STAL	0B04	STA<15:0>																0000
DMA0STAH	0B06	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA0STBL	0B08	STB<15:0>																0000
DMA0STBH	0B0A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA0PAD	0B0C	PAD<15:0>																0000
DMA0CNT	0B0E	—	—	CNT<13:0>														0000
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA1REQ	0B12	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA1STAL	0B14	STA<15:0>																0000
DMA1STAH	0B16	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA1STBL	0B18	STB<15:0>																0000
DMA1STBH	0B1A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA1PAD	0B1C	PAD<15:0>																0000
DMA1CNT	0B1E	—	—	CNT<13:0>														0000
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA2REQ	0B22	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA2STAL	0B24	STA<15:0>																0000
DMA2STAH	0B26	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA2STBL	0B28	STB<15:0>																0000
DMA2STBH	0B2A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA2PAD	0B2C	PAD<15:0>																0000
DMA2CNT	0B2E	—	—	CNT<13:0>														0000
DMA3CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA3REQ	0B32	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA3STAL	0B34	STA<15:0>																0000
DMA3STAH	0B36	—	—	—	—	—	—	—	—	STA<23:16>								0000
DMA3STBL	0B38	STB<15:0>																0000
DMA3STBH	0B3A	—	—	—	—	—	—	—	—	STB<23:16>								0000
DMA3PAD	0B3C	PAD<15:0>																0000
DMA3CNT	0B3E	—	—	CNT<13:0>														0000
DMA3PWC	0BF0	—	—	—	—	—	—	—	—	—	—	—	—	PWCOL<3:0>				0000
DMA3RQC	0BF2	—	—	—	—	—	—	—	—	—	—	—	—	RQCOL<3:0>				0000
DMA3PPS	0BF4	—	—	—	—	—	—	—	—	—	—	—	—	PPST<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 7-2: dsPIC33EVXXXGM00X/10X FAMILY INTERRUPT VECTOR TABLE

Reset – GOTO Instruction	0x000000
Reset – GOTO Address	0x000002
Oscillator Fail Trap Vector	0x000004
Address Error Trap Vector	0x000006
Generic Hard Trap Vector	0x000008
Stack Error Trap Vector	0x00000A
Math Error Trap Vector	0x00000C
DMAC Error Trap Vector	0x00000E
Generic Soft Trap Vector	0x000010
Reserved	0x000012
Interrupt Vector 0	0x000014
Interrupt Vector 1	0x000016
:	:
:	:
:	:
Interrupt Vector 52	0x00007C
Interrupt Vector 53	0x00007E
Interrupt Vector 54	0x000080
:	:
:	:
:	:
Interrupt Vector 116	0x0000FC
Interrupt Vector 117	0x0000FE
Interrupt Vector 118	0x000100
Interrupt Vector 119	0x000102
Interrupt Vector 120	0x000104
:	:
:	:
:	:
Interrupt Vector 244	0x0001FC
Interrupt Vector 245	0x0001FE
START OF CODE	0x000200

Decreasing Natural Order Priority

IVT

See Table 7-1 for Interrupt Vector Details

dsPIC33EVXXXGM00X/10X FAMILY

Table 9-1 provides the Configuration bits which allow users to choose between the various clock modes.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>
Fast RC Oscillator with Divide-by-N (FRCDIVN) ^(1,2)	Internal	xx	111
Fast RC Oscillator with Divide-by-16 (FRCDIV16) ⁽¹⁾	Internal	xx	110
Low-Power RC Oscillator (LPRC) ⁽¹⁾	Internal	xx	101
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011
Primary Oscillator (EC) with PLL (ECPLL) ⁽¹⁾	Primary	00	011
Primary Oscillator (HS)	Primary	10	010
Primary Oscillator (XT)	Primary	01	010
Primary Oscillator (EC) ⁽¹⁾	Primary	00	010
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL) ⁽¹⁾	Internal	xx	001
Fast RC Oscillator (FRC) ⁽¹⁾	Internal	xx	000

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/Output	Pin Assignment
000 0000	I	Vss	011 0010	I	RPI50
000 0001	I	CMP1 ⁽¹⁾	011 0011	I	RPI51
000 0010	I	CMP2 ⁽¹⁾	011 0100	I	RPI52
000 0011	I	CMP3 ⁽¹⁾	011 0101	I	RPI53
000 0100	I	CMP4 ⁽¹⁾	011 0110	I/O	RP54
000 0101	—	—	011 0111	I/O	RP55
000 1100	I	CMP5 ⁽¹⁾	011 1000	I/O	RP56
000 1101	—	—	011 1001	I/O	RP57
000 1110	—	—	011 1010	I	RPI58
000 1111	—	—	011 1011	—	—
001 0000	I	RPI16	011 1100	I	RPI60
001 0001	I	RPI17	011 1101	I	RPI61
001 0010	I	RPI18	011 1110	—	—
001 0011	I	RPI19	011 1111	I	RPI 63
001 0100	I/O	RP20	100 0000	—	—
001 0101	—	—	100 0001	—	—
001 0110	—	—	100 0010	—	—
001 0111	—	—	100 0011	—	—
001 1000	I	RPI24	100 0100	—	—
001 1001	I	RPI25	100 0101	I/O	RP69
001 1010	—	—	100 0110	I/O	RP70
001 1011	I	RPI27	100 0111	—	—
001 1100	I	RPI28	100 1000	I	RPI72
001 1101	—	—	100 1001	—	—
001 1110	—	—	100 1010	—	—
001 1111	—	—	100 1011	—	—
010 0000	I	RPI32	100 1110	—	—
010 0001	I	RPI33	100 1111	—	—
010 0010	I	RPI34	101 0010	—	—
010 0011	I/O	RP35	101 0011	—	—
010 0100	I/O	RP36	101 0100	—	—
010 0101	I/O	RP37	010 1001	I/O	RP41
010 0110	I/O	RP38	010 1010	I/O	RP42
010 0111	I/O	RP39	010 1011	I/O	RP43
010 1000	I/O	RP40	101 1000	—	—
010 1100	I	RPI44	101 1001	—	—
010 1101	I	RPI45	101 1010	—	—
010 1110	I	RPI46	101 1011	—	—
010 1111	I	RPI47	101 1100	—	—
011 0000	I/O	RP48	101 1101	—	—

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

Note 1: These are virtual pins. See **Section 11.5.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)

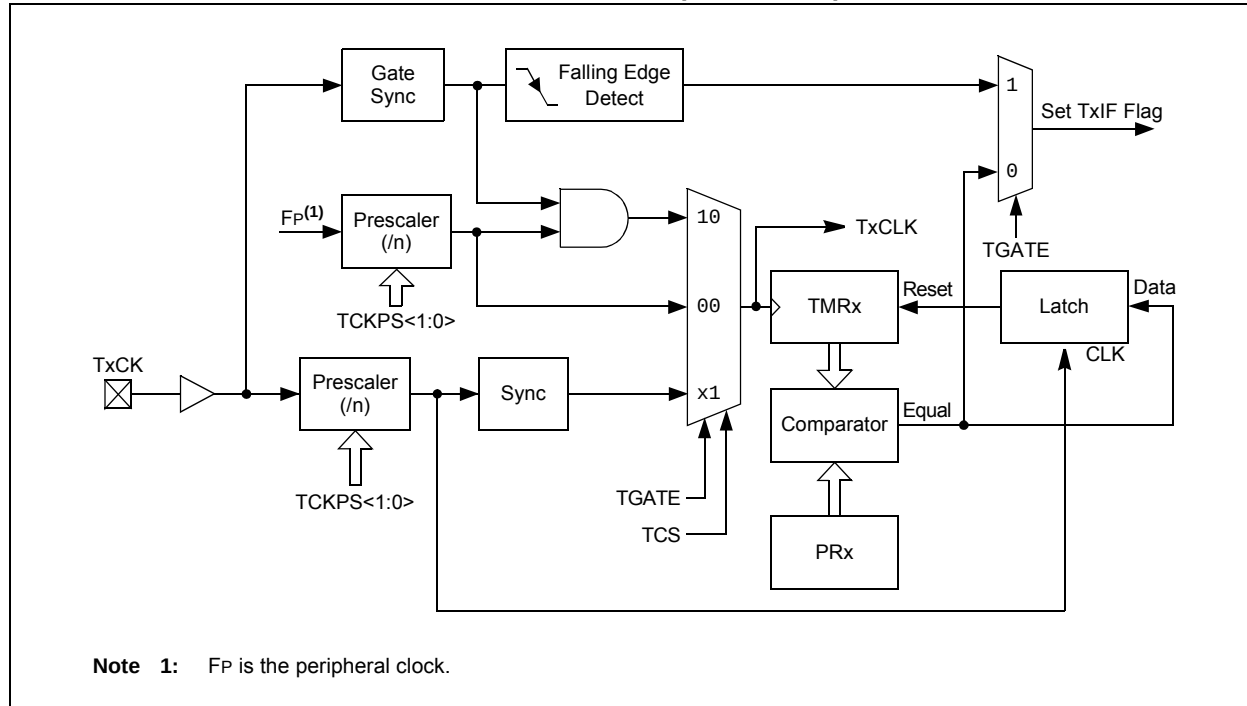
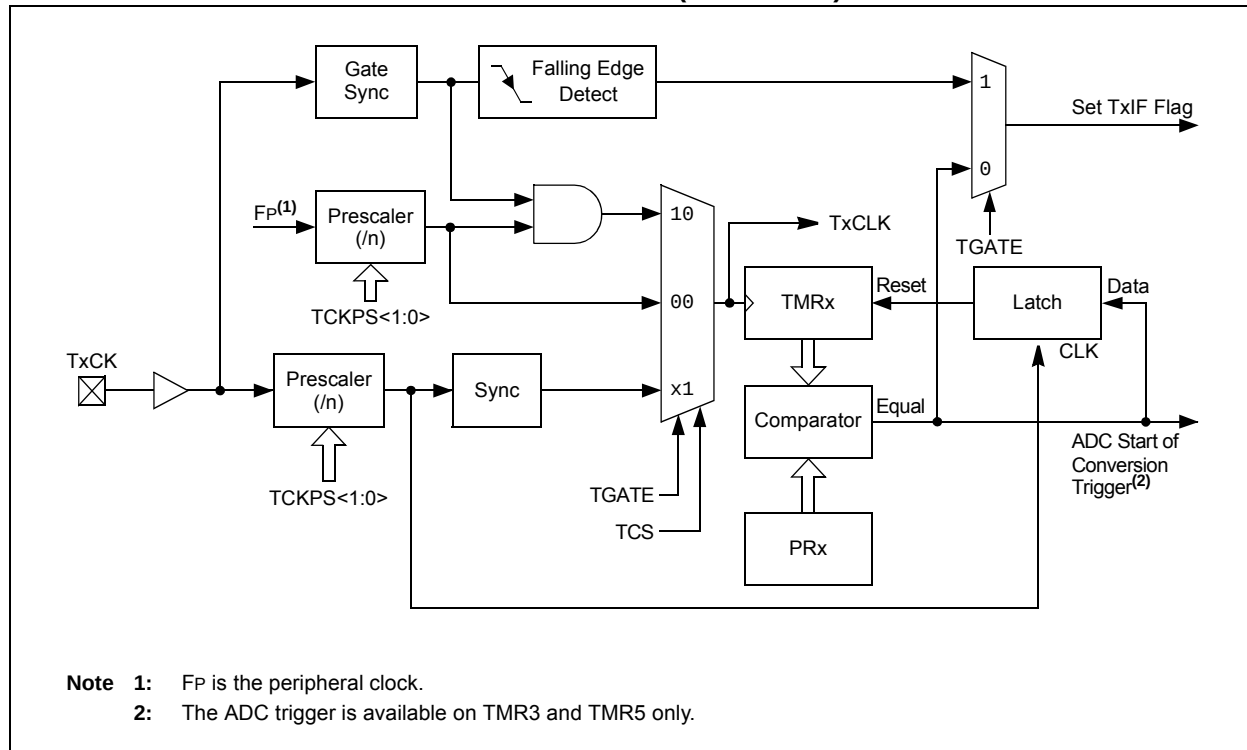


FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits⁽⁴⁾

11111 = Reserved
11110 = Reserved
11101 = Reserved
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization⁽⁵⁾
11010 = Analog Comparator 3 is the source for the capture timer synchronization⁽⁵⁾
11001 = Analog Comparator 2 is the source for the capture timer synchronization⁽⁵⁾
11000 = Analog Comparator 1 is the source for the capture timer synchronization⁽⁵⁾
10111 = Analog Comparator 5 is the source for the capture timer synchronization⁽⁵⁾
10110 = Analog Comparator 4 is the source for the capture timer synchronization⁽⁵⁾
10101 = Reserved
10100 = Reserved
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = Reserved
01001 = Reserved
01000 = Input Capture 4 is the source for the capture timer synchronization⁽⁶⁾
00111 = Input Capture 3 is the source for the capture timer synchronization⁽⁶⁾
00110 = Input Capture 2 is the source for the capture timer synchronization⁽⁶⁾
00101 = Input Capture 1 is the source for the capture timer synchronization⁽⁶⁾
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Reserved

- Note 1:** The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own sync or trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 17-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PDCx<15:0>**: PWMx Generator Duty Cycle Value bits

REGISTER 17-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7				bit 0			

Legend:

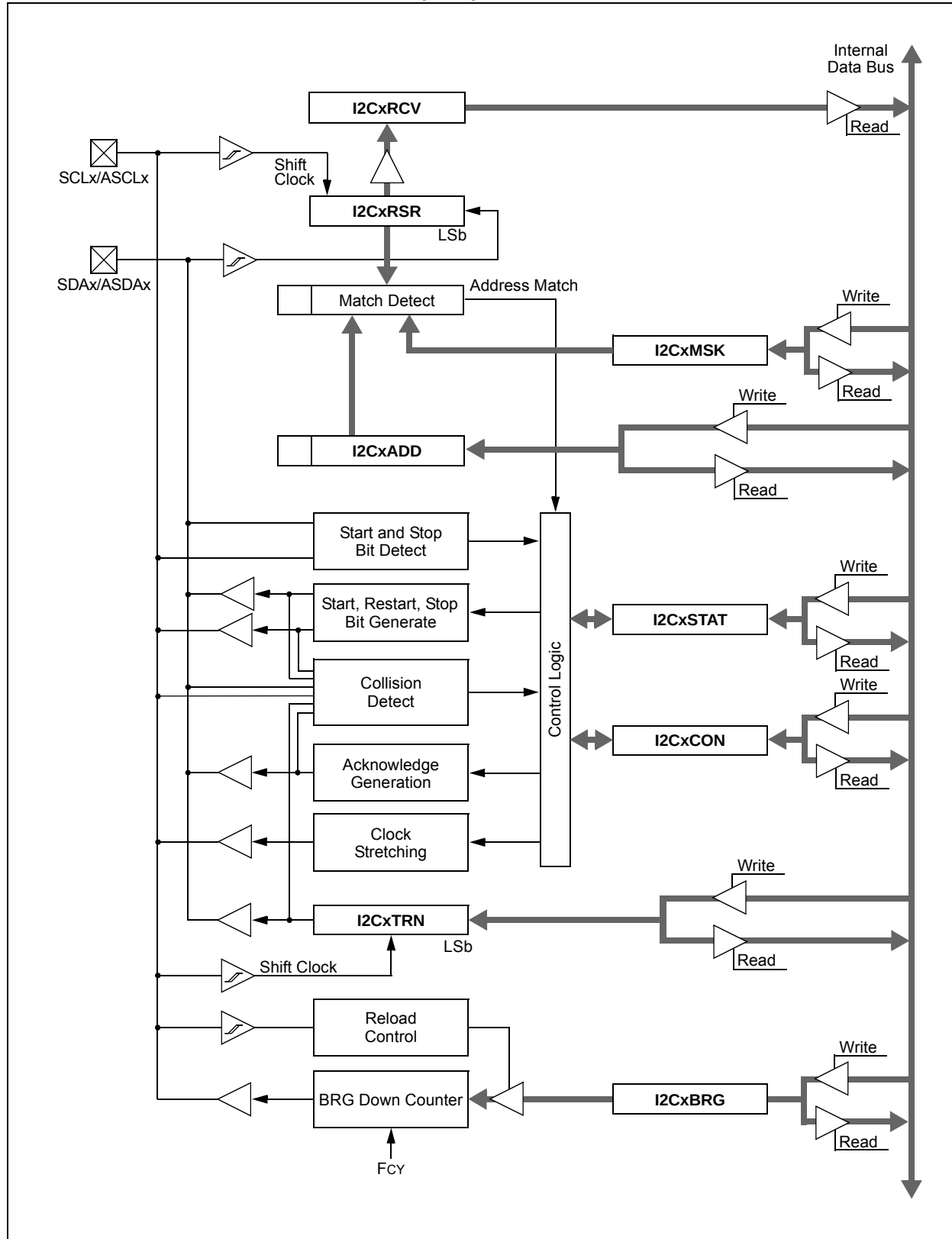
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PHASEx<15:0>**: PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

- Note 1:** If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.
- 2:** If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base period value for PWMxH and PWMxL.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1)



dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 24-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<15:0>**: ADCx Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

2: CSSx = ANx, where 'x' = 0-5.

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended		
Parameter No.	Typ. ⁽²⁾	Max.	Units	Conditions	
Power-Down Current (I _{PD}) – dsPIC33EVXXXGM00X/10X ⁽¹⁾					
DC60d	9.25	30	μA	-40°C	5.0V Base Power-Down Current
DC60a	15.75	35	μA	+25°C	
DC60b	67.75	250	μA	+85°C	
DC60c	270	750	μA	+125°C	
DC61d	1	7	μA	-40°C	5.0V Watchdog Timer Current: ΔI _{WDT} ⁽³⁾
DC61a	1.25	8	μA	+25°C	
DC61b	3.5	12	μA	+85°C	
DC61c	5	15	μA	+125°C	

Note 1: I_{PD} (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}} = V_{DD}$, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all ones)
- The VREGS bit (RCON<8>) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON<11>) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)

2: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See Note 3
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1} \downarrow$ to SCK1 $\uparrow$ or SCK1 $\downarrow$ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1} \uparrow$ to SDO1 Output High-Impedance	10	—	50	ns	See Note 4
SP52	Tsch2ssH, TscL2ssH	$\overline{SS1} \uparrow$ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See Note 4

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

dsPIC33EVXXXGM00X/10X FAMILY

NOTES:

32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. V_{CM}

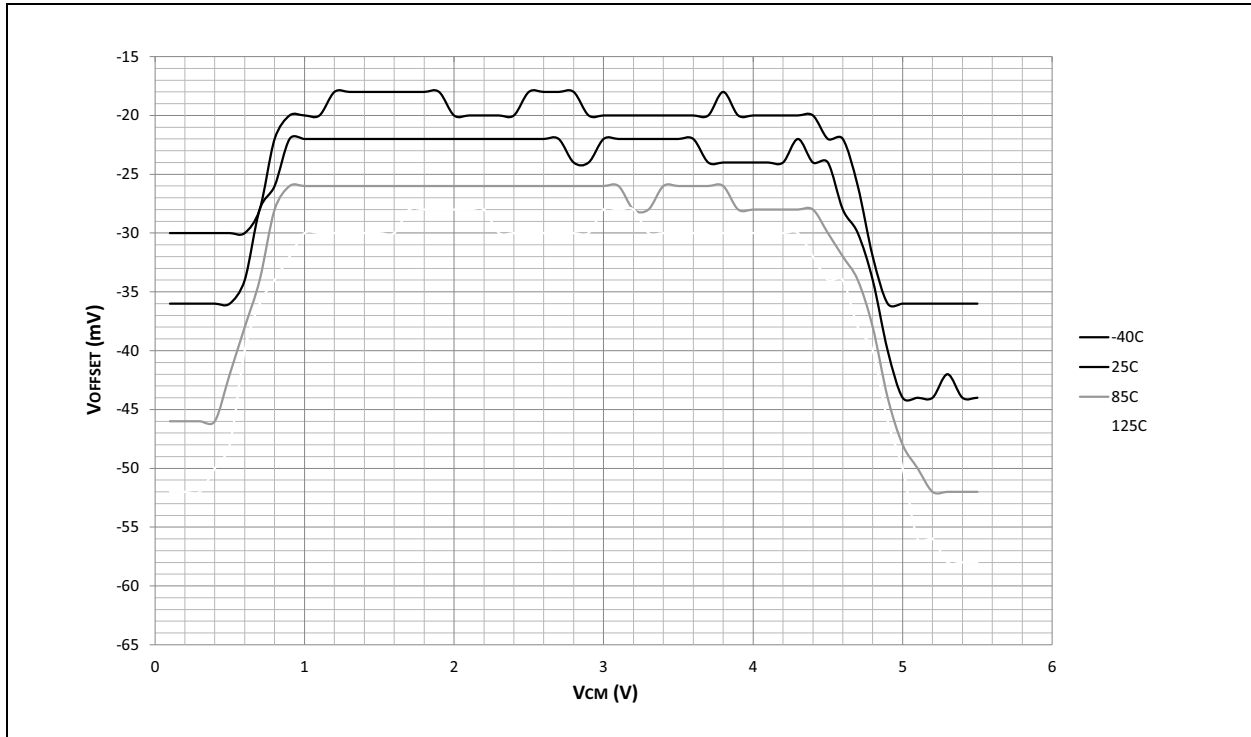
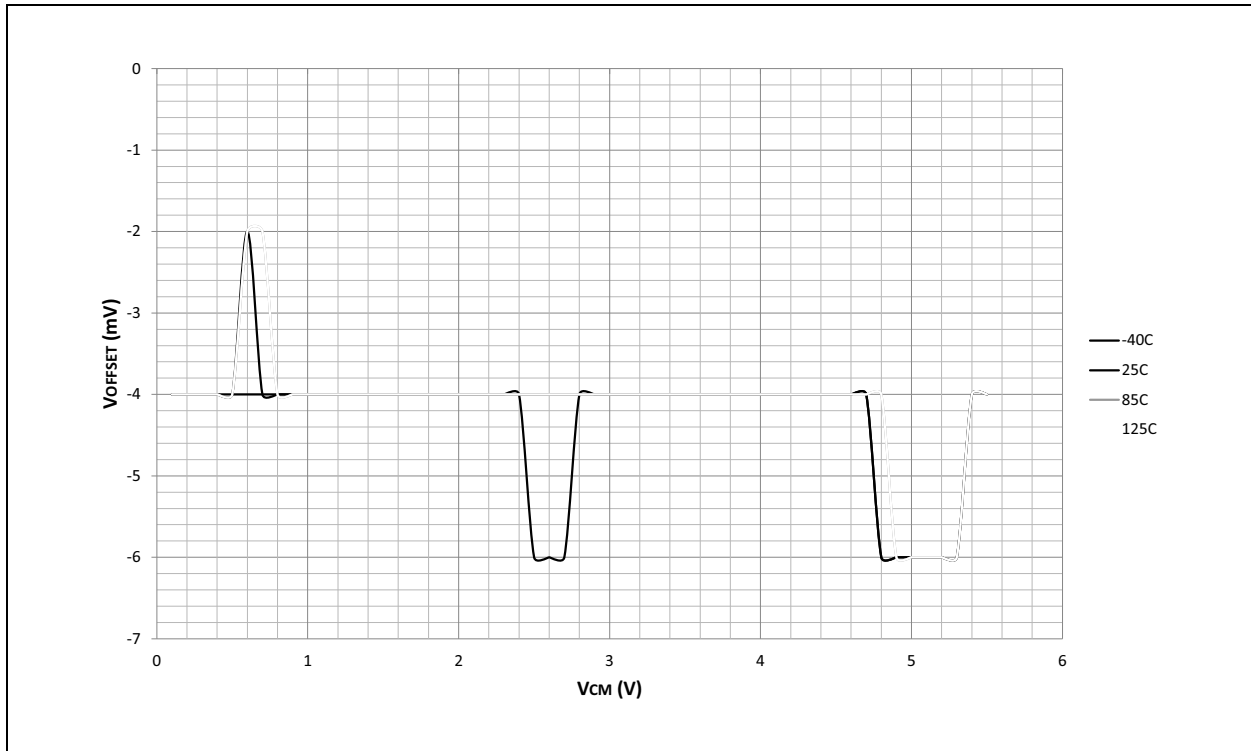


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. V_{CM} OP AMP OFFSET



dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 33-7: TYPICAL I_{IDLE} vs. V_{DD} (EC MODE, 20 MIPS)

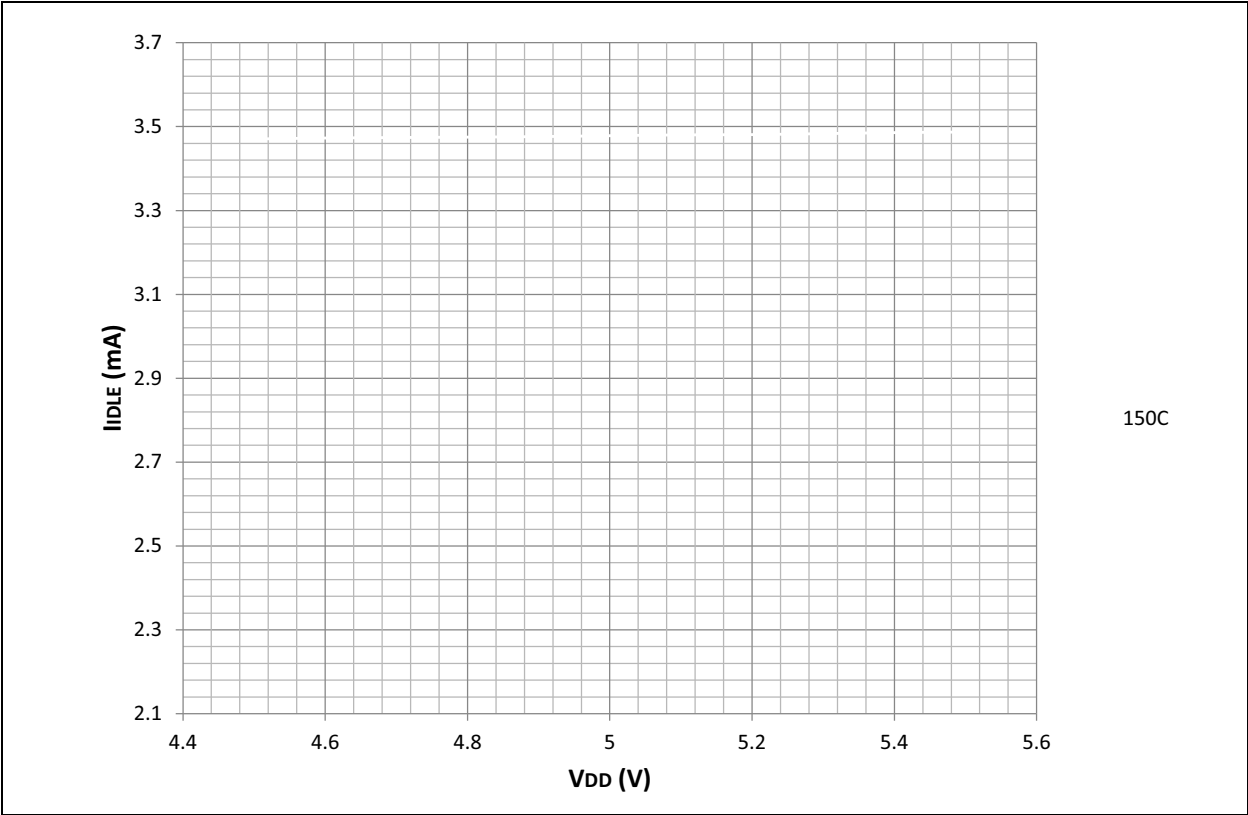
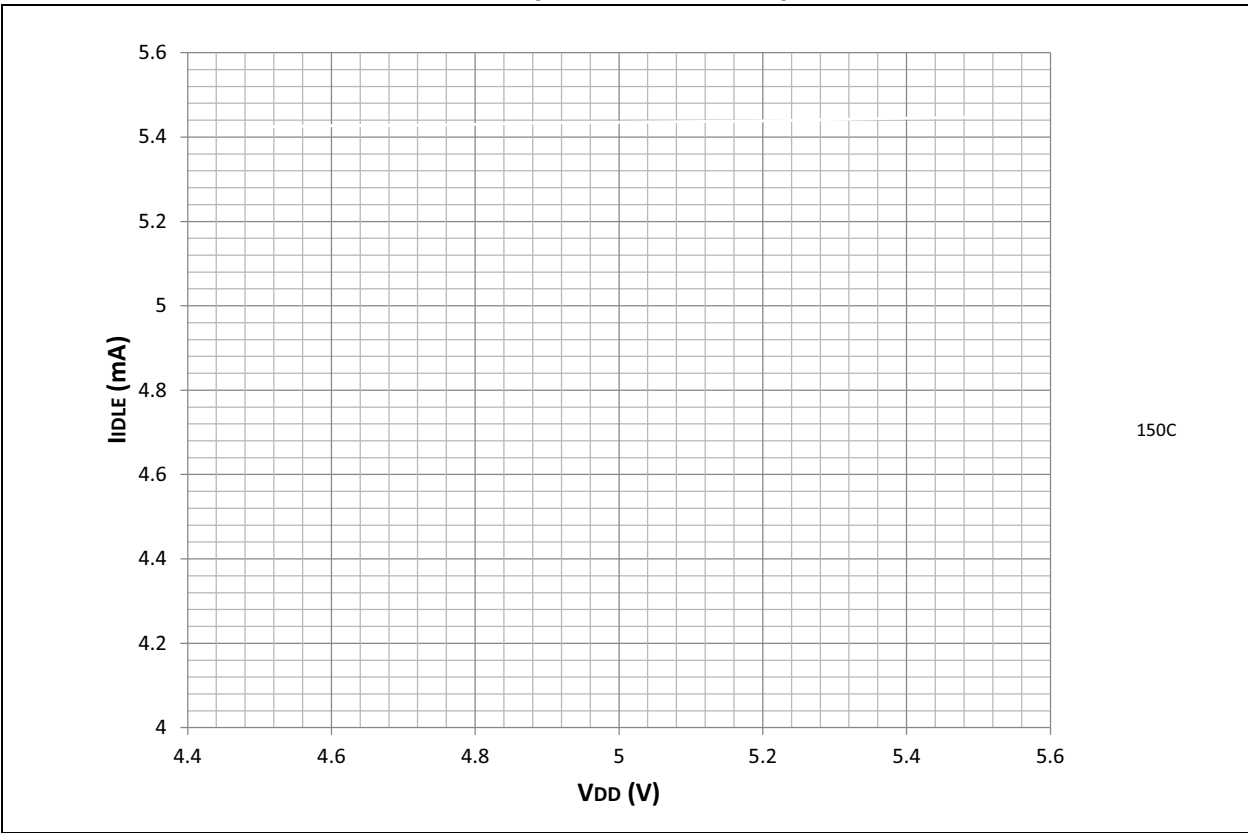
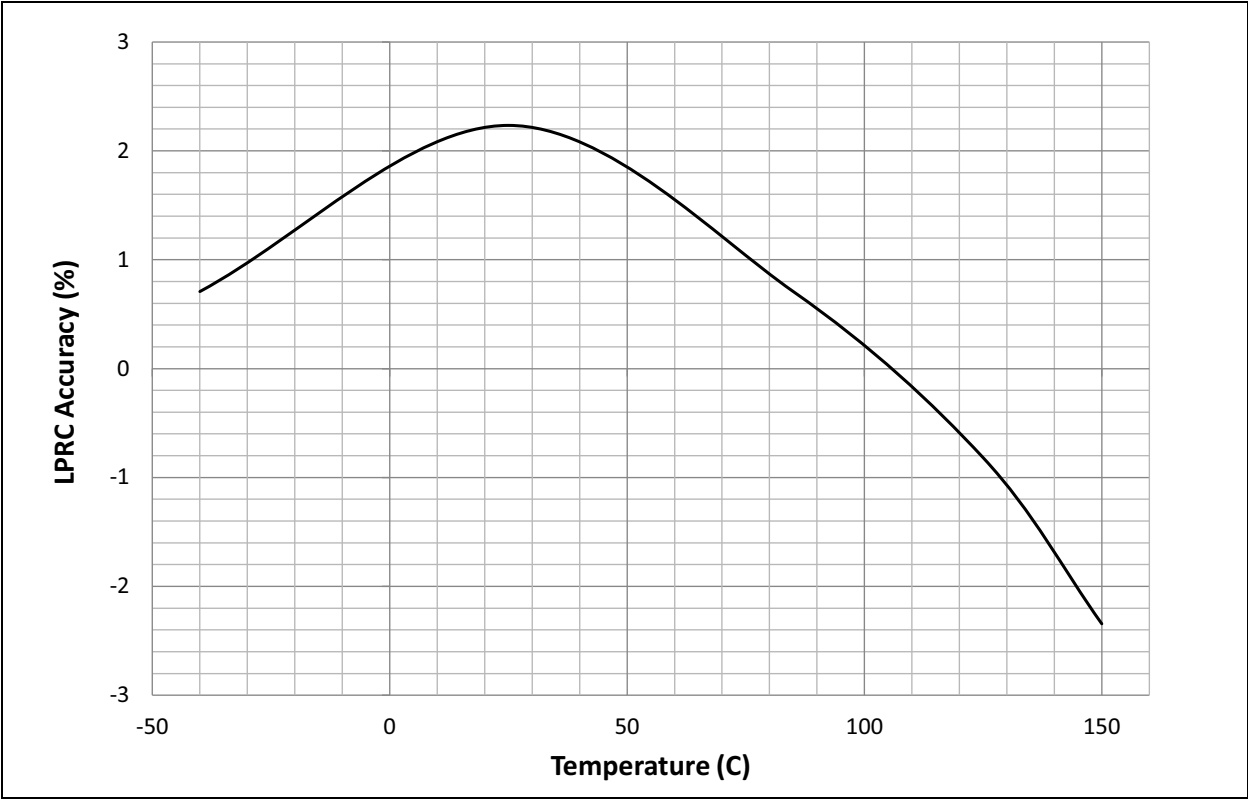


FIGURE 33-8: TYPICAL I_{IDLE} vs. V_{DD} (EC MODE, 40 MIPS)



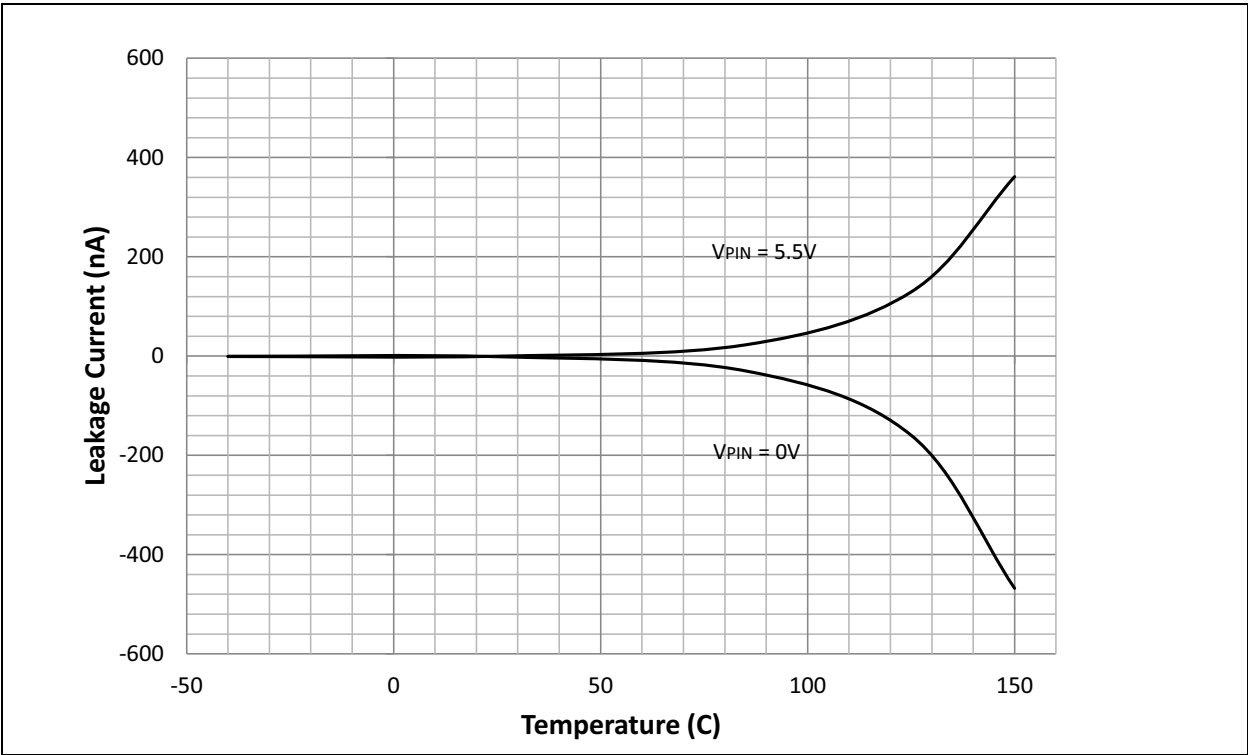
dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 33-19: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V VDD)



33.7 Leakage Current

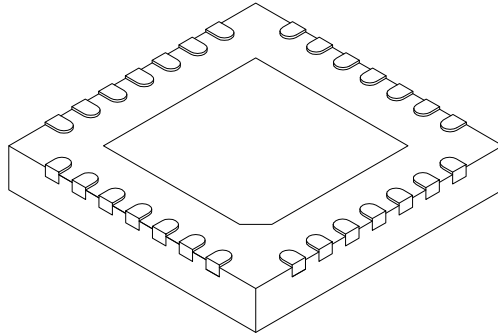
FIGURE 33-20: TYPICAL I_{IL} vs. TEMPERATURE ($\overline{\text{MCLR}}$)



dsPIC33EVXXXGM00X/10X FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

dsPIC33EVXXXGM00X/10X FAMILY

SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0)	366	V	
SPI2 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0)	368	Voltage Regulator (On-Chip)	324
Timer1-Timer5 External Clock	357	W	
UARTx I/O	391	Watchdog Timer (WDT).....	317, 325
U		Programming Considerations	325
UART		WWW Address	493
Control Registers	249	WWW, On-Line Support	11
Helpful Tips	248		
Universal Asynchronous Receiver			
Transmitter (UART).....	247		
Universal Asynchronous Receiver Transmitter. See UART.			
User OTP Memory	324		