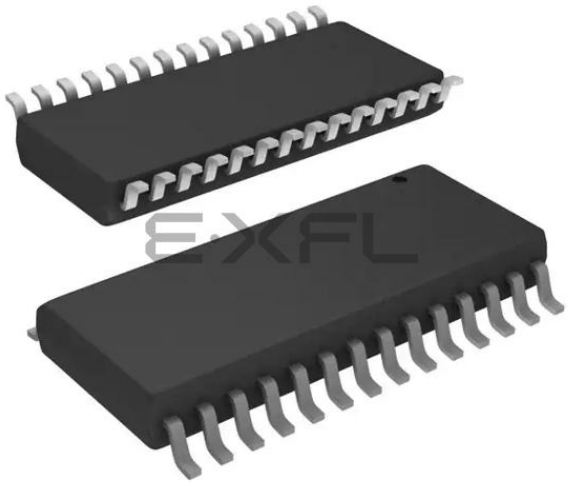
Microchip Technology - DSPIC33EV64GM002-I/SO Datasheet



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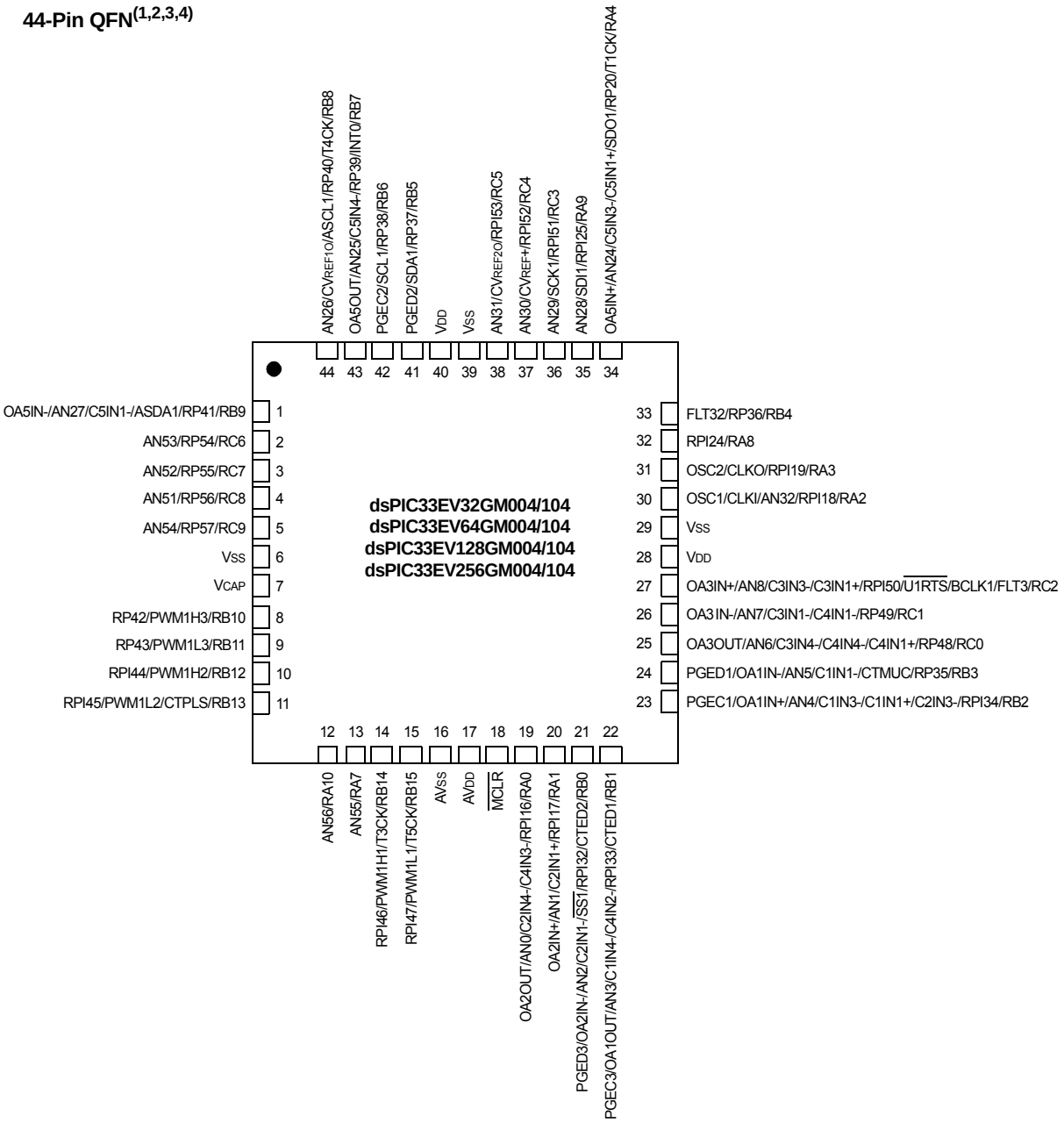
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm002-i-so

Pin Diagrams (Continued)

44-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT(1)	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminates executing the DO loop at the end of the current loop iteration
0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
111 = 7 DO loops are active
•
•
•
001 = 1 DO loop is active
000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EVXXXGM10X DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11SID	046C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF11EID	046E	EID<15:0>																xxxx
C1RXF12SID	0470	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF12EID	0472	EID<15:0>																xxxx
C1RXF13SID	0474	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF13EID	0476	EID<15:0>																xxxx
C1RXF14SID	0478	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF14EID	047A	EID<15:0>																xxxx
C1RXF15SID	047C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF15EID	047E	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: SENT1 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT1CON1	0500	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT1CON2	0504	TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode)																FFFF
SENT1CON3	0508	FRAMETIME<15:0> (Transmit modes) or SYNCMIN<15:0> (Receive mode)																FFFF
SENT1STAT	050C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT1SYNC	0510	Synchronization Time Period Register (Transmit mode)																0000
SENT1DATL	0514	DATA4<3:0>				DATA5<3:0>				DATA6<3:0>				CRC<3:0>				0000
SENT1DATH	0516	STAT<3:0>				DATA1<3:0>				DATA2<3:0>				DATA3<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: SENT2 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT2CON1	0520	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT2CON2	0524	TICKTIME<15:0> (Transmit modes) or SYNCMAX<15:0> (Receive mode)																FFFF
SENT2CON3	0528	FRAMETIME<15:0> (Transmit modes) or SYNCMIN<15:0> (Receive mode)																FFFF
SENT2STAT	052C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT2SYNC	0530	Synchronization Time Period Register (Transmit mode)																0000
SENT2DATL	0534	DATA4<3:0>				DATA5<3:0>				DATA6<3:0>				CRC<3:0>				0000
SENT2DATH	0536	STAT<3:0>				DATA1<3:0>				DATA2<3:0>				DATA3<3:0>				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-19: NVM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	RPDF	URERR	—	—	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMADR	072A	NVMADR<15:0>																0000
NVMADRU	072C	—	—	—	—	—	—	—	—	NVMADRU<23:16>								0000
NVMKEY	072E	—	—	—	—	—	—	—	—	NVMKEY<7:0>								0000
NVMSRCADRL	0730	NVMSRCADR<15:1>															0	0000
NVMSRCADRH	0732	—	—	—	—	—	—	—	—	NVMSRCADR<23:16>								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: SYSTEM CONTROL REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	0000
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV<8:0>									0000
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on the Configuration fuses.

TABLE 4-21: REFERENCE CLOCK REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-37: PORTC REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E28	TRISC15	—	TRISC<13:0>														BFFF
PORTC	0E2A	RC15	—	RC<13:0>														xxxx
LATC	0E2C	LATC15	—	LATC<13:0>														xxxx
ODCC	0E2E	ODCC15	—	ODCC<13:0>														0000
CNENC	0E30	CNIEC15	—	CNIEC<13:0>														0000
CNPUC	0E32	CNPUC15	—	CNPUC<13:0>														0000
CNPDC	0E34	CNPDC15	—	CNPDC<13:0>														0000
ANSELC	0E36	—	—	—	ANSC<12:0>													1FFF
SR1C	0E38	—	—	—	—	—	—	SR1C<9:6>				—	—	SR1C3	—	—	—	0000
SR0C	0E3A	—	—	—	—	—	—	SR0C<9:6>				—	—	SR0C3	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PORTC REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E28	—	—	—	—	—	—	TRISC<9:0>										BFFF
PORTC	0E2A	—	—	—	—	—	—	RC<9:0>										xxxx
LATC	0E2C	—	—	—	—	—	—	LATC<9:0>										xxxx
ODCC	0E2E	—	—	—	—	—	—	ODCC<9:0>										0000
CNENC	0E30	—	—	—	—	—	—	CNIEC<9:0>										0000
CNPUC	0E32	—	—	—	—	—	—	CNPUC<9:0>										0000
CNPDC	0E34	—	—	—	—	—	—	CNPDC<9:0>										0000
ANSELC	0E36	—	—	—	—	—	—	ANSC<9:0>										0807
SR1C	0E38	—	—	—	—	—	—	SR1C<9:6>				—	—	SR1C3	—	—	—	0000
SR0C	0E3A	—	—	—	—	—	—	SR0C<9:6>				—	—	SR0C3	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

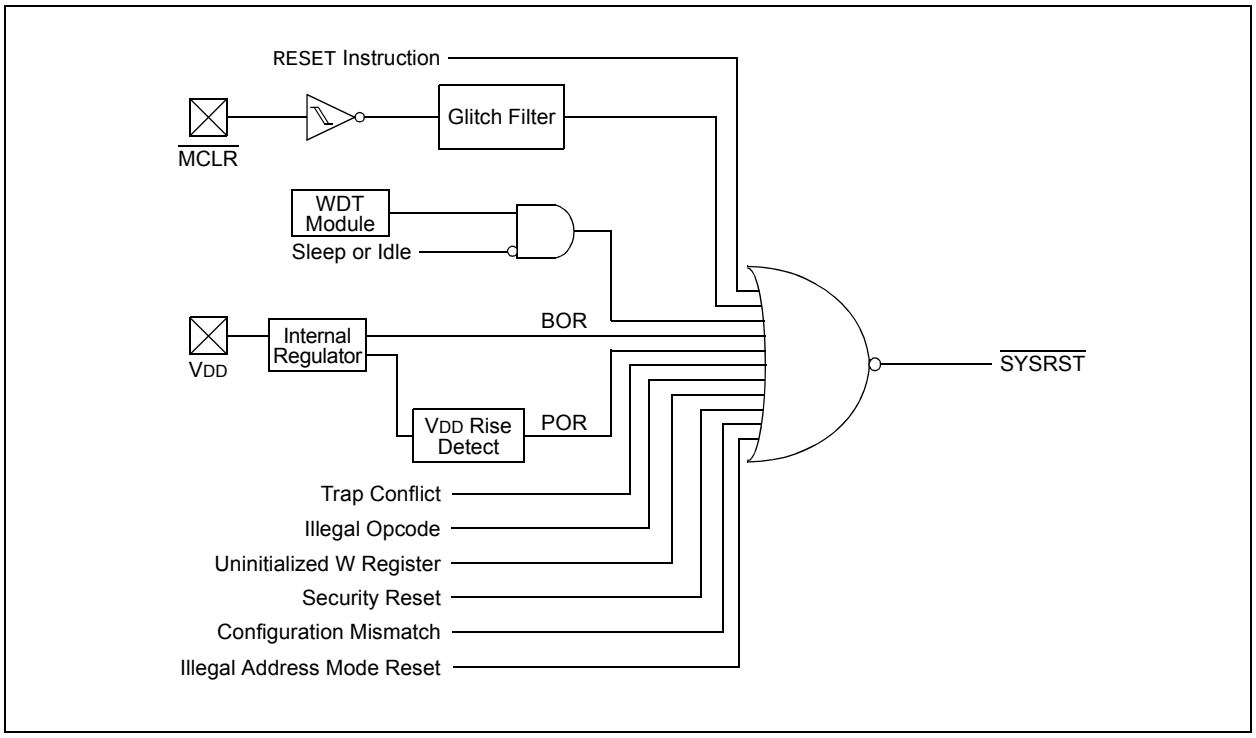


Table 9-1 provides the Configuration bits which allow users to choose between the various clock modes.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>
Fast RC Oscillator with Divide-by-N (FRCDIVN)(1,2)	Internal	xx	111
Fast RC Oscillator with Divide-by-16 (FRCDIV16)(1)	Internal	xx	110
Low-Power RC Oscillator (LPRC)(1)	Internal	xx	101
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011
Primary Oscillator (EC) with PLL (ECPLL)(1)	Primary	00	011
Primary Oscillator (HS)	Primary	10	010
Primary Oscillator (XT)	Primary	01	010
Primary Oscillator (EC)(1)	Primary	00	010
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)(1)	Internal	xx	001
Fast RC Oscillator (FRC)(1)	Internal	xx	000

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 11-28: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R5(1)	RP120R4(1)	RP120R3(1)	RP120R2(1)	RP120R1(1)	RP120R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP176R<5:0>:** Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits(1) (see Table 11-3 for peripheral function numbers)

Note 1: RP120R<5:0> is present in dsPIC33EVXXXGM006/106 devices only.

REGISTER 11-29: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP178R<5:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP177R<5:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 11-3 for peripheral function numbers)

NOTES:

17.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EVXXXGM00X/10X family devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FDEVOPT<0>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 17-1.

EXAMPLE 17-1: PWM1 WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd, w10      ; Load first unlock key to w10 register
mov #0x4321, w11      ; Load second unlock key to w11 register
mov #0x0000, w0       ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY       ; Write first unlock key to PWMKEY register
mov w11, PWMKEY       ; Write second unlock key to PWMKEY register
mov w0, FCLCON1       ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd, w10      ; Load first unlock key to w10 register
mov #0x4321, w11      ; Load second unlock key to w11 register
mov #0xF000, w0       ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY       ; Write first unlock key to PWMKEY register
mov w11, PWMKEY       ; Write second unlock key to PWMKEY register
mov w0, IOCON1        ; Write desired value to IOCON1 register
```

17.3 PWMx Control Registers

REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HS-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU(1)	SYNCPOL(1)	SYNCOEN(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN(1)	SYNCSRC2(1)	SYNCSRC1(1)	SYNCSRC0(1)	SEVTPS3(1)	SEVTPS2(1)	SEVTPS1(1)	SEVTPS0(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 17-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled through the BCH and BCL bits in the LEBCONx register).

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the state blank source
0010 = PWM2H is selected as the state blank source
0001 = PWM1H is selected as the state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits

The selected signal will enable and disable (Chop) the selected PWMx outputs.

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the chop clock source
0010 = PWM2H is selected as the chop clock source
0001 = PWM1H is selected as the chop clock source
0000 = Chop clock generator is selected as the chop clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

REGISTER 20-3: SENTxDATL: SENTx RECEIVE DATA REGISTER LOW(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA4<3:0>				DATA5<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA6<3:0>				CRC<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **DATA4<3:0>:** Data Nibble 4 Data bits

bit 11-8 **DATA5<3:0>:** Data Nibble 5 Data bits

bit 7-4 **DATA6<3:0>:** Data Nibble 6 Data bits

bit 3-0 **CRC<3:0>:** CRC Nibble Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

REGISTER 20-4: SENTxDATH: SENTx RECEIVE DATA REGISTER HIGH(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STAT<3:0>				DATA1<3:0>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA2<3:0>				DATA3<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **STAT<3:0>:** Status Nibble Data bits

bit 11-8 **DATA1<3:0>:** Data Nibble 1 Data bits

bit 7-4 **DATA2<3:0>:** Data Nibble 2 Data bits

bit 3-0 **DATA3<3:0>:** Data Nibble 3 Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC<3:0> bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

22.3 CAN Control Registers

REGISTER 22-1: CxCTRL1: CANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CANx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** CANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Sets Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Sets Configuration mode
011 = Sets Listen Only mode
010 = Sets Loopback mode
001 = Sets Disable mode
000 = Sets Normal Operation mode

bit 7-5 **OPMODE<2:0>**: Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CANx Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<15:8>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<7:0>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<31:24>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<23:16>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEVID<23:16>(1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID<15:8>(1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID<7:0>(1)							
bit 7							bit 0

Legend:	R = Read-Only bit	U = Unimplemented bit

bit 23-0 **DEVID<23:0>:** Device Identifier bits(1)

Note 1: Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of Device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
DEVREV<23:16>(1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV<15:8>(1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV<7:0>(1)							
bit 7							bit 0

Legend:	R = Read-only bit	U = Unimplemented bit

bit 23-0 **DEVREV<23:0>:** Device Revision bits(1)

Note 1: Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of device revision values.

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33EVXXXGM00X/10X Family
HDC5	4.5V to 5.5V(1,2)	-40°C to +150°C	40

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Device functionality is tested but is not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: When BOR is enabled, the device will work from 4.7V to 5.5V.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
Operating Voltage							
HDC10	VDD	**Supply Voltage(3)**	VBOR	—	5.5	V	
HDC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	
HDC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
HDC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-5.0V in 5 ms
HDC18	VCORE	**VDD Core** Internal Regulator Voltage	1.62	1.8	1.98	V	Voltage is dependent on load, temperature and VDD

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: VDD voltage must remain at VSS for a minimum of 200 μs to ensure POR.

32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. VCM

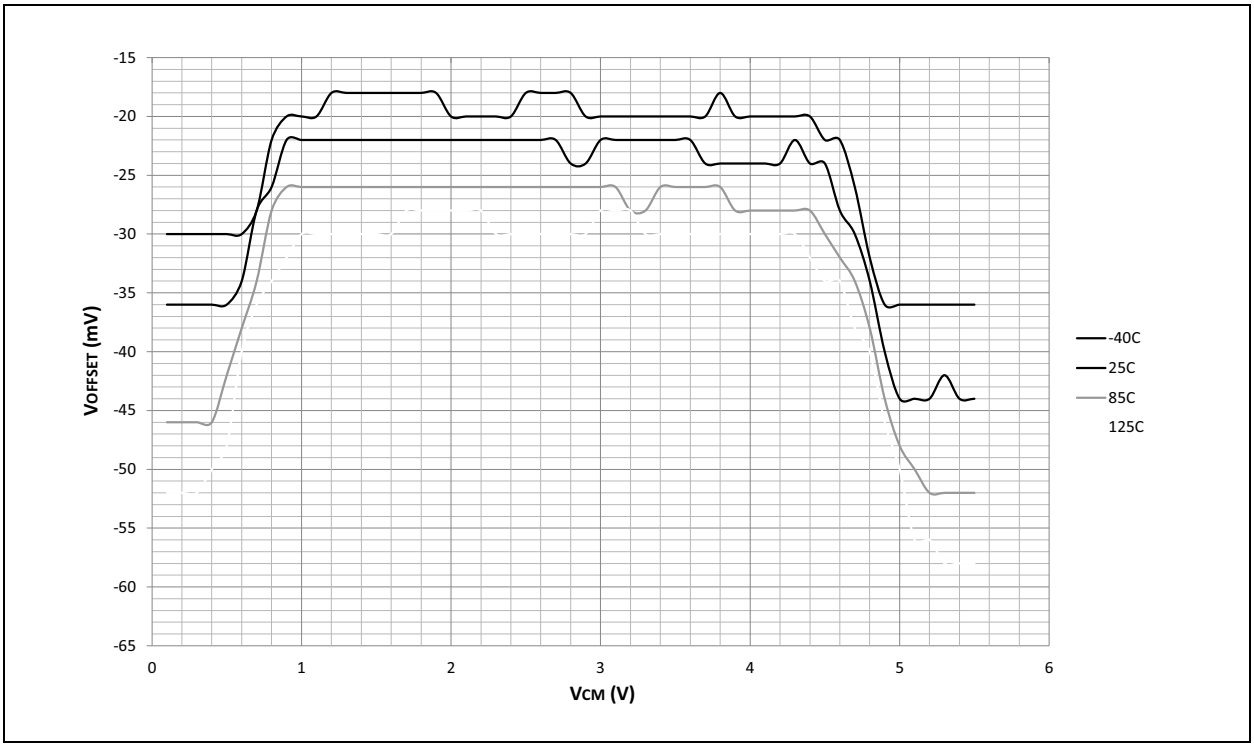
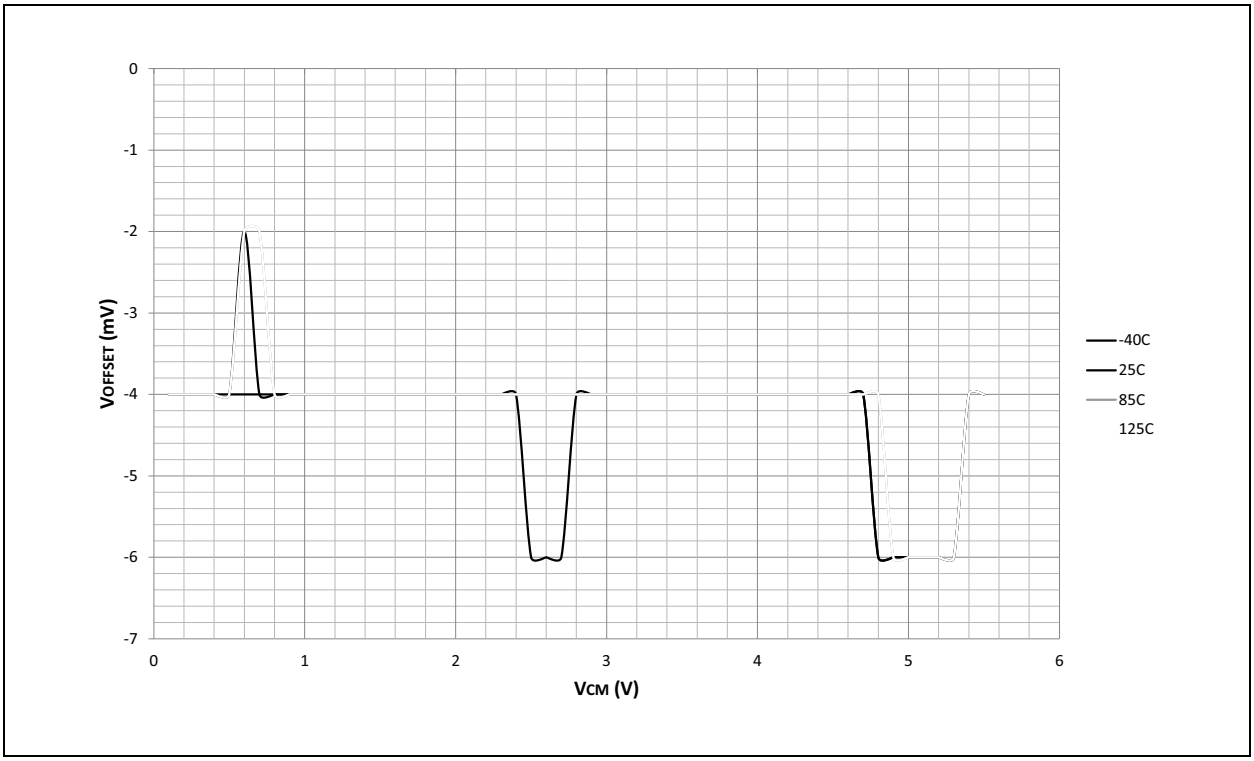


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. VCM OP AMP OFFSET



33.14 Comparator Op Amp Offset

FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. VCM

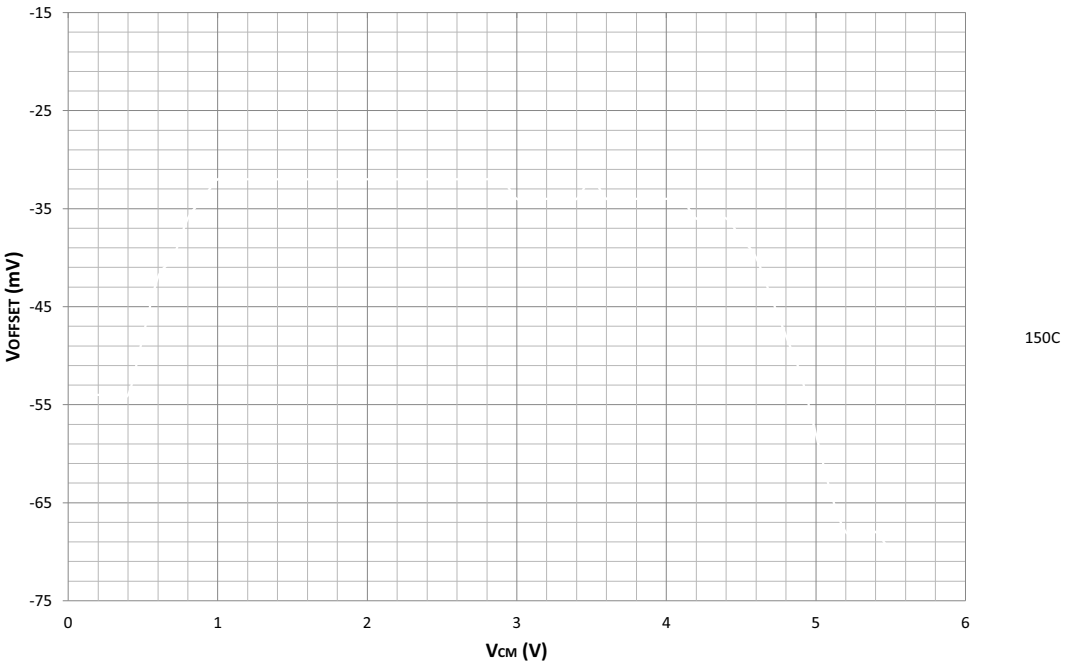


FIGURE 33-34: TYPICAL OP AMP OFFSET vs. VCM