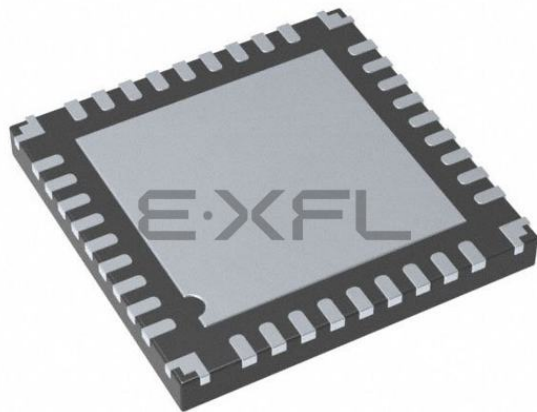




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#### Details

|                            |                                                                                                                                                                               |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                        |
| Core Processor             | dsPIC                                                                                                                                                                         |
| Core Size                  | 16-Bit                                                                                                                                                                        |
| Speed                      | 60 MIPS                                                                                                                                                                       |
| Connectivity               | I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART                                                                                                                               |
| Peripherals                | Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT                                                                                                                 |
| Number of I/O              | 25                                                                                                                                                                            |
| Program Memory Size        | 64KB (22K x 24)                                                                                                                                                               |
| Program Memory Type        | FLASH                                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                                             |
| RAM Size                   | 8K x 8                                                                                                                                                                        |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V                                                                                                                                                                   |
| Data Converters            | A/D 13x10b/12b                                                                                                                                                                |
| Oscillator Type            | Internal                                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 125°C (TA)                                                                                                                                                            |
| Mounting Type              | Surface Mount                                                                                                                                                                 |
| Package / Case             | 36-UQFN Exposed Pad                                                                                                                                                           |
| Supplier Device Package    | 36-UQFN (5x5)                                                                                                                                                                 |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm003-e-m5">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm003-e-m5</a> |

## dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.

**TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES**

| Device            | Program Memory Bytes | SRAM Bytes | CAN | DMA Channels | 16-Bit Timers (T1) | 32-Bit Timers | Input Capture | Output Compare | PWM | UART | SPI | I <sup>2</sup> C | SENT | 10/12-Bit ADC | ADC Inputs | Op Amp/Comparators | CTMU | Security     | Peripheral Pin Select (PPS) | General Purpose I/O (GPIO) | External Interrupts | Pins | Packages                 |
|-------------------|----------------------|------------|-----|--------------|--------------------|---------------|---------------|----------------|-----|------|-----|------------------|------|---------------|------------|--------------------|------|--------------|-----------------------------|----------------------------|---------------------|------|--------------------------|
| dsPIC33EV32GM002  | 32K                  | 4K         | 0   | 4            | 5                  | 2             | 4             | 4              | 3x2 | 2    | 2   | 1                | 2    | 1             | 11         | 3/4                | 1    | Intermediate | Y                           | 21                         | 3                   | 28   | SPDIP, SOIC, SSOP, QFN-S |
| dsPIC33EV32GM102  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM002  | 64K                  | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM102  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM002 | 128K                 | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM102 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM002 | 256K                 | 16K        | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM102 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV32GM004  | 32K                  | 4K         | 0   | 4            | 5                  | 2             | 4             | 4              | 3x2 | 2    | 2   | 1                | 2    | 1             | 24         | 4/5                | 1    | Intermediate | Y                           | 35                         | 3                   | 44   | TQFP, QFN                |
| dsPIC33EV32GM104  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM004  | 64K                  | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM104  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM004 | 128K                 | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM104 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM004 | 256K                 | 16K        | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM104 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV32GM006  | 32K                  | 4K         | 0   | 4            | 5                  | 2             | 4             | 4              | 3x2 | 2    | 2   | 1                | 2    | 1             | 36         | 4/5                | 1    | Intermediate | Y                           | 53                         | 3                   | 64   | TQFP, QFN                |
| dsPIC33EV32GM106  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM006  | 64K                  | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV64GM106  |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM006 | 128K                 | 8K         | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV128GM106 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM006 | 256K                 | 16K        | 0   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |
| dsPIC33EV256GM106 |                      |            | 1   |              |                    |               |               |                |     |      |     |                  |      |               |            |                    |      |              |                             |                            |                     |      |                          |

## Referenced Sources

This device data sheet is based on the following individual chapters of the *“dsPIC33/PIC24 Family Reference Manual”*, which are available from the Microchip web site ([www.microchip.com](http://www.microchip.com)). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- **“Introduction”** (DS70573)
- **“CPU”** (DS70359)
- **“Data Memory”** (DS70595)
- **“dsPIC33E/PIC24E Program Memory”** (DS70000613)
- **“Flash Programming”** (DS70609)
- **“Interrupts”** (DS70000600)
- **“Oscillator”** (DS70580)
- **“Reset”** (DS70602)
- **“Watchdog Timer and Power-Saving Modes”** (DS70615)
- **“I/O Ports”** (DS70000598)
- **“Timers”** (DS70362)
- **“CodeGuard™ Intermediate Security”** (DS70005182)
- **“Deadman Timer (DMT)”** (DS70005155)
- **“Input Capture”** (DS70000352)
- **“Output Compare”** (DS70005157)
- **“High-Speed PWM”** (DS70645)
- **“Analog-to-Digital Converter (ADC)”** (DS70621)
- **“Universal Asynchronous Receiver Transmitter (UART)”** (DS70000582)
- **“Serial Peripheral Interface (SPI)”** (DS70005185)
- **“Inter-Integrated Circuit™ (I²C™)”** (DS70000195)
- **“Enhanced Controller Area Network (ECAN™)”** (DS70353)
- **“Direct Memory Access (DMA)”** (DS70348)
- **“Programming and Diagnostics”** (DS70608)
- **“Op Amp/Comparator”** (DS70000357)
- **“Device Configuration”** (DS70000618)
- **“Charge Time Measurement Unit (CTMU)”** (DS70661)
- **“Single-Edge Nibble Transmission (SENT) Module”** (DS70005145)

TABLE 4-22: PMD REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12  | Bit 11  | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6 | Bit 5 | Bit 4  | Bit 3  | Bit 2  | Bit 1               | Bit 0 | All Resets |
|----------|-------|--------|--------|--------|---------|---------|--------|--------|--------|--------|-------|-------|--------|--------|--------|---------------------|-------|------------|
| PMD1     | 0760  | T5MD   | T4MD   | T3MD   | T2MD    | T1MD    | —      | PWMMD  | —      | I2C1MD | U2MD  | U1MD  | SPI2MD | SPI1MD | —      | C1MD <sup>(1)</sup> | AD1MD | 0000       |
| PMD2     | 0762  | —      | —      | —      | —       | IC4MD   | IC3MD  | IC2MD  | IC1MD  | —      | —     | —     | —      | OC4MD  | OC3MD  | OC2MD               | OC1MD | 0000       |
| PMD3     | 0764  | —      | —      | —      | —       | —       | CMPMD  | —      | —      | —      | —     | —     | —      | —      | —      | —                   | —     | 0000       |
| PMD4     | 0766  | —      | —      | —      | —       | —       | —      | —      | —      | —      | —     | —     | —      | REFOMD | CTMUMD | —                   | —     | 0000       |
| PMD6     | 076A  | —      | —      | —      | —       | —       | PWM3MD | PWM2MD | PWM1MD | —      | —     | —     | —      | —      | —      | —                   | —     | 0000       |
| PMD7     | 076C  | —      | —      | —      | —       | —       | —      | —      | —      | —      | —     | —     | DMA0MD | —      | —      | —                   | —     | 0000       |
|          |       |        |        |        |         |         |        |        |        |        |       |       | DMA1MD |        |        |                     |       |            |
|          |       |        |        |        |         |         |        |        |        |        |       |       | DMA2MD |        |        |                     |       |            |
|          |       |        |        |        |         |         |        |        |        |        |       |       | DMA3MD |        |        |                     |       |            |
| PMD8     | 076E  | —      | —      | —      | SENT2MD | SENT1MD | —      | —      | DMTMD  | —      | —     | —     | —      | —      | —      | —                   | —     | 0000       |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** This feature is available only on dsPIC33EVXXXGM10X devices.

# dsPIC33EVXXXGM00X/10X FAMILY

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source                           | Vector No. | IRQ No. | IVT Address       | Interrupt Bit Location |           |              |
|--------------------------------------------|------------|---------|-------------------|------------------------|-----------|--------------|
|                                            |            |         |                   | Flag                   | Enable    | Priority     |
| UART1 Error Interrupt (U1E)                | 73         | 65      | 0x000096          | IFS4<1>                | IEC4<1>   | IPC16<6:4>   |
| UART2 Error Interrupt (U2E)                | 74         | 66      | 0x000098          | IFS4<2>                | IEC4<2>   | IPC16<10:8>  |
| Reserved                                   | 76-77      | 68-69   | 0x00009C-0x00009E | —                      | —         | —            |
| CAN1 TX Data Request (C1TX) <sup>(1)</sup> | 78         | 70      | 0x0000A0          | IFS4<6>                | IEC4<6>   | IPC17<10:8>  |
| Reserved                                   | 80         | 72      | 0x0000A4          | —                      | —         | —            |
| Reserved                                   | 82         | 74      | 0x0000A8          | —                      | —         | —            |
| Reserved                                   | 84         | 76      | 0x0000AC          | —                      | —         | —            |
| CTMU Interrupt (CTMU)                      | 85         | 77      | 0x0000AE          | IFS4<13>               | IEC4<13>  | IPC19<6:4>   |
| Reserved                                   | 86-88      | 78-80   | 0x0000B0-0x0000B4 | —                      | —         | —            |
| Reserved                                   | 92-94      | 84-86   | 0x0000BC-0x0000C0 | —                      | —         | —            |
| Reserved                                   | 100-101    | 92-93   | 0x0000CC-0x0000CE | —                      | —         | —            |
| PWM Generator 1 (PWM1)                     | 102        | 94      | 0x0000D0          | IFS5<14>               | IEC5<14>  | IPC23<10:8>  |
| PWM Generator 2 (PWM2)                     | 103        | 95      | 0x0000D2          | IFS5<15>               | IEC5<15>  | IPC23<14:12> |
| PWM Generator 3 (PWM3)                     | 104        | 96      | 0x0000D4          | IFS6<0>                | IEC6<0>   | IPC24<2:0>   |
| Reserved                                   | 108-149    | 100-141 | 0x0000DC-0x00012E | —                      | —         | —            |
| ICD Application (ICD)                      | 150        | 142     | 0x000142          | IFS8<14>               | IEC8<14>  | IPC35<10:8>  |
| Reserved                                   | 152        | 144     | 0x000134          | —                      | —         | —            |
| Bus Collision (I2C1)                       | —          | 173     | 0x00016E          | IFS10<13>              | IEC10<13> | IPC43<4:6>   |
| SENT1 Error (SENT1ERR)                     | —          | 182     | 0x000180          | IFS11<6>               | IEC11<6>  | IPC45<10:8>  |
| SENT1 TX/RX (SENT1)                        | —          | 183     | 0x000182          | IFS11<7>               | IEC11<7>  | IPC45<14:12> |
| SENT2 Error (SENT2ERR)                     | —          | 184     | 0x000184          | IFS11<8>               | IEC11<8>  | IPC46<2:0>   |
| SENT2 TX/RX (SENT2)                        | —          | 185     | 0x000186          | IFS11<9>               | IEC11<9>  | IPC46<6:4>   |
| ECC Single-Bit Error (ECCSBE)              | —          | 186     | 0x000188          | IFS11<10>              | IEC11<10> | IPC45<10:8>  |
| Reserved                                   | 159-245    | 187-245 | 0x000142-0x0001FE | —                      | —         | —            |
| Lowest Natural Order Priority              |            |         |                   |                        |           |              |

**Note 1:** This interrupt source is available on dsPIC33EVXXXGM10X devices only.

# dsPIC33EVXXXGM00X/10X FAMILY

**REGISTER 10-7: PMD8: PERIPHERAL MODULE DISABLE CONTROL REGISTER 8**

|        |     |     |         |         |     |       |       |
|--------|-----|-----|---------|---------|-----|-------|-------|
| U-0    | U-0 | U-0 | R/W-0   | R/W-0   | U-0 | U-0   | R/W-0 |
| —      | —   | —   | SENT2MD | SENT1MD | —   | —     | DMTMD |
| bit 15 |     |     |         |         |     | bit 8 |       |

|       |     |     |     |     |     |       |     |
|-------|-----|-----|-----|-----|-----|-------|-----|
| U-0   | U-0 | U-0 | U-0 | U-0 | U-0 | U-0   | U-0 |
| —     | —   | —   | —   | —   | —   | —     | —   |
| bit 7 |     |     |     |     |     | bit 0 |     |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **SENT2MD:** SENT2 Module Disable bit

1 = SENT2 module is disabled

0 = SENT2 module is enabled

bit 11 **SENT1MD:** SENT1 Module Disable bit

1 = SENT1 module is disabled

0 = SENT1 module is enabled

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **DMTMD:** Deadman Timer Disable bit

1 = Deadman Timer is disabled

0 = Deadman Timer is enabled

bit 7-0 **Unimplemented:** Read as '0'

## 12.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “Timers” (DS70362) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running, interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The Timer1 External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

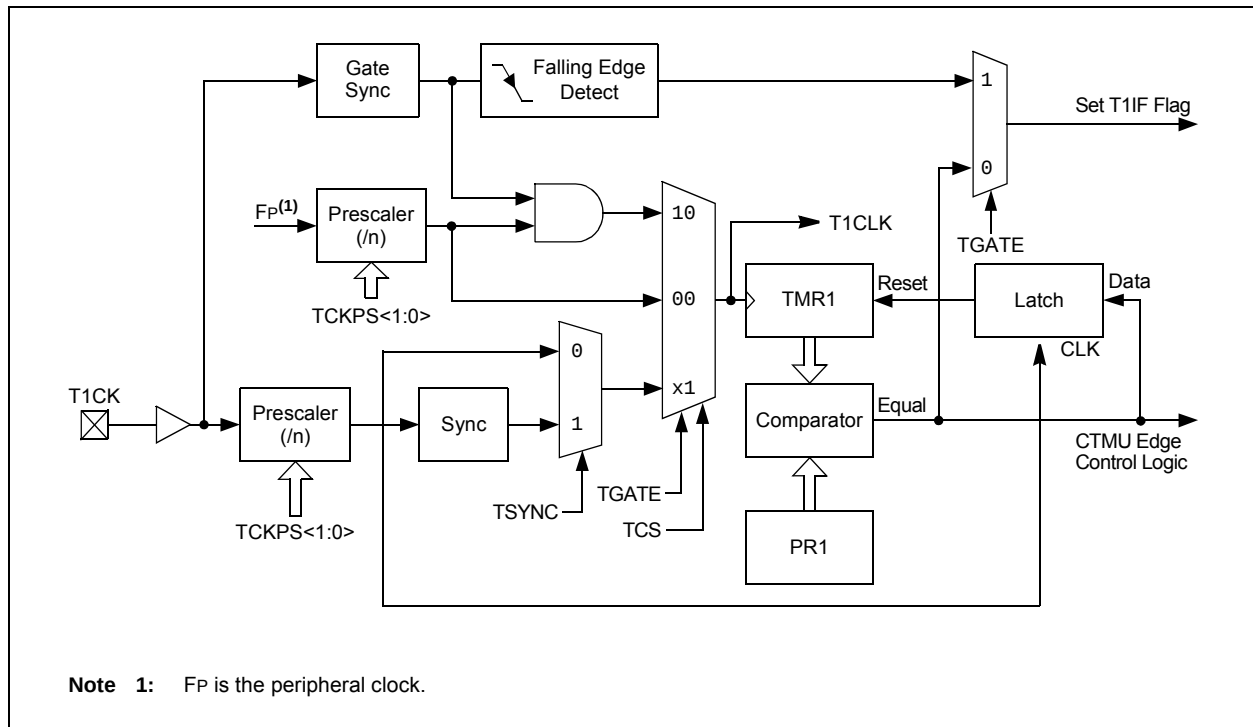
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit settings for different operating modes are given in Table 12-1.

**TABLE 12-1: TIMER MODE SETTINGS**

| Mode                 | TCS | TGATE | TSYNC |
|----------------------|-----|-------|-------|
| Timer                | 0   | 0     | x     |
| Gated Timer          | 0   | 1     | x     |
| Synchronous Counter  | 1   | x     | 1     |
| Asynchronous Counter | 1   | x     | 0     |

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**



## 14.0 DEADMAN TIMER (DMT)

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Deadman Timer (DMT)**” (DS70005155) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

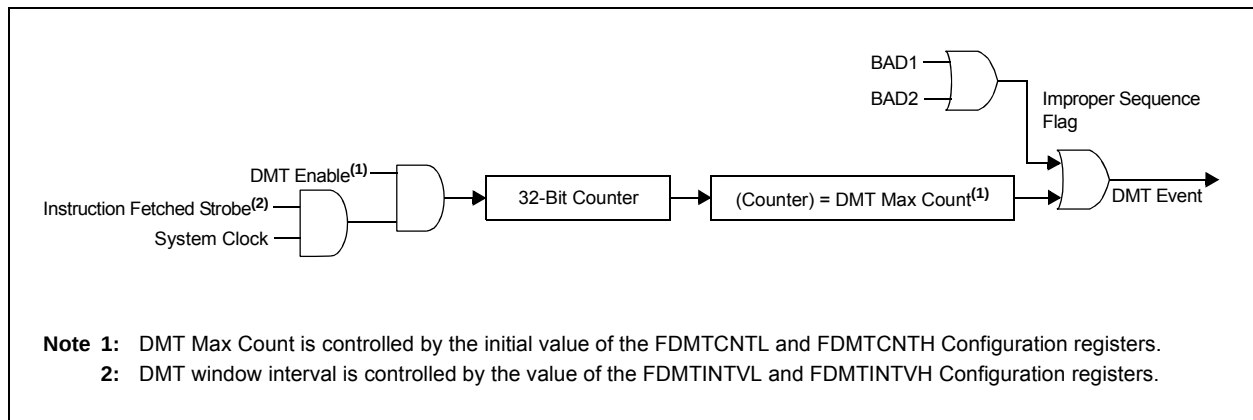
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical, and safety-critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 14-1 shows a block diagram of the Deadman Timer module.

**FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM**



# dsPIC33EVXXXGM00X/10X FAMILY

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NOTES:

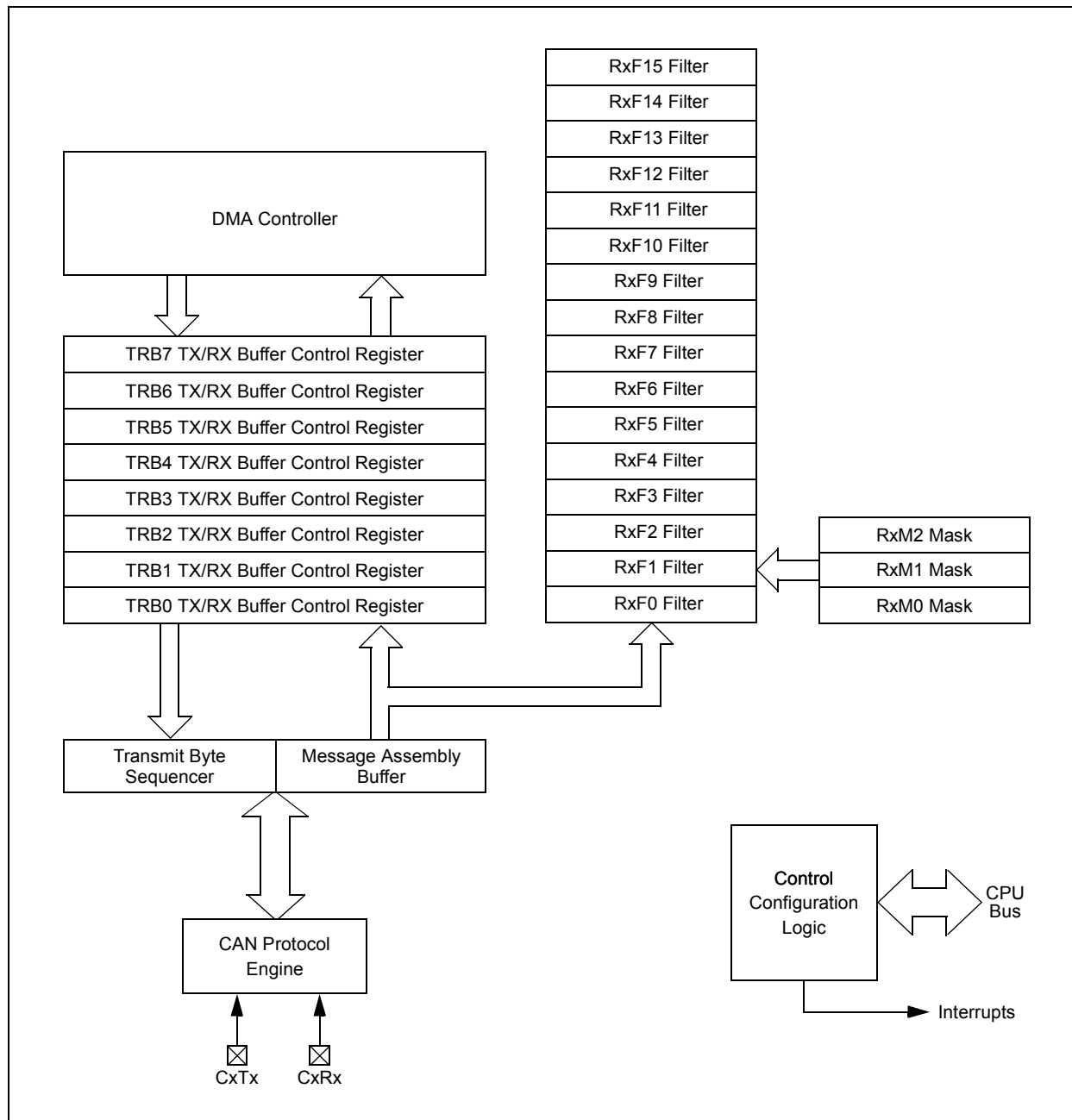
# dsPIC33EVXXXGM00X/10X FAMILY

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NOTES:

# dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 22-1: CANx MODULE BLOCK DIAGRAM



## 22.2 Modes of Operation

The CANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

# dsPIC33EVXXXGM00X/10X FAMILY

## REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

|             |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/C-0       | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<15:8> |       |       |       |       |       |       |       |
| bit 15      |       |       |       | bit 8 |       |       |       |

|            |       |       |       |       |       |       |       |
|------------|-------|-------|-------|-------|-------|-------|-------|
| R/C-0      | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<7:0> |       |       |       |       |       |       |       |
| bit 7      |       |       |       | bit 0 |       |       |       |

|                   |                                                                |                                    |                    |
|-------------------|----------------------------------------------------------------|------------------------------------|--------------------|
| <b>Legend:</b>    | C = Writable bit, but only '0' can be written to clear the bit |                                    |                    |
| R = Readable bit  | W = Writable bit                                               | U = Unimplemented bit, read as '0' |                    |
| -n = Value at POR | '1' = Bit is set                                               | '0' = Bit is cleared               | x = Bit is unknown |

bit 15-0      **RXOVF<15:0>**: Receive Buffer n Overflow bits  
1 = Module attempted to write to a full buffer (set by module)  
0 = No overflow condition (cleared by user software)

## REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

|              |       |       |       |       |       |       |       |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/C-0        | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<31:24> |       |       |       |       |       |       |       |
| bit 15       |       |       |       | bit 8 |       |       |       |

|              |       |       |       |       |       |       |       |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/C-0        | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
| RXOVF<23:16> |       |       |       |       |       |       |       |
| bit 7        |       |       |       | bit 0 |       |       |       |

|                   |                                                                |                                    |                    |
|-------------------|----------------------------------------------------------------|------------------------------------|--------------------|
| <b>Legend:</b>    | C = Writable bit, but only '0' can be written to clear the bit |                                    |                    |
| R = Readable bit  | W = Writable bit                                               | U = Unimplemented bit, read as '0' |                    |
| -n = Value at POR | '1' = Bit is set                                               | '0' = Bit is cleared               | x = Bit is unknown |

bit 15-0      **RXOVF<31:16>**: Receive Buffer n Overflow bits  
1 = Module attempted to write to a full buffer (set by module)  
0 = No overflow condition (cleared by user software)

## 24.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Analog-to-Digital Converter (ADC)**” (DS70621) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site ([www.microchip.com](http://www.microchip.com)).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Analog-to-Digital (ADC) module in the dsPIC33EVXXXGM00X/10X family devices supports up to 36 analog input channels.

The ADC module can be configured by the user as either a 10-bit, 4 Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, 1 S&H ADC.

**Note:** The ADC module needs to be disabled before modifying the AD12B bit.

### 24.1 Key Features

#### 24.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) Conversion
- Conversion Speeds of up to 1.1 Msps
- Up to 36 Analog Input Pins
- Connections to Four Internal Op Amps
- Connections to the Charge Time Measurement Unit (CTMU) and Temperature Measurement Diode
- Simultaneous Sampling of:
  - Up to four analog input pins
  - Four op amp outputs
- Combinations of Analog Inputs and Op Amp Outputs
- Automatic Channel Scan mode
- Selectable Conversion Trigger Source
- Selectable Buffer Fill modes
- Four Result Alignment Options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle Modes

#### 24.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed previously, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration. Therefore, simultaneous sampling of multiple channels is not supported.

The ADC has up to 36 analog inputs. The analog inputs, AN32 through AN63, are multiplexed, thus providing flexibility in using any of these analog inputs in addition to the analog inputs, AN0 through AN31. Since AN32 through AN63 are multiplexed, do not use two channels simultaneously, since it may result in erroneous output from the module. These analog inputs are shared with op amp inputs and outputs, comparator inputs and external voltage references. When op amp/comparator functionality is enabled, the analog input that shares that pin is no longer available. The actual number of analog input pins and op amps depends on the specific device.

A block diagram of the ADC module with connection options is shown in Figure 24-1. Figure 24-2 shows a block diagram of the ADC conversion clock period.

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**REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER**

|        |     |     |     |     |     |     |       |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0    | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0   |
| —      | —   | —   | —   | —   | —   | —   | —     |
| bit 15 |     |     |     |     |     |     | bit 8 |

|       |        |        |        |         |        |        |        |
|-------|--------|--------|--------|---------|--------|--------|--------|
| U-0   | R/W-0  | R/W-0  | R/W-0  | R/W-0   | R/W-0  | R/W-0  | R/W-0  |
| —     | CFSEL2 | CFSEL1 | CFSEL0 | CFLTREN | CFDIV2 | CFDIV1 | CFDIV0 |
| bit 7 |        |        |        |         |        |        | bit 0  |

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator x Filter Input Clock Select bits

111 = T5CLK<sup>(1)</sup>

110 = T4CLK<sup>(2)</sup>

101 = T3CLK<sup>(1)</sup>

100 = T2CLK<sup>(2)</sup>

011 = Reserved

010 = SYNCO1<sup>(3)</sup>

001 = Fosc<sup>(4)</sup>

000 = Fp<sup>(4)</sup>

bit 3 **CFLTREN:** Comparator x Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator x Filter Clock Divide Select bits

111 = Clock divide 1:128

110 = Clock divide 1:64

101 = Clock divide 1:32

100 = Clock divide 1:16

011 = Clock divide 1:8

010 = Clock divide 1:4

001 = Clock divide 1:2

000 = Clock divide 1:1

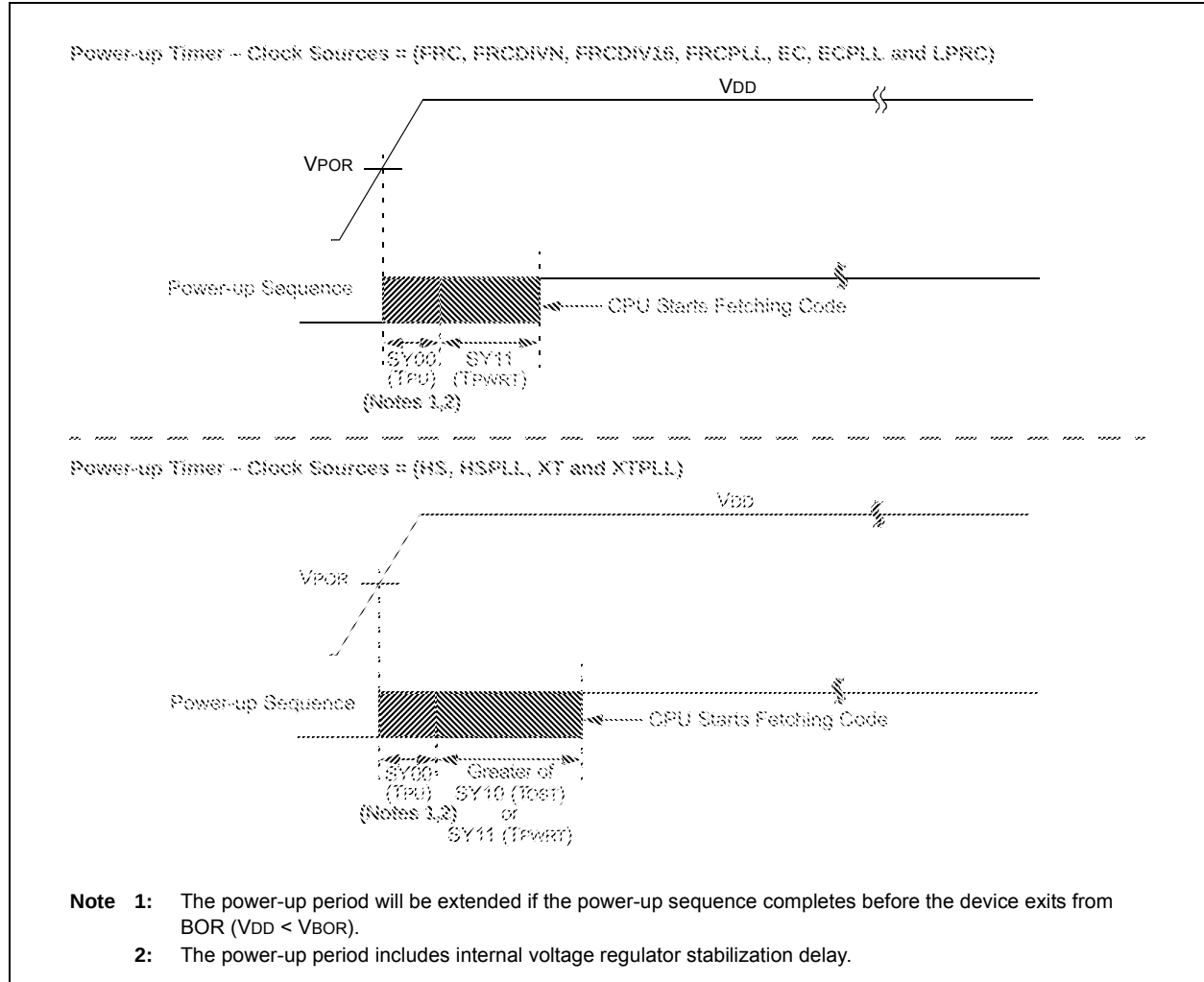
**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).

**2:** See the Type B Timer Block Diagram (Figure 13-1).

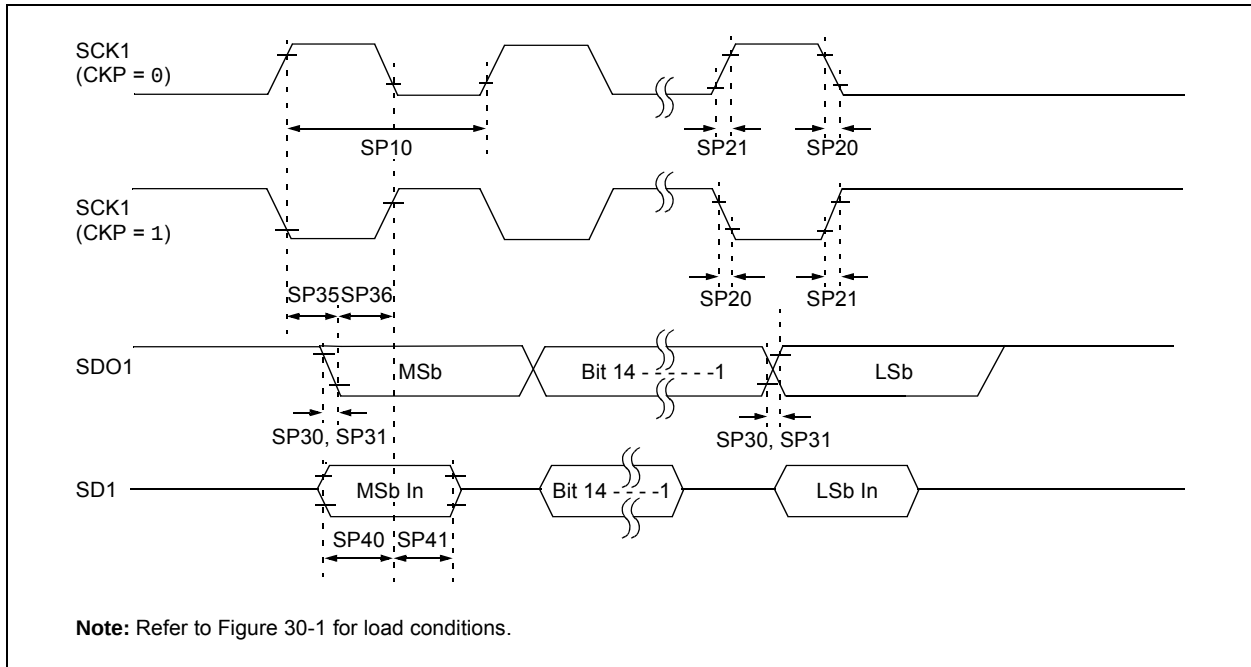
**3:** See the High-Speed PWMx Module Register Interconnection Diagram (Figure 17-2).

**4:** See the Oscillator System Diagram (Figure 9-1).

**FIGURE 30-5: POWER-ON RESET TIMING CHARACTERISTICS**



**FIGURE 30-23: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)  
TIMING CHARACTERISTICS**



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**TABLE 30-57: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS       |        |                                                                      | Standard Operating Conditions (see Note 2): 4.5V to 5.5V<br>(unless otherwise stated)<br>Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial<br>$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended |                     |      |       |                                      |
|--------------------------|--------|----------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|------|-------|--------------------------------------|
| Param No.                | Symbol | Characteristic                                                       | Min.                                                                                                                                                                                                                                                           | Typ. <sup>(4)</sup> | Max. | Units | Conditions                           |
| <b>Clock Parameters</b>  |        |                                                                      |                                                                                                                                                                                                                                                                |                     |      |       |                                      |
| AD50                     | TAD    | ADC Clock Period                                                     | 117.6                                                                                                                                                                                                                                                          | —                   | —    | ns    |                                      |
| AD51                     | trc    | ADC Internal RC Oscillator Period                                    | —                                                                                                                                                                                                                                                              | 250                 | —    | ns    |                                      |
| <b>Conversion Rate</b>   |        |                                                                      |                                                                                                                                                                                                                                                                |                     |      |       |                                      |
| AD55                     | tCONV  | Conversion Time                                                      | —                                                                                                                                                                                                                                                              | 14                  | —    | TAD   |                                      |
| AD56                     | FCNV   | Throughput Rate                                                      | —                                                                                                                                                                                                                                                              | —                   | 500  | ksps  |                                      |
| AD57a                    | TSAMP  | Sample Time when Sampling Any ANx Input                              | 3                                                                                                                                                                                                                                                              | —                   | —    | TAD   |                                      |
| AD57b                    | TSAMP  | Sample Time when Sampling the Op Amp Outputs                         | 3                                                                                                                                                                                                                                                              | —                   | —    | TAD   |                                      |
| <b>Timing Parameters</b> |        |                                                                      |                                                                                                                                                                                                                                                                |                     |      |       |                                      |
| AD60                     | tpCS   | Conversion Start from Sample Trigger <sup>(1)</sup>                  | 2                                                                                                                                                                                                                                                              | —                   | 3    | TAD   | Auto-convert trigger is not selected |
| AD61                     | tpSS   | Sample Start from Setting Sample (SAMP) bit <sup>(1)</sup>           | 2                                                                                                                                                                                                                                                              | —                   | 3    | TAD   |                                      |
| AD62                     | tcSS   | Conversion Completion to Sample Start (ASAM = 1) <sup>(1)</sup>      | —                                                                                                                                                                                                                                                              | 0.5                 | —    | TAD   |                                      |
| AD63                     | tDPU   | Time to Stabilize Analog Stage from ADC Off to ADC On <sup>(1)</sup> | —                                                                                                                                                                                                                                                              | —                   | 20   | μs    | See Note 3                           |

- Note 1:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.
- 2:** Device is functional at  $V_{BORMIN} < V_{DD} < V_{DDMIN}$ , but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.
- 3:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on ( $ADON (ADxCON1<15>) = 1$ ). During this time, the ADC result is indeterminate.
- 4:** These parameters are characterized but not tested in manufacturing.

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## 31.2 AC Characteristics and Timing Parameters

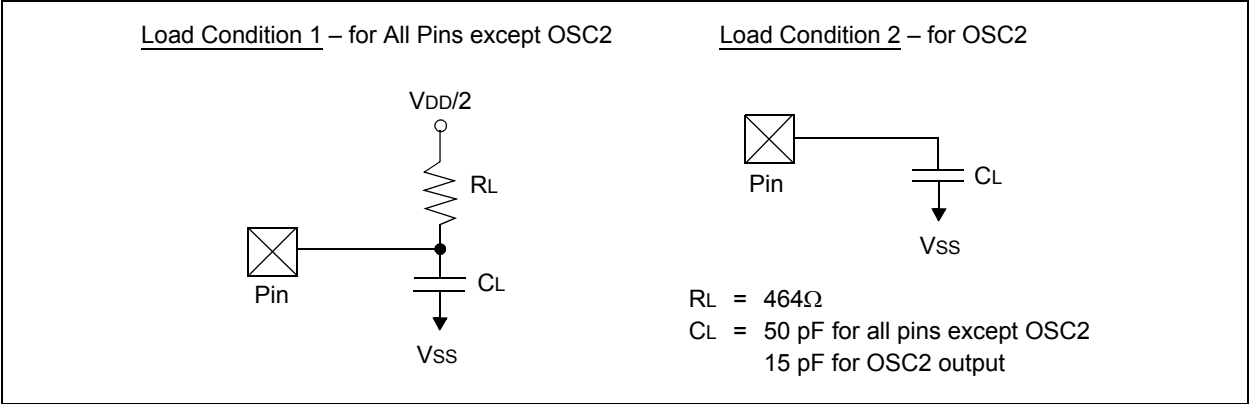
The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 “AC Characteristics and Timing Parameters”**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 “AC Characteristics and Timing Parameters”** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

|                    |                                                                                |
|--------------------|--------------------------------------------------------------------------------|
| AC CHARACTERISTICS | Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)          |
|                    | Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
|                    | Operating voltage VDD range as described in Table 31-1.                        |

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



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FIGURE 32-15: TYPICAL I<sub>DOZE</sub> vs. V<sub>DD</sub> (DOZE 1:128, 70 MIPS)

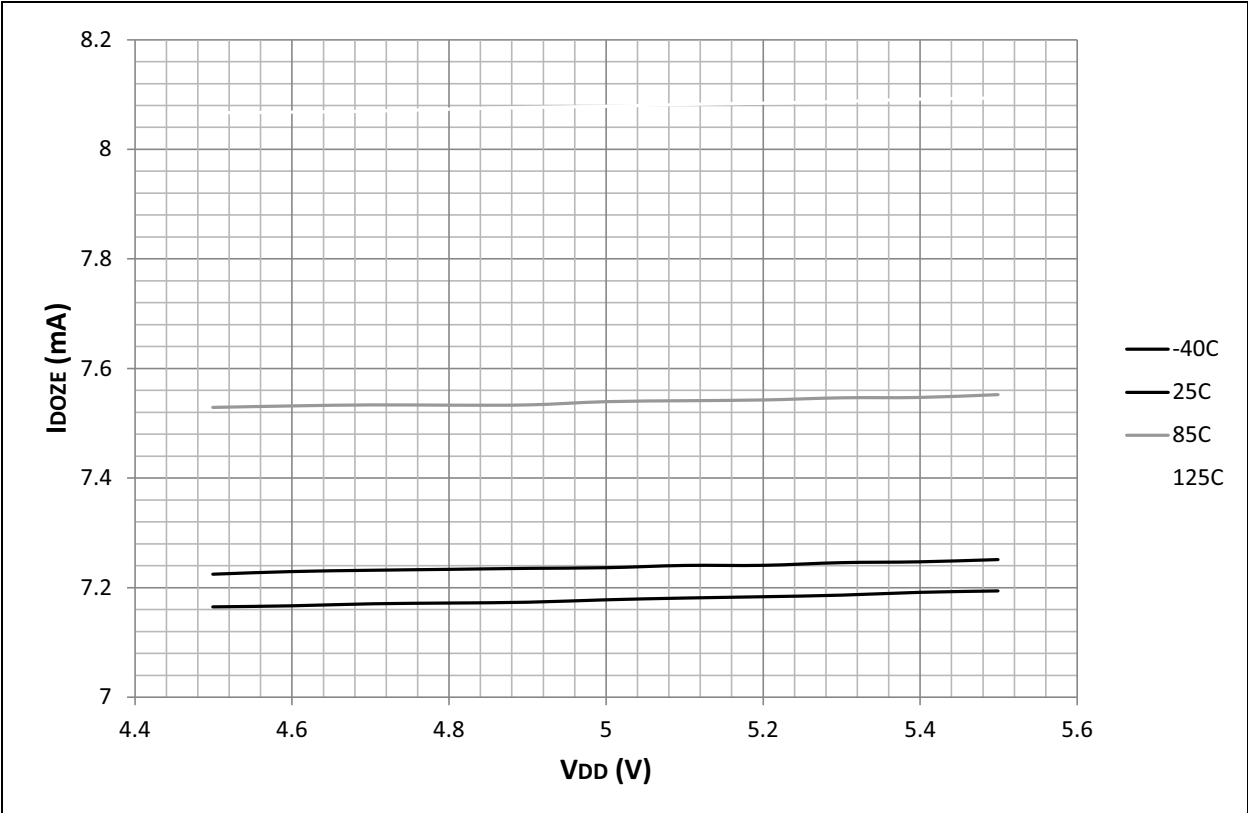
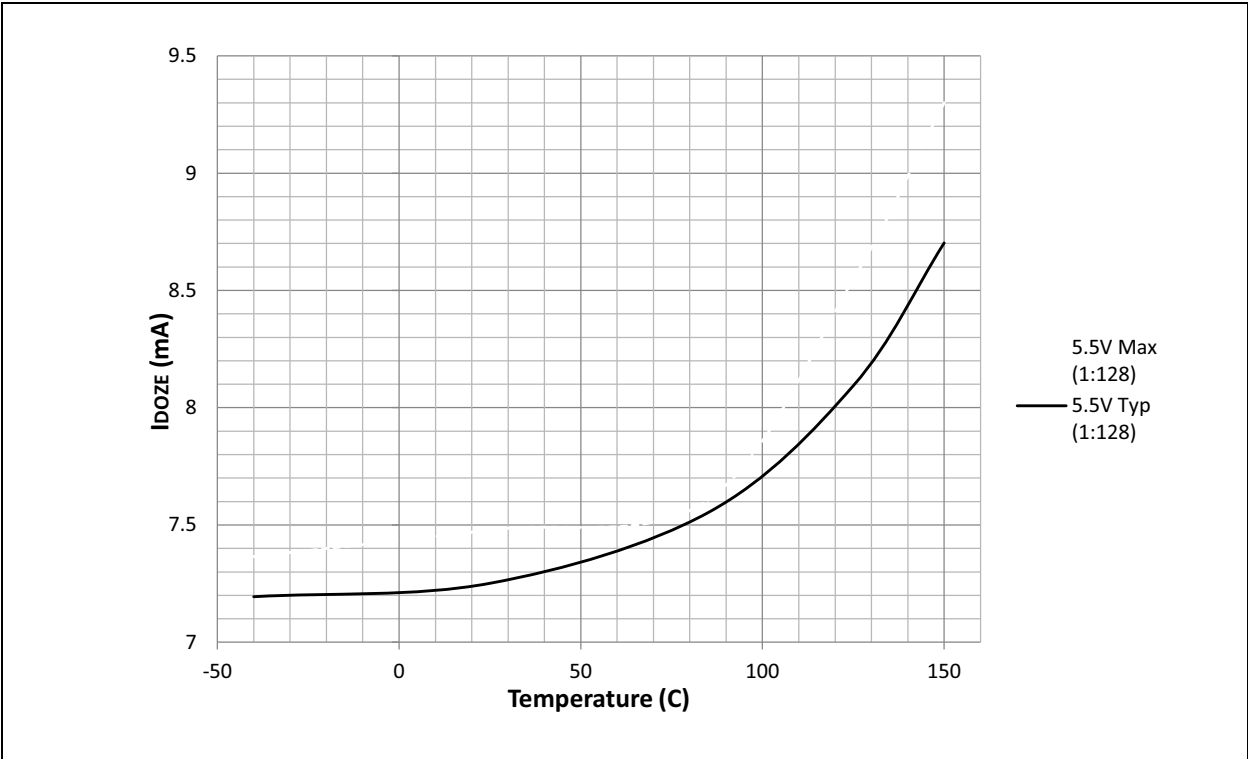
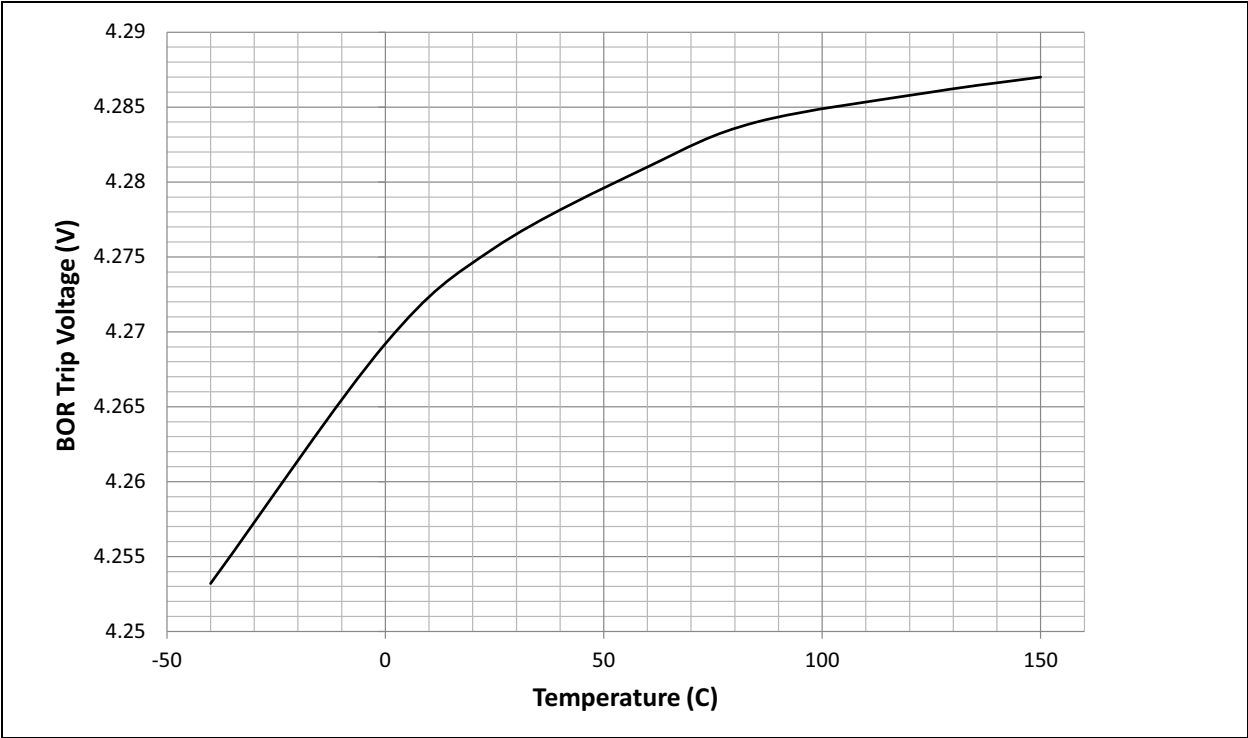


FIGURE 32-16: TYPICAL/MAXIMUM I<sub>DOZE</sub> vs. TEMPERATURE (DOZE 1:128, 70 MIPS)



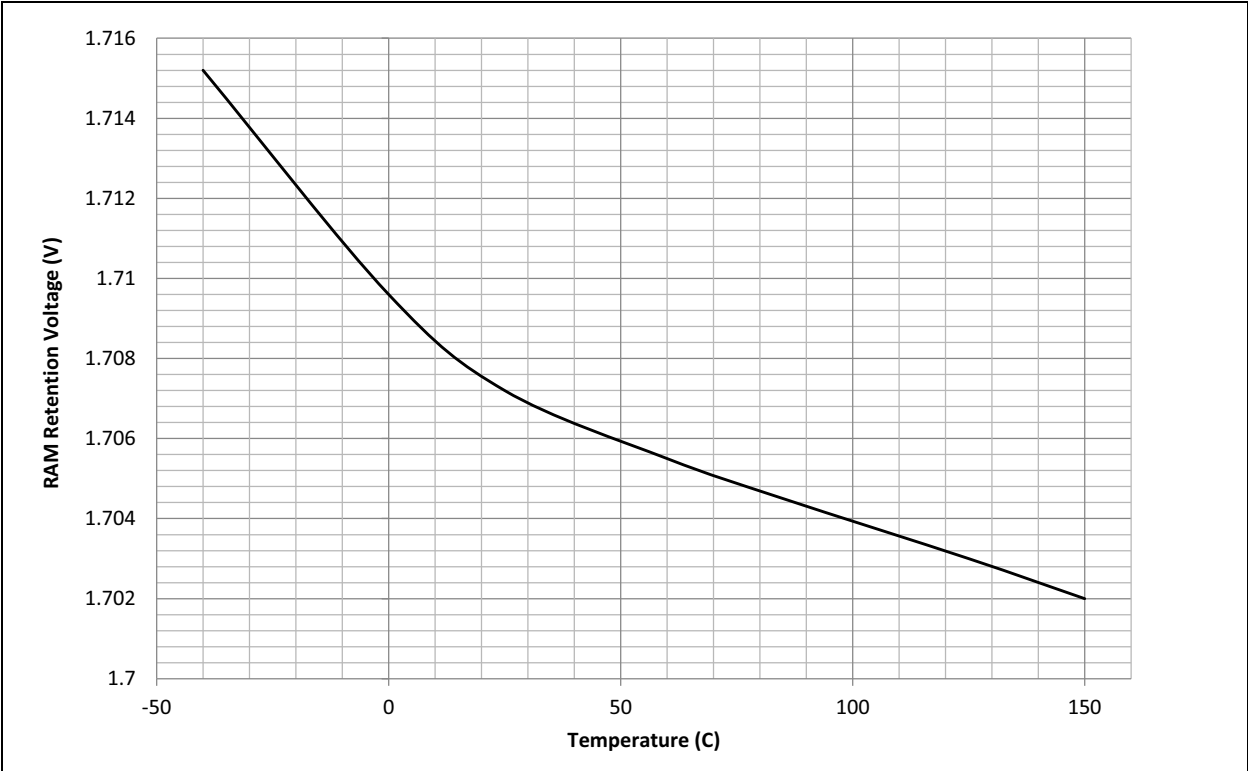
32.12 V<sub>BOR</sub>

FIGURE 32-35: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



32.13 RAM Retention

FIGURE 32-36: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE



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NOTES: