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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm004t-i-ml

dsPIC33EVXXXGM00X/10X FAMILY

4.2.5 X AND Y DATA SPACES

The dsPIC33EVXXXGM00X/10X family core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified, linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X DS is used by all instructions and supports all addressing modes. The X DS has separate read and write data buses. The X read data bus is the read data path for all instructions that view the DS as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y DS is used in concert with the X DS by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSA, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to the X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

TABLE 4-5: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMO	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	UART1 Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMO	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	UART2 Baud Rate Generator Prescaler Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

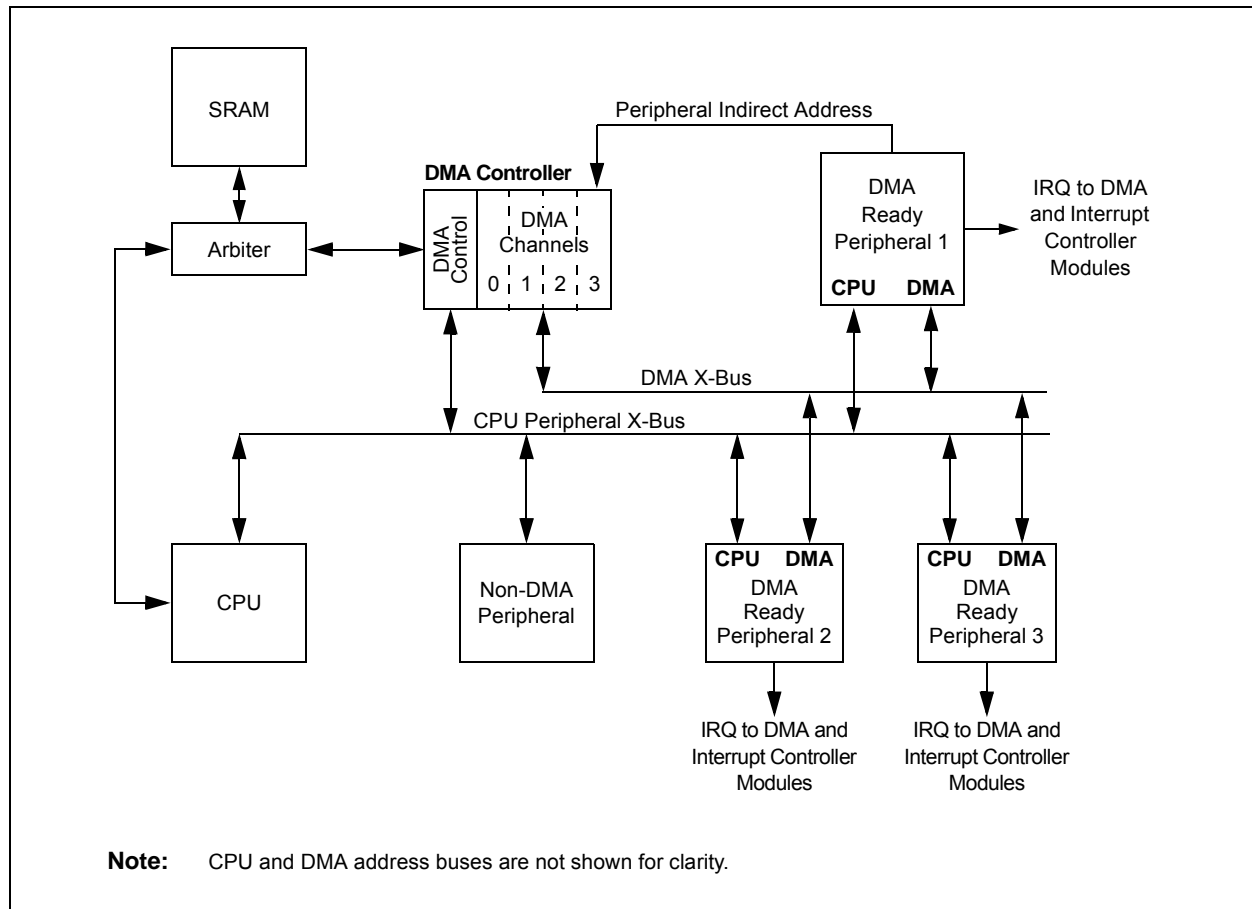
R/W-0	R-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	NSTDIS: Interrupt Nesting Disable bit 1 = Interrupt nesting is disabled 0 = Interrupt nesting is enabled
bit 14	OVAERR: Accumulator A Overflow Trap Flag bit 1 = Trap was caused by overflow of Accumulator A 0 = Trap was not caused by overflow of Accumulator A
bit 13	OVBERR: Accumulator B Overflow Trap Flag bit 1 = Trap was caused by overflow of Accumulator B 0 = Trap was not caused by overflow of Accumulator B
bit 12	COVAERR: Accumulator A Catastrophic Overflow Trap Flag bit 1 = Trap was caused by catastrophic overflow of Accumulator A 0 = Trap was not caused by catastrophic overflow of Accumulator A
bit 11	COVBERR: Accumulator B Catastrophic Overflow Trap Flag bit 1 = Trap was caused by catastrophic overflow of Accumulator B 0 = Trap was not caused by catastrophic overflow of Accumulator B
bit 10	OVATE: Accumulator A Overflow Trap Enable bit 1 = Trap overflow of Accumulator A 0 = Trap is disabled
bit 9	OVBTE: Accumulator B Overflow Trap Enable bit 1 = Trap overflow of Accumulator B 0 = Trap is disabled
bit 8	COVTE: Catastrophic Overflow Trap Enable bit 1 = Trap on catastrophic overflow of Accumulator A or B is enabled 0 = Trap is disabled
bit 7	SFTACERR: Shift Accumulator Error Status bit 1 = Math error trap was caused by an invalid accumulator shift 0 = Math error trap was caused by an invalid accumulator shift
bit 6	DIV0ERR: Divide-by-Zero Error Status bit 1 = Math error trap was caused by a divide-by-zero 0 = Math error trap was not caused by a divide-by-zero
bit 5	DMACERR: DMAC Trap Flag bit 1 = DMAC trap has occurred 0 = DMAC trap has not occurred
bit 4	MATHERR: Math Error Status bit 1 = Math error trap has occurred 0 = Math error trap has not occurred

Figure 8-2 illustrates the DMA Controller block diagram.

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



8.1 DMAC Controller Registers

Each DMAC Channel x (where x = 0 to 3) contains the following registers:

- 16-Bit DMA Channel x Control Register (DMAxCON)
- 16-Bit DMA Channel x IRQ Select Register (DMAxREQ)
- 32-Bit DMA Channel x Start Address Register A High/Low (DMAxSTAH/L)
- 32-Bit DMA Channel x Start Address Register B High/Low (DMAxSTBH/L)
- 16-Bit DMA Channel x Peripheral Address Register (DMAxPAD)
- 14-Bit DMA Channel x Transfer Count Register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADRH/L) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The DMA Interrupt Flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding DMA Interrupt Enable bits (DMAxIE) are located in an IECx register in the interrupt controller and the corresponding DMA Interrupt Priority bits (DMAxIP) are located in an IPCx register in the interrupt controller.

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NOTES:

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REGISTER 10-7: PMD8: PERIPHERAL MODULE DISABLE CONTROL REGISTER 8

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	—	—	SENT2MD	SENT1MD	—	—	DMTMD
bit 15			bit 8				

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **SENT2MD:** SENT2 Module Disable bit

1 = SENT2 module is disabled

0 = SENT2 module is enabled

bit 11 **SENT1MD:** SENT1 Module Disable bit

1 = SENT1 module is disabled

0 = SENT1 module is enabled

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **DMTMD:** Deadman Timer Disable bit

1 = Deadman Timer is disabled

0 = Deadman Timer is enabled

bit 7-0 **Unimplemented:** Read as '0'

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11.8 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1R<7:0>							
bit 15							
bit 8							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							
bit 0							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **INT1R<7:0>**: Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•

•

•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

bit 7-0 **Unimplemented**: Read as '0'

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2R<7:0>							
bit 7							
bit 0							

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented**: Read as '0'

bit 7-0 **INT2R<7:0>**: Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•

•

•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

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REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **SCK2R<7:0>**: Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•
•
•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

bit 7-0 **SDI2R<7:0>**: Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181

•
•
•

00000001 = Input tied to CMP1

00000000 = Input tied to Vss

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REGISTER 14-11: DMTHOLDREG: DMT HOLD REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<15:8>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT<7:0>							
bit 7							
bit 0							

Legend:							
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at POR		'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	

bit 15-0 **UPRCNT<15:0>**: Value of the DMTCNTH register when DMTCNTL and DMTCNTH were Last Read bits

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>**: Input Source Select for Synchronization and Trigger Operation bits⁽⁴⁾

11111 = Reserved
11110 = Reserved
11101 = Reserved
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization⁽⁵⁾
11010 = Analog Comparator 3 is the source for the capture timer synchronization⁽⁵⁾
11001 = Analog Comparator 2 is the source for the capture timer synchronization⁽⁵⁾
11000 = Analog Comparator 1 is the source for the capture timer synchronization⁽⁵⁾
10111 = Analog Comparator 5 is the source for the capture timer synchronization⁽⁵⁾
10110 = Analog Comparator 4 is the source for the capture timer synchronization⁽⁵⁾
10101 = Reserved
10100 = Reserved
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = Reserved
01001 = Reserved
01000 = Input Capture 4 is the source for the capture timer synchronization⁽⁶⁾
00111 = Input Capture 3 is the source for the capture timer synchronization⁽⁶⁾
00110 = Input Capture 2 is the source for the capture timer synchronization⁽⁶⁾
00101 = Input Capture 1 is the source for the capture timer synchronization⁽⁶⁾
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Reserved

- Note 1:** The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by the SYNCSEL<4:0> bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own sync or trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

19.2 I²C Control Registers

REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/S-1	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL ⁽¹⁾	STRICT	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **I2CEN:** I2Cx Enable bit (writable from SW only)
 1 = Enables the I²C module and configures the SDAx and SCLx pins as serial port pins
 0 = Disables the I²C module and all I²C pins are controlled by port functions
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
 1 = Discontinues module operation when the device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **SCLREL:** SCLx Release Control bit (I²C Slave mode only)⁽¹⁾
 Module resets and (I2CEN = 0) sets SCLREL = 1.
If STREN = 0:⁽²⁾
 1 = Releases clock
 0 = Forces clock low (clock stretch)
If STREN = 1:
 1 = Releases clock
 0 = Holds clock low (clock stretch); user may program this bit to '0', clock stretch at the next SCLx low
- bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
 1 = Strict reserved addressing is enforced
 In Slave mode, the device does not respond to reserved address space and addresses falling in that category are NACKed.
 0 = Reserved addressing would be Acknowledged
 In Slave mode, the device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK.
- bit 10 **A10M:** 10-Bit Slave Address Flag bit
 1 = I2CxADD is a 10-bit slave address
 0 = I2CxADD is a 7-bit slave address
- bit 9 **DISSLW:** Slew Rate Control Disable bit
 1 = Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
 0 = Slew rate control is enabled for High-Speed mode (400 kHz)
- bit 8 **SMEN:** SMBus Input Levels Enable bit
 1 = Enables the input logic so thresholds are compliant with the SMBus specification
 0 = Disables the SMBus-specific inputs

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

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BUFFER 22-3: CANx MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-10 **EID<5:0>**: Extended Identifier bits
- bit 9 **RTR**: Remote Transmission Request bit
 When IDE = 1:
 1 = Message will request remote transmission
 0 = Normal message
 When IDE = 0:
 The RTR bit is ignored.
- bit 8 **RB1**: Reserved Bit 1
 User must set this bit to '0' per CAN protocol.
- bit 7-5 **Unimplemented**: Read as '0'
- bit 4 **RB0**: Reserved Bit 0
 User must set this bit to '0' per CAN protocol.
- bit 3-0 **DLC<3:0>**: Data Length Code bits

BUFFER 22-4: CANx MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-8 **Byte 1<15:8>**: CANx Message Byte 1 bits
- bit 7-0 **Byte 0<7:0>**: CANx Message Byte 0 bits

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TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Program Flash Memory							
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	4.5	—	5.5	V	
D132b	VPEW	VDD for Self-Timed Write	4.5	—	5.5	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current During Programming	—	10	—	mA	
D136a	TRW	Row Write Cycle Time	0.657	—	0.691	ms	TRW = 4965 FRC cycles, TA = +85°C (see Note 2)
D136b	TRW	Row Write Cycle Time	0.651	—	0.698	ms	TRW = 4965 FRC cycles, TA = +125°C (see Note 2)
D137a	TPE	Page Erase Time	19.44	—	20.44	ms	TPE = 146893 FRC cycles, TA = +85°C (see Note 2)
D137b	TPE	Page Erase Time	19.24	—	20.65	ms	TPE = 146893 FRC cycles, TA = +125°C (see Note 2)
D138a	TWW	Word Write Cycle Time	45.78	—	48.15	μs	TWW = 346 FRC cycles, TA = +85°C (see Note 2)
D138b	TWW	Word Write Cycle Time	45.33	—	48.64	μs	TWW = 346 FRC cycles, TA = +125°C (see Note 2)

Note 1: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.3728 MHz, TUN<5:0> = b' 011111 (for Min), TUN<5:0> = b' 100000 (for Max). This parameter depends on the FRC accuracy (see Table 30-20) and the value of the FRC Oscillator Tuning register.

TABLE 30-14: ELECTRICAL CHARACTERISTICS: INTERNAL BAND GAP REFERENCE VOLTAGE

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DVR10	VBG	Internal Band Gap Reference Voltage	1.14	1.2	1.26	V	

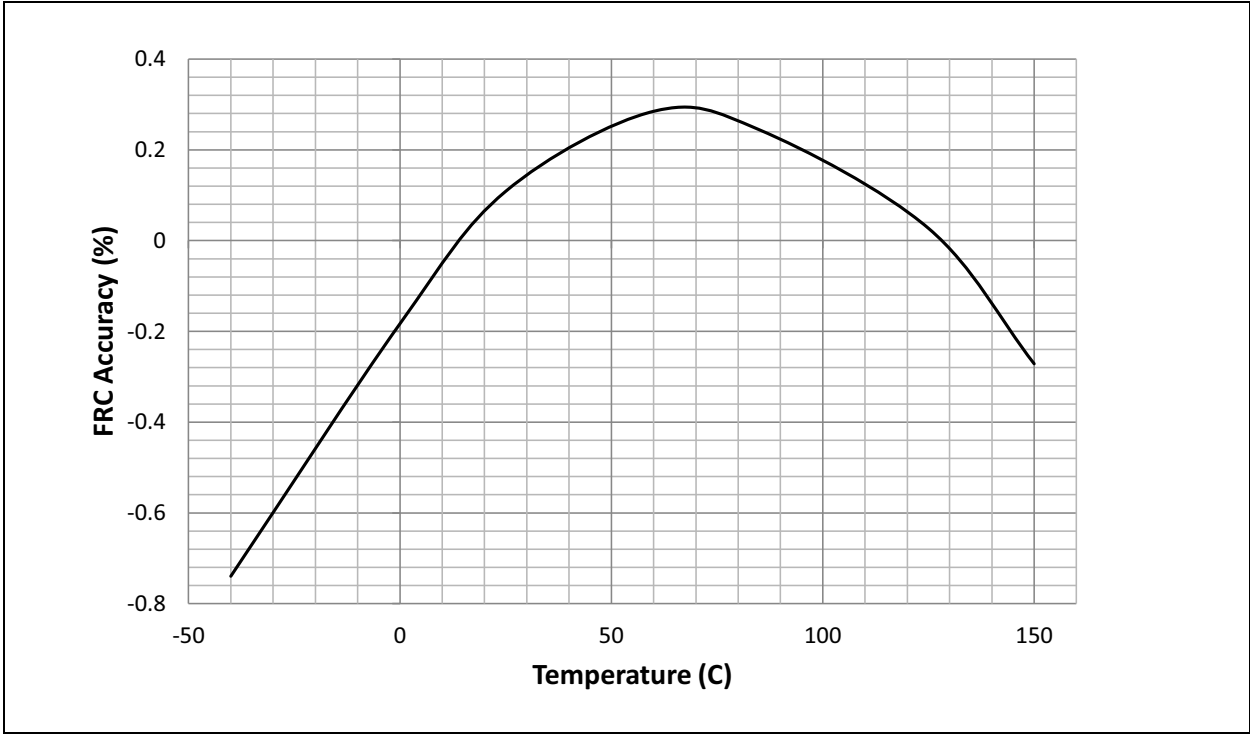
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**TABLE 30-41: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1)
TIMING REQUIREMENTS**

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	-40°C to +125°C and see Note 3
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and Note 4
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and Note 4
SP35	Tsch2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sch, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2sch, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	

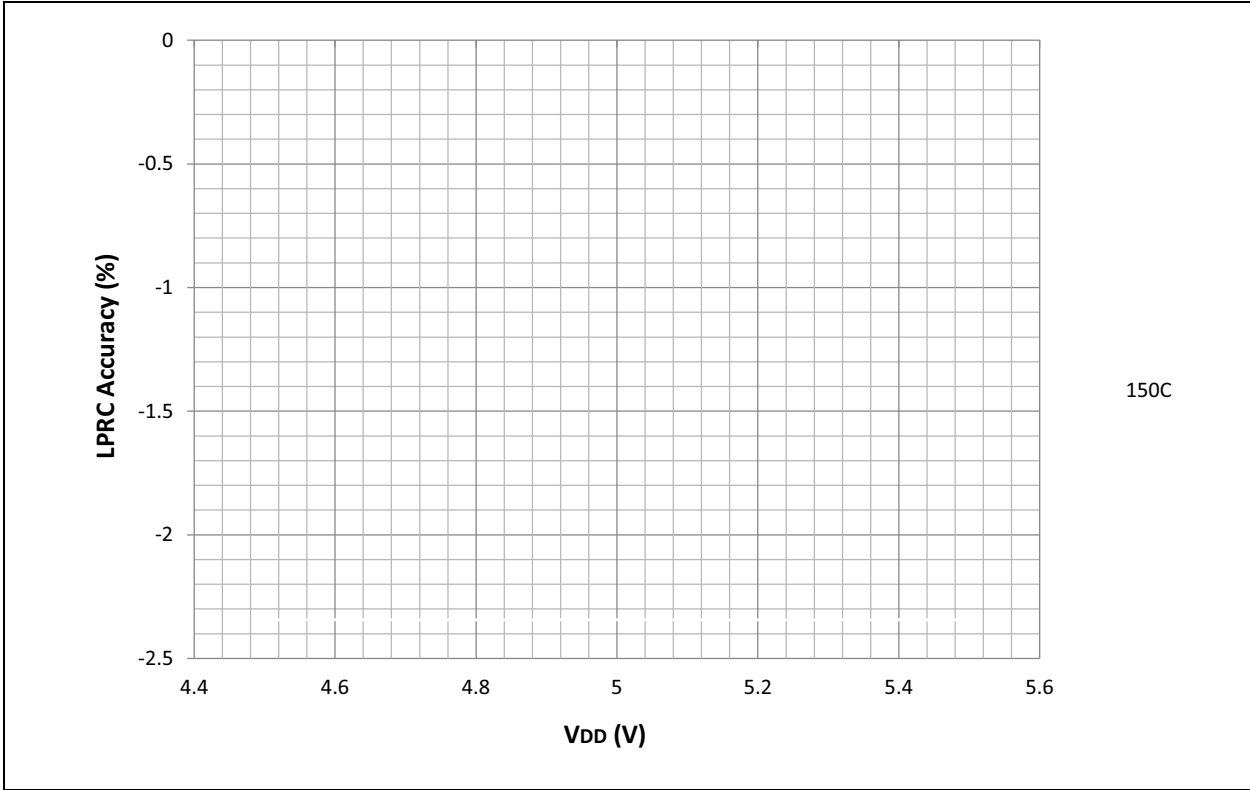
- Note 1:** These parameters are characterized but not tested in manufacturing.
Note 2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.
Note 3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.
Note 4: Assumes 50 pF load on all SPI1 pins.

FIGURE 33-17: TYPICAL FRC ACCURACY vs. TEMPERATURE (5.5V VDD)



33.6 LPRC

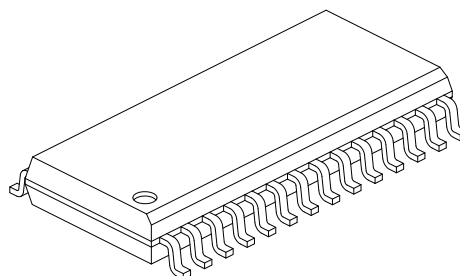
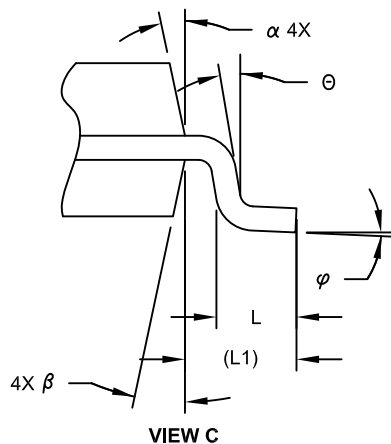
FIGURE 33-18: TYPICAL LPRC ACCURACY vs. VDD



dsPIC33EVXXXGM00X/10X FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	17.90 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

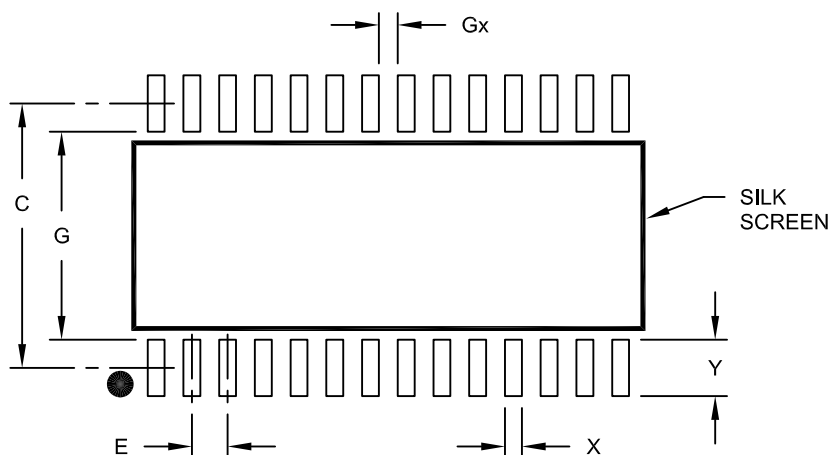
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

dsPIC33EVXXXGM00X/10X FAMILY

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

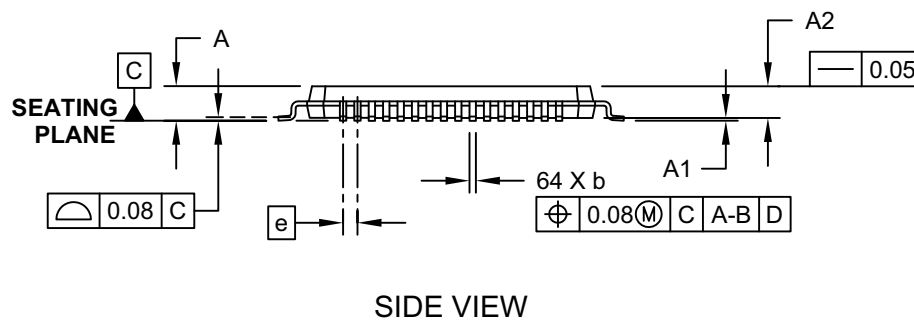
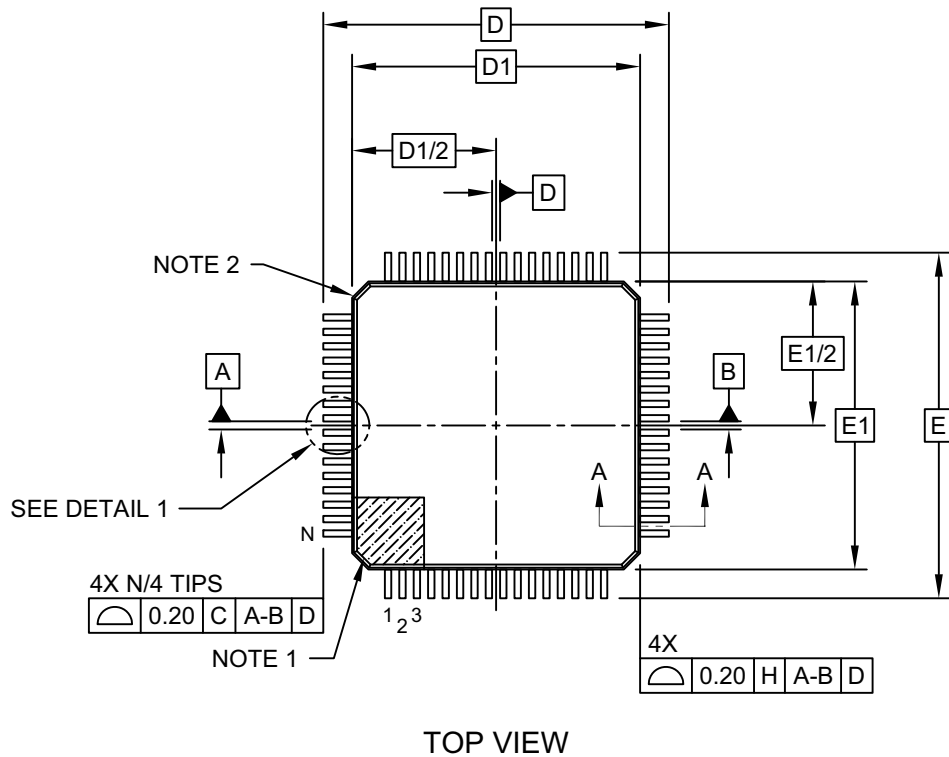
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

dsPIC33EVXXXGM00X/10X FAMILY

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



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