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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm006-e-pt

dsPIC33EVXXGM00X/10X FAMILY

Timers/Output Compare/Input Capture

- Nine General Purpose Timers:
 - Five 16-bit and up to two 32-bit timers/counters; Timer3 can provide ADC trigger
- Four Output Compare modules Configurable as Timers/Counters
- Four Input Capture modules

Communication Interfaces

- Two Enhanced Addressable Universal Asynchronous Receiver/Transmitter (UART) modules (6.25 Mbps):
 - With support for LIN/J2602 bus and IrDA®
 - High and low speed (SCI)
- Two SPI modules (15 Mbps):
 - 25 Mbps data rate without using PPS
- One I²C module (up to 1 Mbaud) with SMBus Support
- Two SENT J2716 (Single-Edge Nibble Transmission-Transmit/Receive) module for Automotive Applications
- One CAN module:
 - 32 buffers, 16 filters and three masks

Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, Serial Peripheral Interface (SPI), ADC, Input Capture, Output Compare and Controller Area Network (CAN)

Input/Output

- GPIO Registers to Support Selectable Slew Rate I/Os
- Peripheral Pin Select (PPS) to allow Function Remap
- Sink/Source: 8 mA or 12 mA, Pin-Specific for Standard VOH/VOL
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Change Notice Interrupts on All I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: -40°C to +125°C) Compliant
- AEC-Q100 REVG (Grade 0: -40°C to +150°C) Compliant
- Class B Safety Library, IEC 60730

Class B Fault Handling Support

- Backup FRC
- Windowed WDT uses LPRC
- Windowed Deadman Timer (DMT) uses System Clock (System Windowed Watchdog Timer)
- H/W Clock Monitor Circuit
- Oscillator Frequency Monitoring through CTMU (OSCI, SYSCLK, FRC, BFRC, LPRC)
- Dedicated PWM Fault Pin
- Lockable Clock Configuration

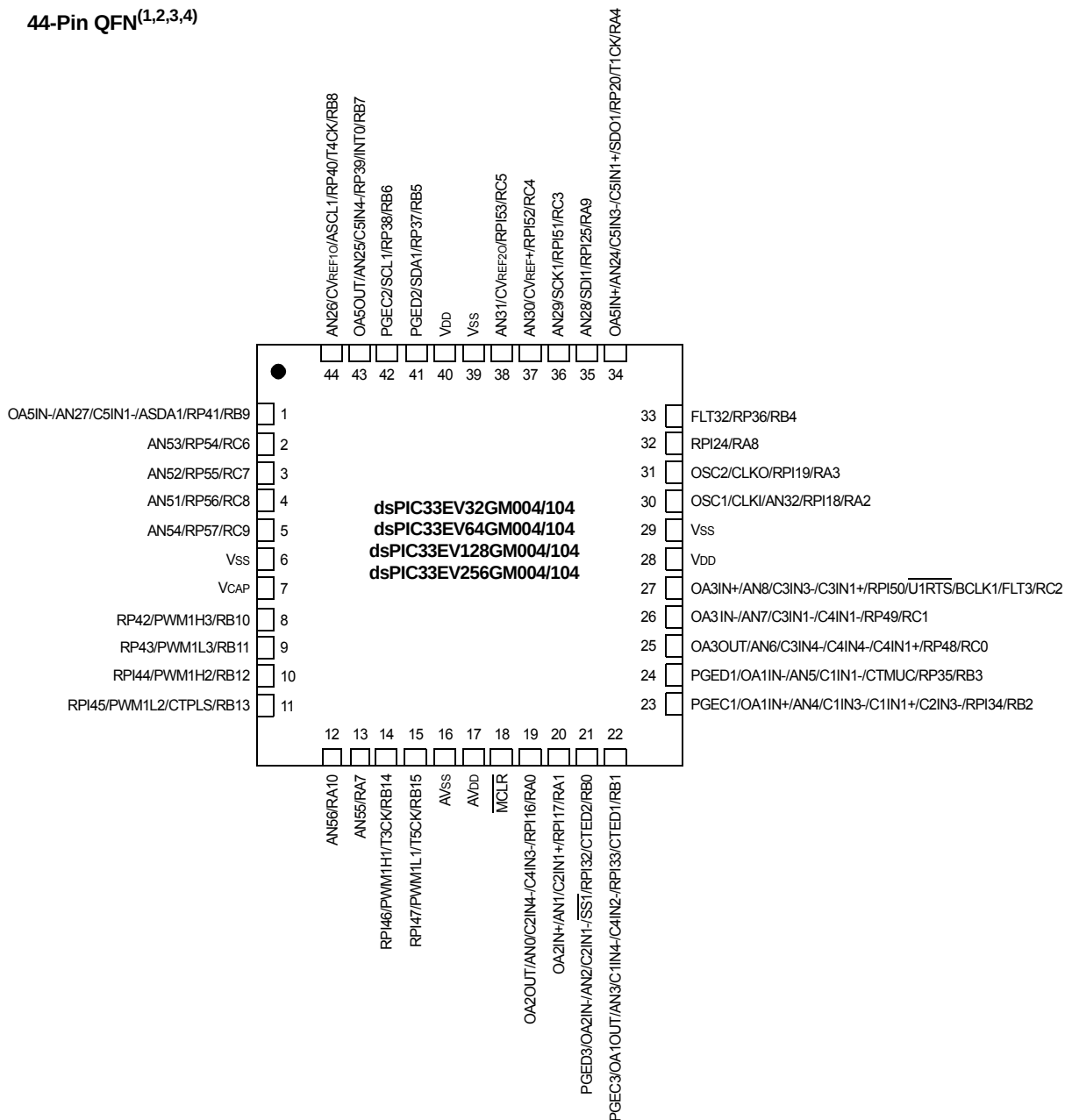
Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- Trace and Run-Time Watch

dsPIC33EVXXXGM00X/10X FAMILY

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3,4)



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.5 “Peripheral Pin Select (PPS)”** for available peripherals and information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAX input is used; otherwise, the ANx input is used.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

3.5 Programmer's Model

The programmer's model for the dsPIC33EVXXXGM00X/10X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EVXXXGM00X/10X family devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15 ⁽¹⁾	Working Register Array
W0 through W14 ⁽¹⁾	Alternate Working Register Array 1
W0 through W14 ⁽¹⁾	Alternate Working Register Array 2
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	D0 Loop Count Register
DOSTARTH ⁽²⁾ , DOSTARTL ⁽²⁾	D0 Loop Start Address Register (High and Low)
DOENDH, DOENDL	D0 Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, D0 Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represents the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

TABLE 4-29: PWM GENERATOR 2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0C40	FLTSTAT	CLSTAT	TRGSTAT	FLTIE	CLIE	TRGIE	ITB	MDCS	DTC1	DTC0	DTCP	—	—	CAM	XPRES	IUE	0000
IOCON2	0C42	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVREN	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON2	0C44	—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC2	0C46	PDC2<15:0>																0000
PHASE2	0C48	PHASE2<15:0>																0000
DTR2	0C4A	—	—	DTR2<13:0>														0000
ALTDTR2	0C4C	—	—	ALTDTR2<13:0>														0000
TRIG2	0C52	TRGCM2<15:0>																0000
TRGCON2	0C54	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	—	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
PWMCAP2	0C58	PWMCAP2<15:0>																0000
LEBCON2	0C5A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY2	0C5C	—	—	—	—	LEB<11:0>												0000
AUXCON2	0C5E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PWM GENERATOR 3 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0C60	FLTSTAT	CLSTAT	TRGSTAT	FLTIE	CLIE	TRGIE	ITB	MDCS	DTC1	DTC0	DTCP	—	—	CAM	XPRES	IUE	0000
IOCON3	0C62	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVREN	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON3	0C64	—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC3	0C66	PDC3<15:0>																0000
PHASE3	0C68	PHASE3<15:0>																0000
DTR3	0C6A	—	—	DTR3<13:0>														0000
ALTDTR3	0C6C	—	—	ALTDTR3<13:0>														0000
TRIG3	0C72	TRGCM3<15:0>																0000
TRGCON3	0C74	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	—	—	TRGSTR5	TRGSTR4	TRGSTR3	TRGSTR2	TRGSTR1	TRGSTR0	0000
PWMCAP3	0C78	PWMCAP3<15:0>																0000
LEBCON3	0C7A	PHR	PHF	PLR	PLF	FLTEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY3	0C7C	—	—	—	—	LEB<11:0>												0000
AUXCON3	0C7E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA<12:7>						—	—	TRISA4	—	—	TRISA<1:0>		1F93
PORTA	0E02	—	—	—	RA<12:7>						—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	—	—	—	LATA<12:7>						—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	—	—	—	ODCA<12:7>						—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	—	—	—	CNIEA<12:7>						—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	—	—	—	CNPUA<12:7>						—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	—	—	—	CNPDA<12:7>						—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	—	—	—	ANSA<12:9>				—	ANSA7	—	—	ANSA4	—	—	ANSA<1:0>		1E93
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA<10:7>				—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	RA<10:7>				—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	LATA<10:7>				—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	ODCA<10:7>				—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	CNIEA<10:7>				—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	CNPUA<10:7>				—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	CNPDA<10:7>				—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	ANSA<10:9>		—	ANSA7	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA<4:0>					DF9F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA<4:0>					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA<4:0>					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA<4:0>					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA<4:0>					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA<4:0>					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA<4:0>					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	ANSA<2:0>			1813
SR1A	0E10	—	—	—	—	—	—	—	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	—	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets	
TRISB	0E14	TRISB<15:0>																	FFFF
PORTB	0E16	RB<15:0>																	xxxx
LATB	0E18	LATB<15:0>																	xxxx
ODCB	0E1A	ODCB<15:0>																	0000
CNENB	0E1C	CNIEB<15:0>																	0000
CNPUB	0E1E	CNPUB<15:0>																	0000
CNPDB	0E20	CNPDB<15:0>																	0000
ANSELB	0E22	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				038F	
SR1B	0E24	—	—	—	—	—	—	SR1B<9:7>			—	—	SR1B4	—	—	—	—	0000	
SR0B	0E26	—	—	—	—	—	—	SR0B<9:7>			—	—	SR0B4	—	—	—	—	0000	

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

11.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “I/O Ports” (DS70000598) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. All the pins in the device are 5V tolerant pins.

11.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of

the I/O pin. The logic also prevents “loop through”, in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

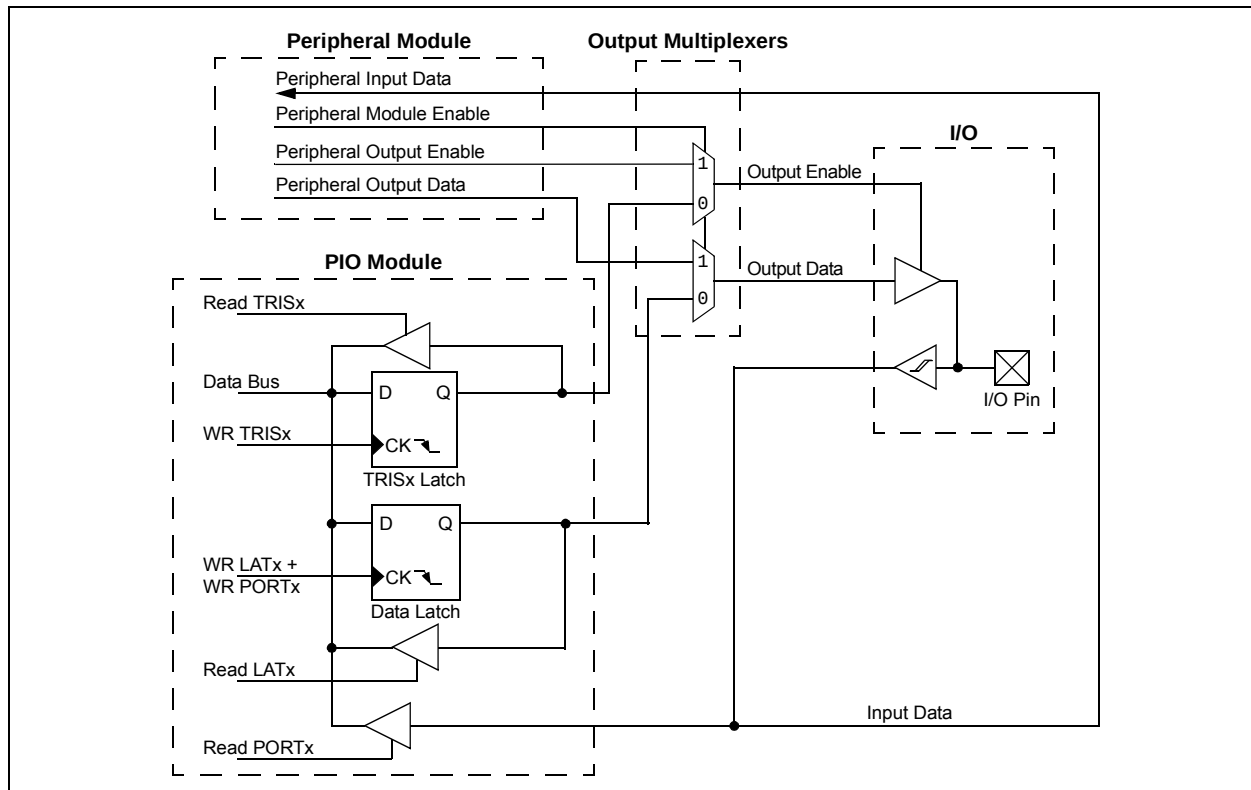
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a ‘1’, then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch; writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means that the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port, because there is no other competing source of output.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



dsPIC33EVXXXGM00X/10X FAMILY

15.1 Input Capture Control Registers

REGISTER 15-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15						bit 8	

U-0	R/W-0	R/W-0	R-0, HC, HS	R-0, HC, HS	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7						bit 0	

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **ICSIDL:** Input Capture x Stop in Idle Mode Control bit
1 = Input Capture x will halt in CPU Idle mode
0 = Input Capture x will continue to operate in CPU Idle mode
- bit 12-10 **ICTSEL<2:0>:** Input Capture x Timer Select bits
111 = Peripheral clock (FP) is the clock source of the ICx
110 = Reserved
101 = Reserved
100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
011 = T5CLK is the clock source of the ICx
010 = T4CLK is the clock source of the ICx
001 = T2CLK is the clock source of the ICx
000 = T3CLK is the clock source of the ICx
- bit 9-7 **Unimplemented:** Read as '0'
- bit 6-5 **ICI<1:0>:** Number of Captures per Interrupt Select bits (this field is not used if ICM<2:0> = 001 or 111)
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event
- bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input Capture x buffer overflow has occurred
0 = Input Capture x buffer overflow has not occurred
- bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
1 = Input Capture x buffer is not empty, at least one more capture value can be read
0 = Input Capture x buffer is empty
- bit 2-0 **ICM<2:0>:** Input Capture x Mode Select bits
111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
110 = Unused (module is disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every edge, rising and falling (Edge Detect mode (ICI<1:0>) is not used in this mode)
000 = Input Capture x module is turned off

dsPIC33EVXXXGM00X/10X FAMILY

REGISTER 22-13: CxBUFPNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F7BP<3:0>**: RX Buffer Mask for Filter 7 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•
•
•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>**: RX Buffer Mask for Filter 6 bits (same values as bits 15-12)

bit 7-4 **F5BP<3:0>**: RX Buffer Mask for Filter 5 bits (same values as bits 15-12)

bit 3-0 **F4BP<3:0>**: RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be ‘1111 1111 1111 1111’. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing ‘1’s to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions $\in \{W4 * W4, W5 * W5, W6 * W6, W7 * W7\}$
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions $\in \{W4 * W5, W4 * W6, W4 * W7, W5 * W6, W5 * W7, W6 * W7\}$
Wn	One of 16 Working registers $\in \{W0...W15\}$
Wnd	One of 16 Destination Working registers $\in \{W0...W15\}$
Wns	One of 16 Source Working registers $\in \{W0...W15\}$
WREG	W0 (Working register used in file register instructions)
Ws	Source W register $\in \{Ws, [Ws], [Ws++] , [Ws--], [++Ws], [--Ws] \}$
Wso	Source W register $\in \{Wns, [Wns], [Wns++] , [Wns--], [++Wns], [--Wns], [Wns+Wb] \}$
Wx	X Data Space Prefetch Address register for DSP instructions $\in \{[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], \text{none}\}$
Wxd	X Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$
Wy	Y Data Space Prefetch Address register for DSP instructions $\in \{[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], \text{none}\}$
Wyd	Y Data Space Prefetch Destination register for DSP instructions $\in \{W4...W7\}$

29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

29.9 PICkit 3 In-Circuit Debugger/Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

dsPIC33EVXXXGM00X/10X FAMILY

TABLE 31-19: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (10-Bit Mode)							
HAD20b	Nr	Resolution	10 data bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	$V_{\text{INL}} = V_{\text{AVSS}} = V_{\text{VREFL}} = 0\text{V}$, $V_{\text{AVDD}} = V_{\text{VREFH}} = 5.5\text{V}$
HAD22b	DNL	Differential Nonlinearity	≥ 1	—	< 1	LSb	$V_{\text{INL}} = V_{\text{AVSS}} = V_{\text{VREFL}} = 0\text{V}$, $V_{\text{AVDD}} = V_{\text{VREFH}} = 5.5\text{V}$
HAD23b	GERR	Gain Error	1	3	6	LSb	$V_{\text{INL}} = V_{\text{AVSS}} = V_{\text{VREFL}} = 0\text{V}$, $V_{\text{AVDD}} = V_{\text{VREFH}} = 5.5\text{V}$
HAD24b	EOFF	Offset Error	1	2	4	LSb	$V_{\text{INL}} = V_{\text{AVSS}} = V_{\text{VREFL}} = 0\text{V}$, $V_{\text{AVDD}} = V_{\text{VREFH}} = 5.5\text{V}$

Note 1: Device is functional at $V_{\text{BORMIN}} < V_{\text{DD}} < V_{\text{DDMIN}}$, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

32.0 CHARACTERISTICS FOR INDUSTRIAL/EXTENDED TEMPERATURE DEVICES (-40°C TO +125°C)

32.1 I_{DD}

FIGURE 32-1: TYPICAL/MAXIMUM I_{DD} vs. F_{osc} (EC MODE, 10 MHz TO 70 MHz, 5.5V MAX)

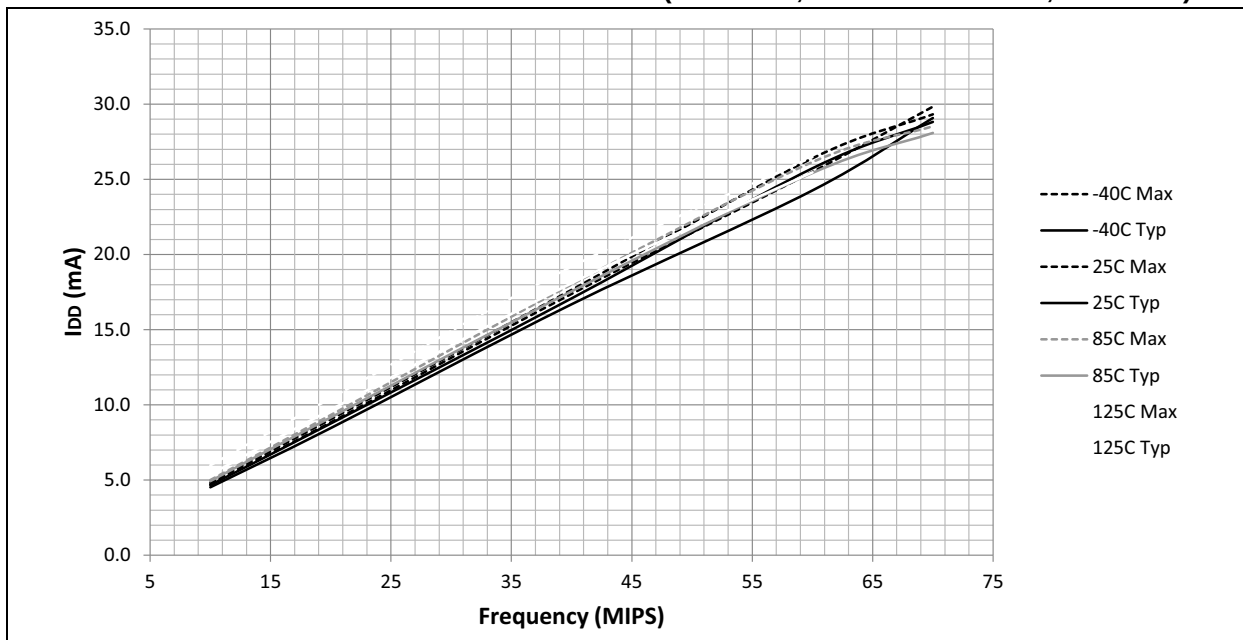


FIGURE 32-2: TYPICAL I_{DD} vs. V_{DD} (EC MODE, 10 MIPS)

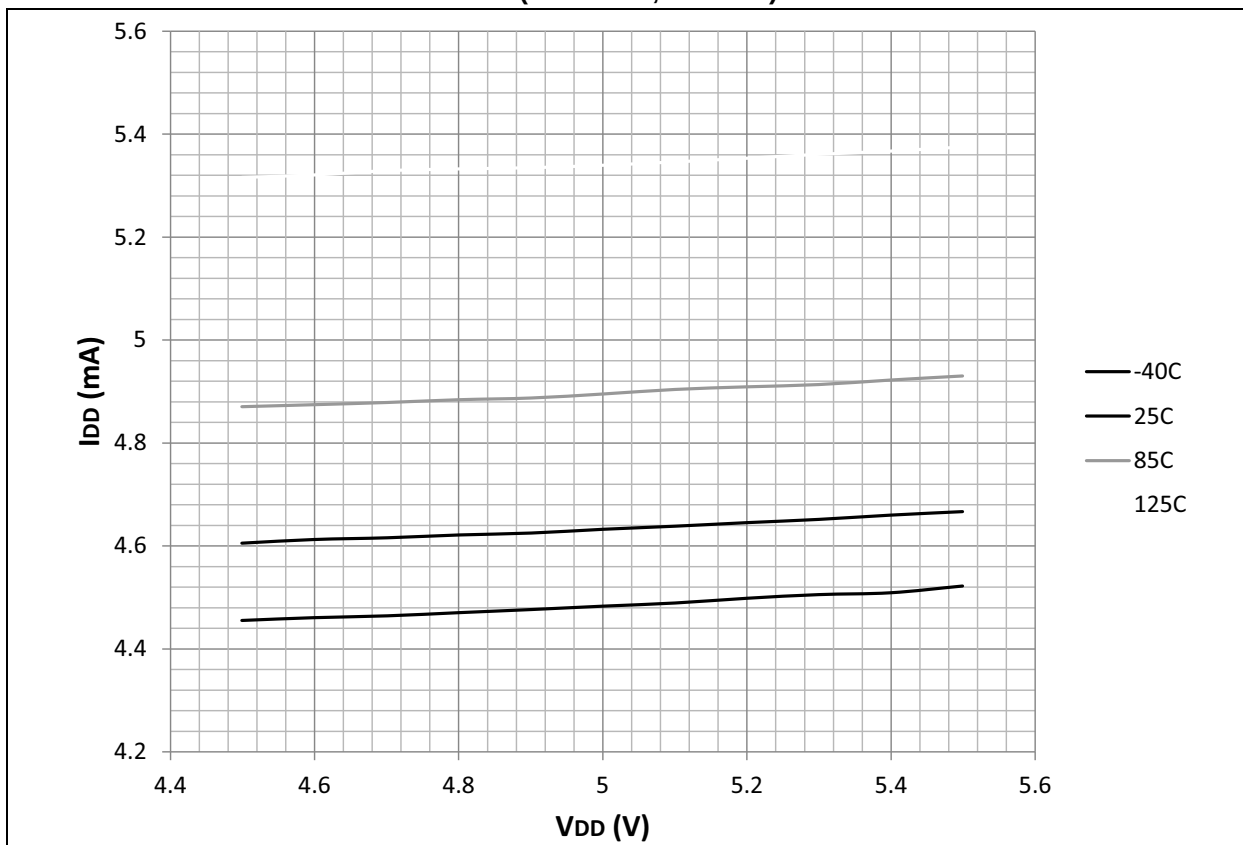
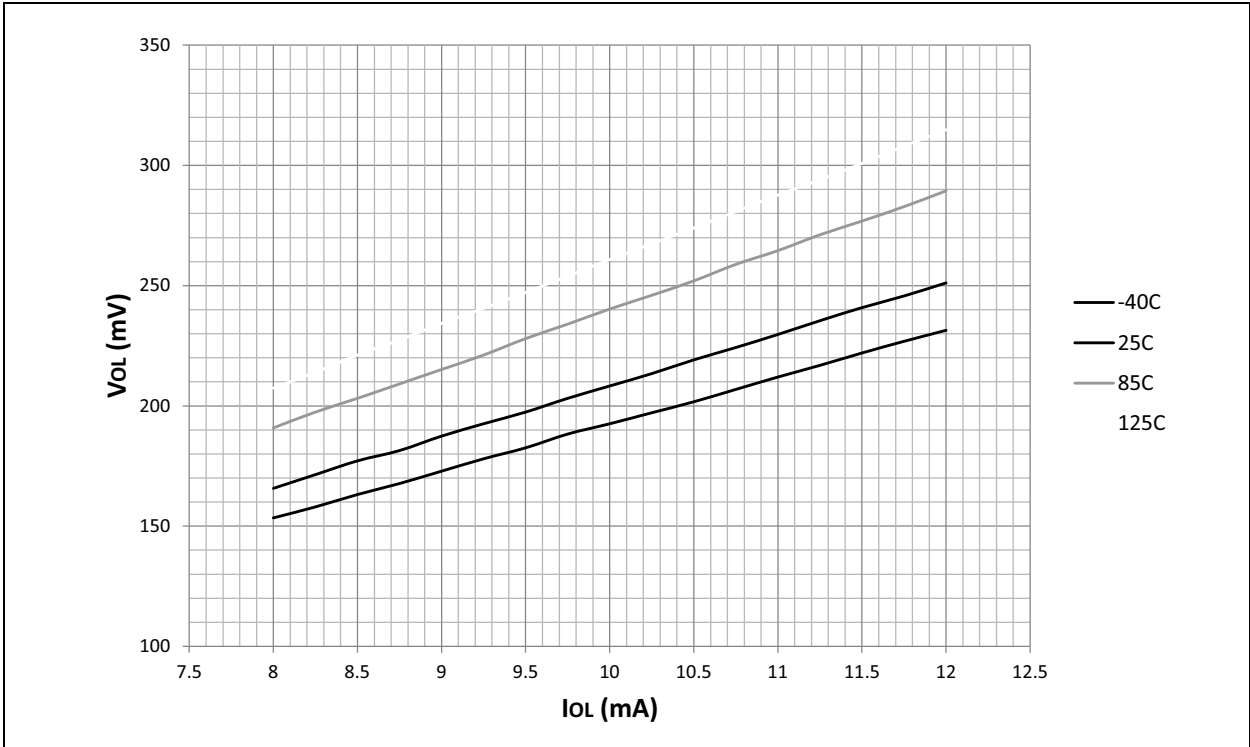
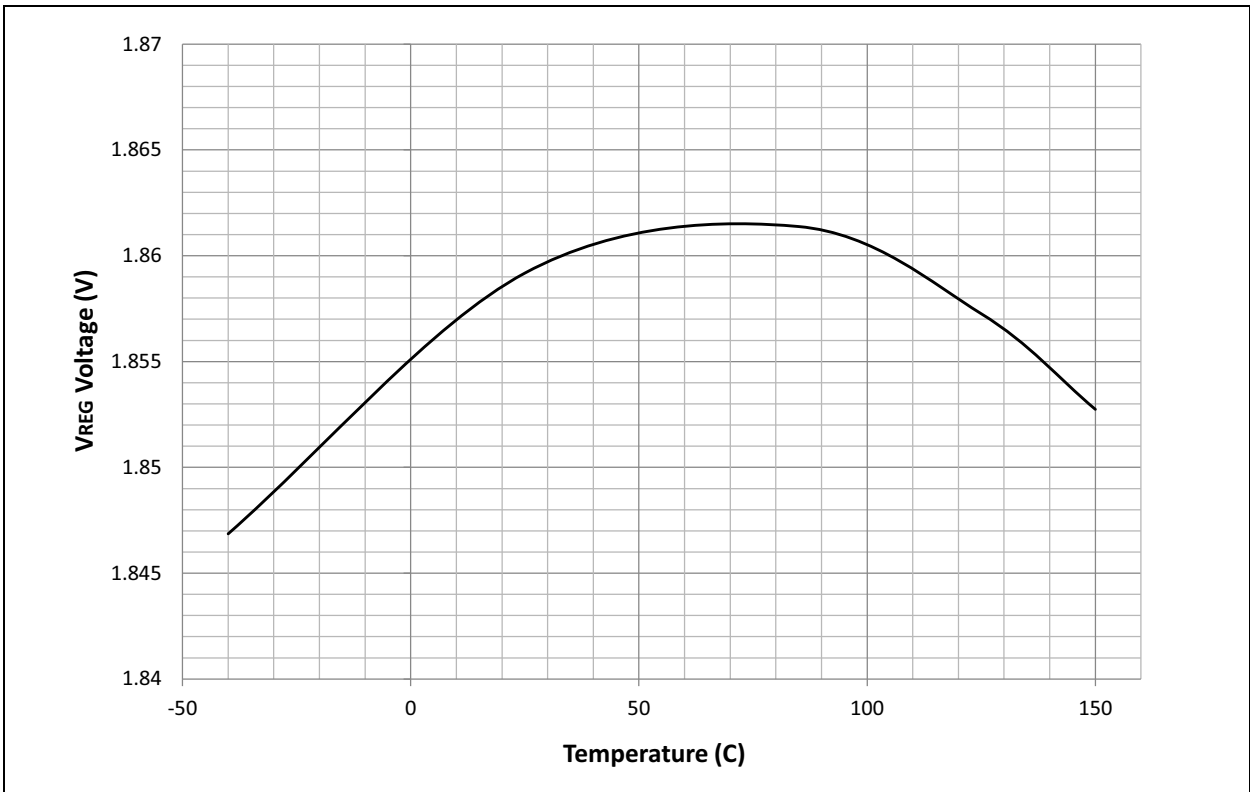


FIGURE 32-33: TYPICAL V_{OL} 4x DRIVER PINS vs. I_{OL} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



32.11 V_{REG}

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE



32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. V_{CM}

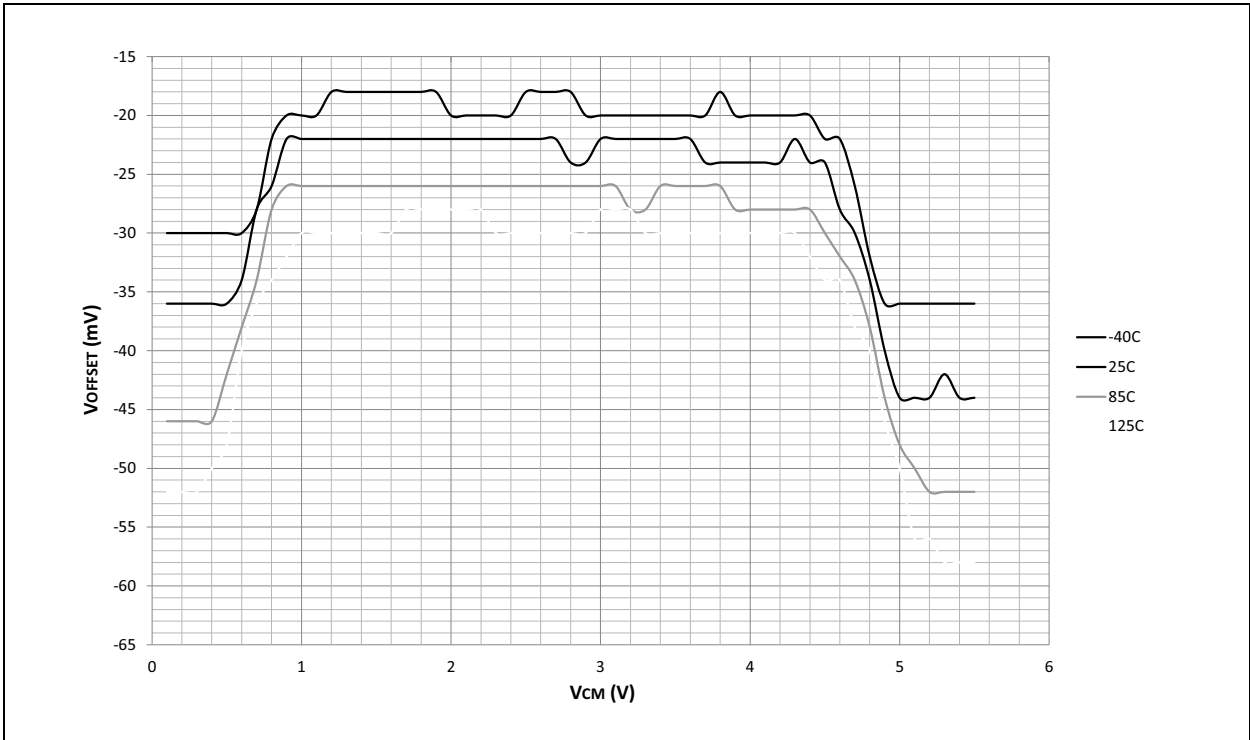
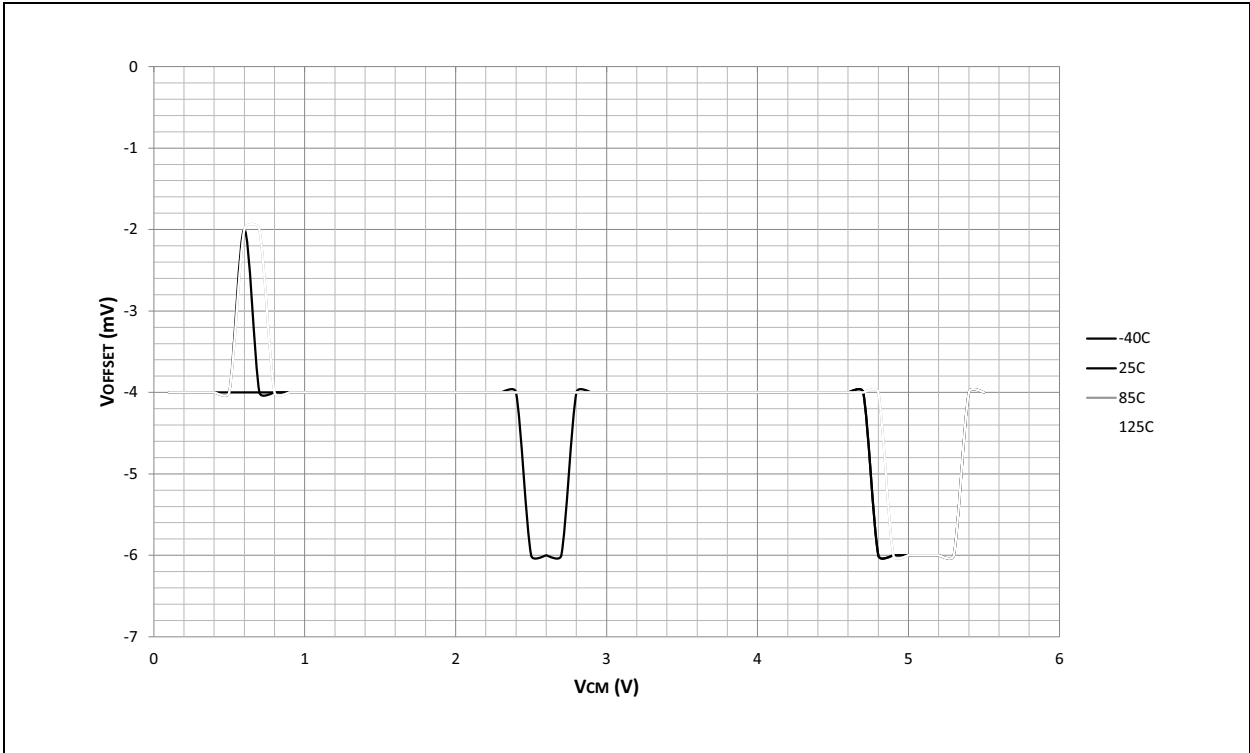


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. V_{CM} OP AMP OFFSET



dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 33-11: TYPICAL I_{DOZE} vs. V_{DD} (DOZE 1:128, 70 MIPS)

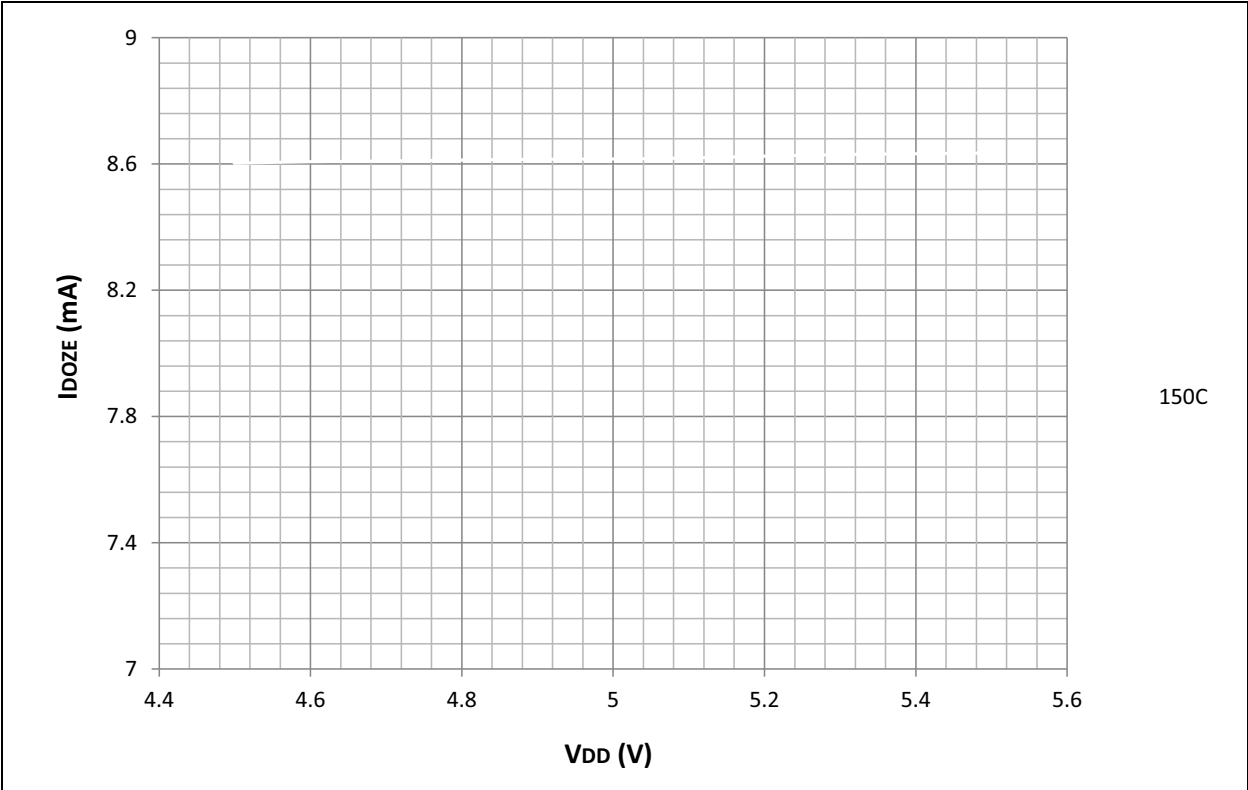
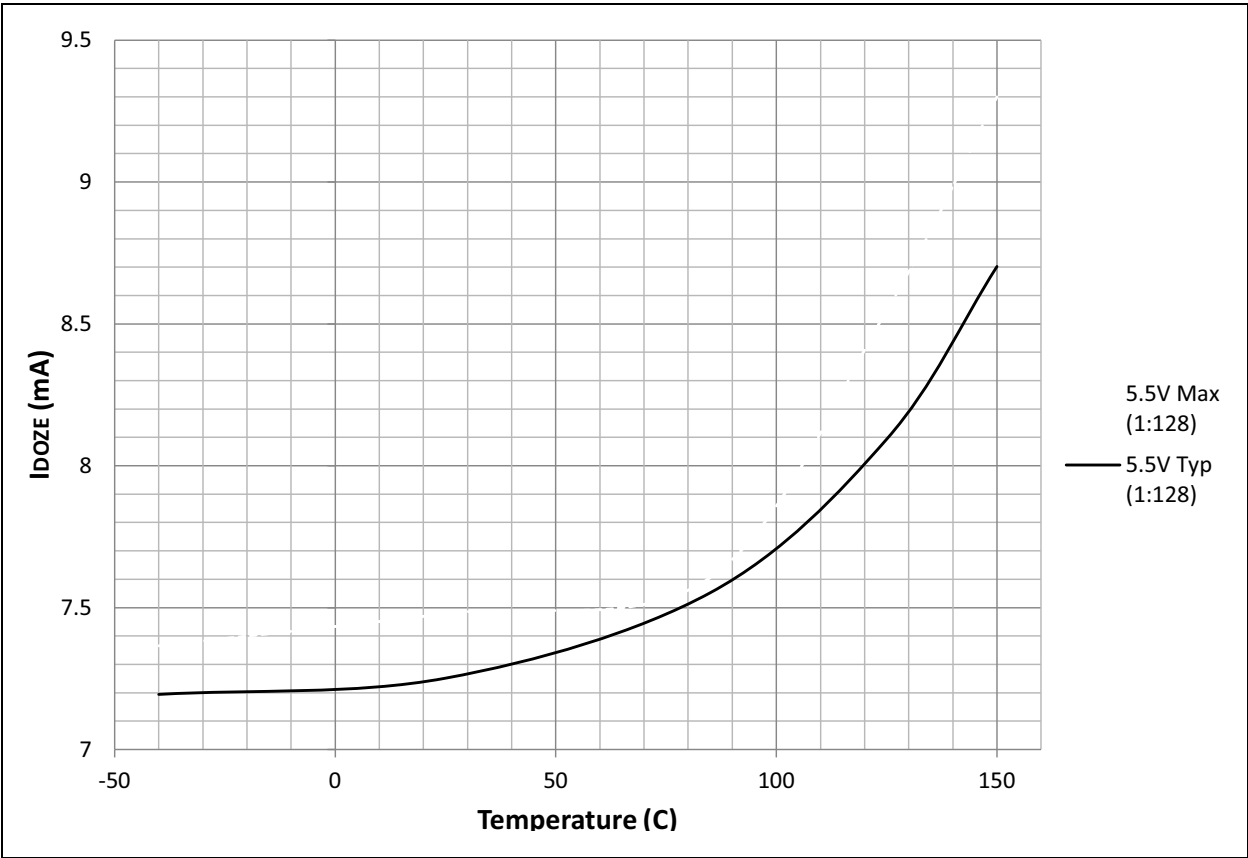


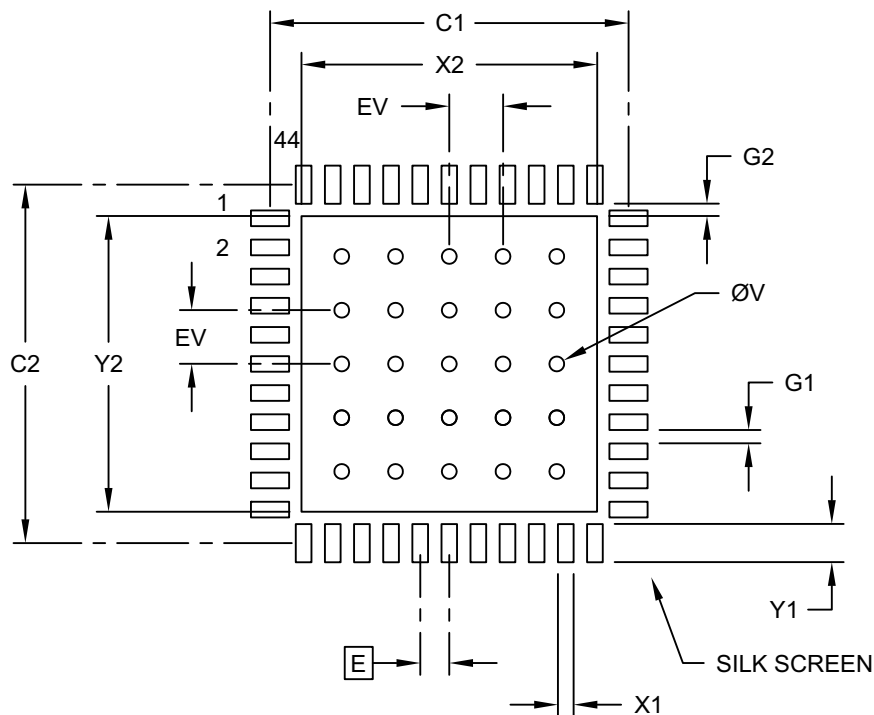
FIGURE 33-12: TYPICAL/MAXIMUM I_{DOZE} vs. TEMPERATURE (DOZE 1:128, 70 MIPS)



dsPIC33EVXXXGM00X/10X FAMILY

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

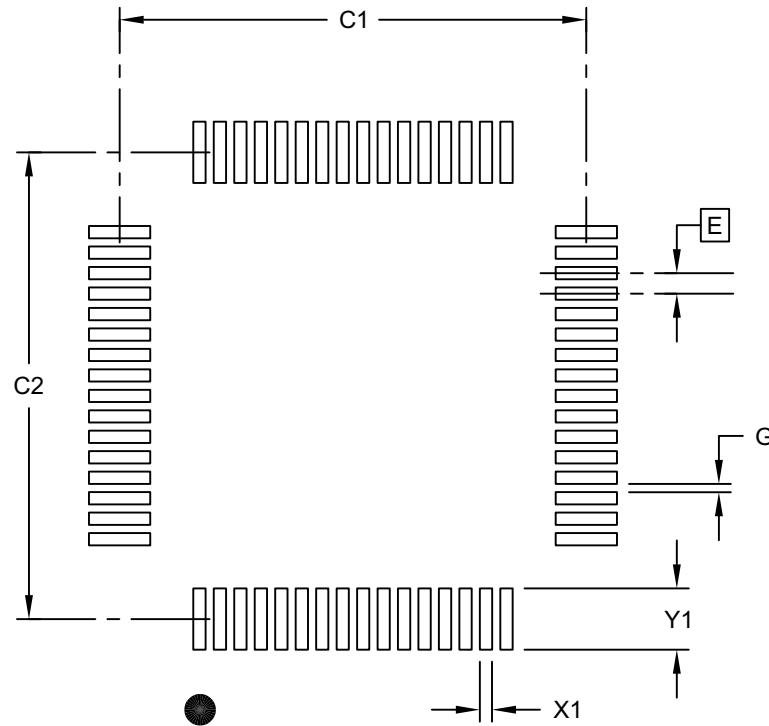
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C

dsPIC33EVXXXGM00X/10X FAMILY

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

dsPIC33EVXXXGM00X/10X FAMILY

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