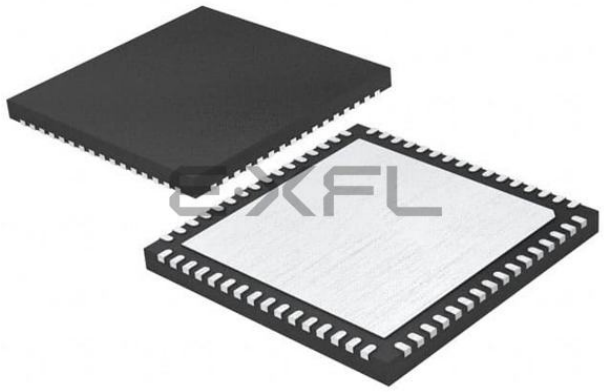
Microchip Technology - DSPIC33EV64GM006-I/MR Datasheet



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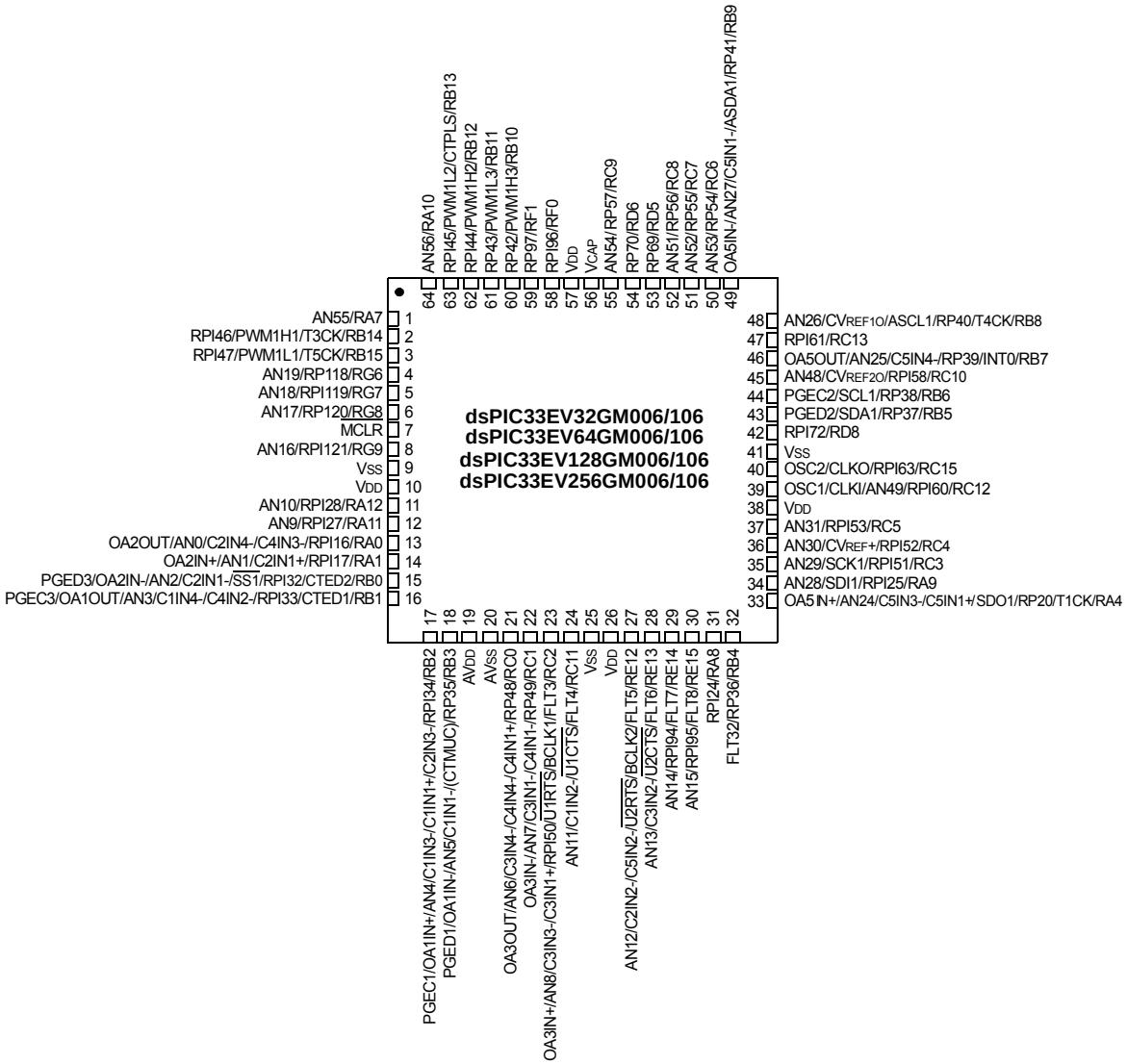
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm006-i-mr

Pin Diagrams (Continued)

64-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

TABLE 4-45: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.4.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.4.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set, {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X Data Space) and W11 (in Y Data Space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.4.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (Branch) instructions use 16-bit signed literals to specify the Branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

NOTES:

REGISTER 23-3: CTMUICON: CTMU CURRENT CONTROL REGISTER(3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1(2)	IRNG0(2)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM<5:0>:** Current Source Trim bits

011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%
•
•
•
000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%
•
•
•
100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG<1:0>:** Current Source Range Select bits(2)

11 = 100 × Base Current
10 = 10 × Base Current
01 = Base Current Level
00 = 1000 × Base Current(1)

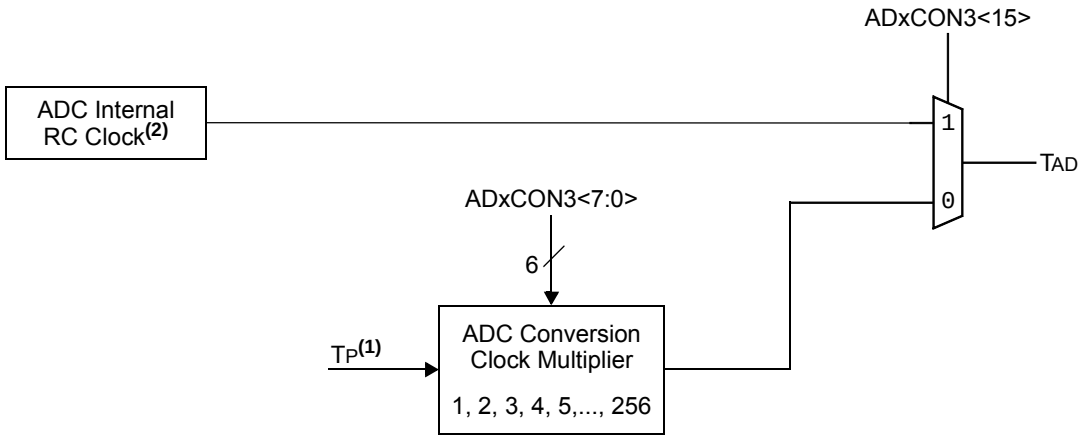
bit 7-0 **Unimplemented:** Read as '0'

Note 1: This current range is not available for use with the internal temperature measurement diode.

2: Refer to the CTMU Current Source Specifications (Table 30-53) in **Section 30.0 "Electrical Characteristics"** for the current range selection values.

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

FIGURE 24-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: TP = 1/FP.

2: Refer to the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

REGISTER 26-2: CVR2CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 2

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE(1)	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF2O Pin) bit(1)
1 = Voltage level is output on the CVREF2O pin
0 = Voltage level is disconnected from the CVREF2O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = Comparator Reference Source 2 (CVR2) provides inverting input voltage when VREFSEL (CVR1CON<10>) = 0
0 = Comparator Reference Source 1 (CVR1) provides inverting input voltage when VREFSEL (CVR1CON<10>) = 0

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR<6:0>:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

Note 1: CVROE (CVR2CON<14>) is not available on the 28-pin devices.

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS
			dsPIC33EVXXXGM00X/10X Family
I-Temp	4.5V to 5.5V(1,2)	-40°C to +85°C	70
E-Temp	4.5V to 5.5V(1,2)	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: When BOR is enabled, the device will work from 4.7V to 5.5V.

Note 1: Customer operating voltage range is specified as: 4.5V to 5.5V.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN, 9x9x0.9 mm	θJA	28.0	—	°C/W	**1**
Package Thermal Resistance, 64-Pin TQFP, 10x10x1 mm	θJA	48.3	—	°C/W	**1**
Package Thermal Resistance, 44-Pin QFN, 8x8 mm	θJA	29.0	—	°C/W	**1**
Package Thermal Resistance, 44-Pin TQFP, 10x10x1 mm	θJA	49.8	—	°C/W	**1**
Package Thermal Resistance, 28-Pin QFN-S, 6x6x0.9 mm	θJA	30.0	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SOIC, 7.50 mm	θJA	69.7	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SSOP, 5.30 mm	θJA	71.0	—	°C/W	**1**
Package Thermal Resistance, 28-Pin SPDIP, 300 mil	θJA	60.0	—	°C/W	**1**

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	4.5	—	5.5	V	
D132b	VPEW	VDD for Self-Timed Write	4.5	—	5.5	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current During Programming	—	10	—	mA	
D136a	TRW	Row Write Cycle Time	0.657	—	0.691	ms	TRW = 4965 FRC cycles, TA = +85°C (see **Note 2)**
D136b	TRW	Row Write Cycle Time	0.651	—	0.698	ms	TRW = 4965 FRC cycles, TA = +125°C (see **Note 2)**
D137a	TPE	Page Erase Time	19.44	—	20.44	ms	TPE = 146893 FRC cycles, TA = +85°C (see **Note 2)**
D137b	TPE	Page Erase Time	19.24	—	20.65	ms	TPE = 146893 FRC cycles, TA = +125°C (see **Note 2)**
D138a	TWW	Word Write Cycle Time	45.78	—	48.15	µs	TWW = 346 FRC cycles, TA = +85°C (see **Note 2)**
D138b	TWW	Word Write Cycle Time	45.33	—	48.64	µs	TWW = 346 FRC cycles, TA = +125°C (see **Note 2)**

Note 1: Data in “Typ.” column is at 5.0V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.3728 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 30-20) and the value of the FRC Oscillator Tuning register.

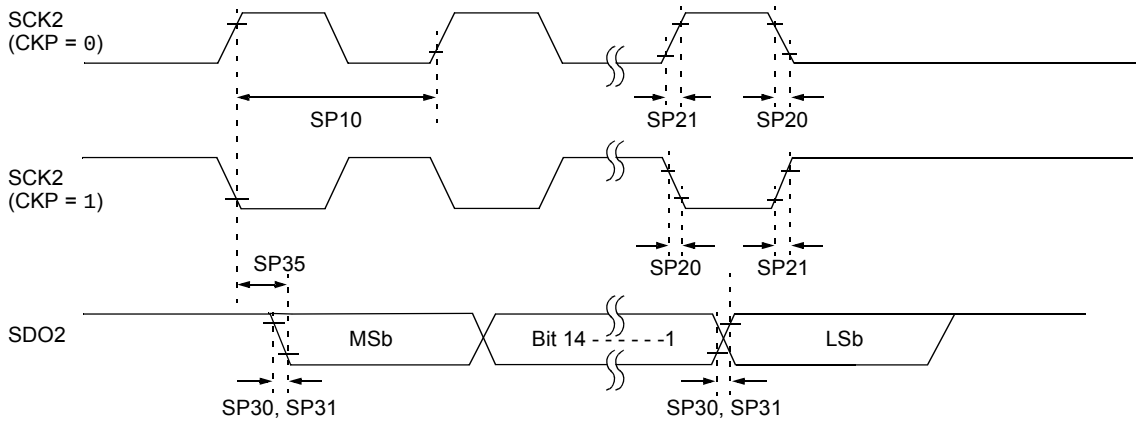
TABLE 30-14: ELECTRICAL CHARACTERISTICS: INTERNAL BAND GAP REFERENCE VOLTAGE

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DVR10	VBG	Internal Band Gap Reference Voltage	1.14	1.2	1.26	V	

TABLE 30-30: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 30-31	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-32	—	1	0,1	1
9 MHz	—	Table 30-33	—	0	0,1	1
15 MHz	—	—	Table 30-34	1	0	0
11 MHz	—	—	Table 30-35	1	1	0
15 MHz	—	—	Table 30-36	0	1	0
11 MHz	—	—	Table 30-37	0	0	0

FIGURE 30-12: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-16: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

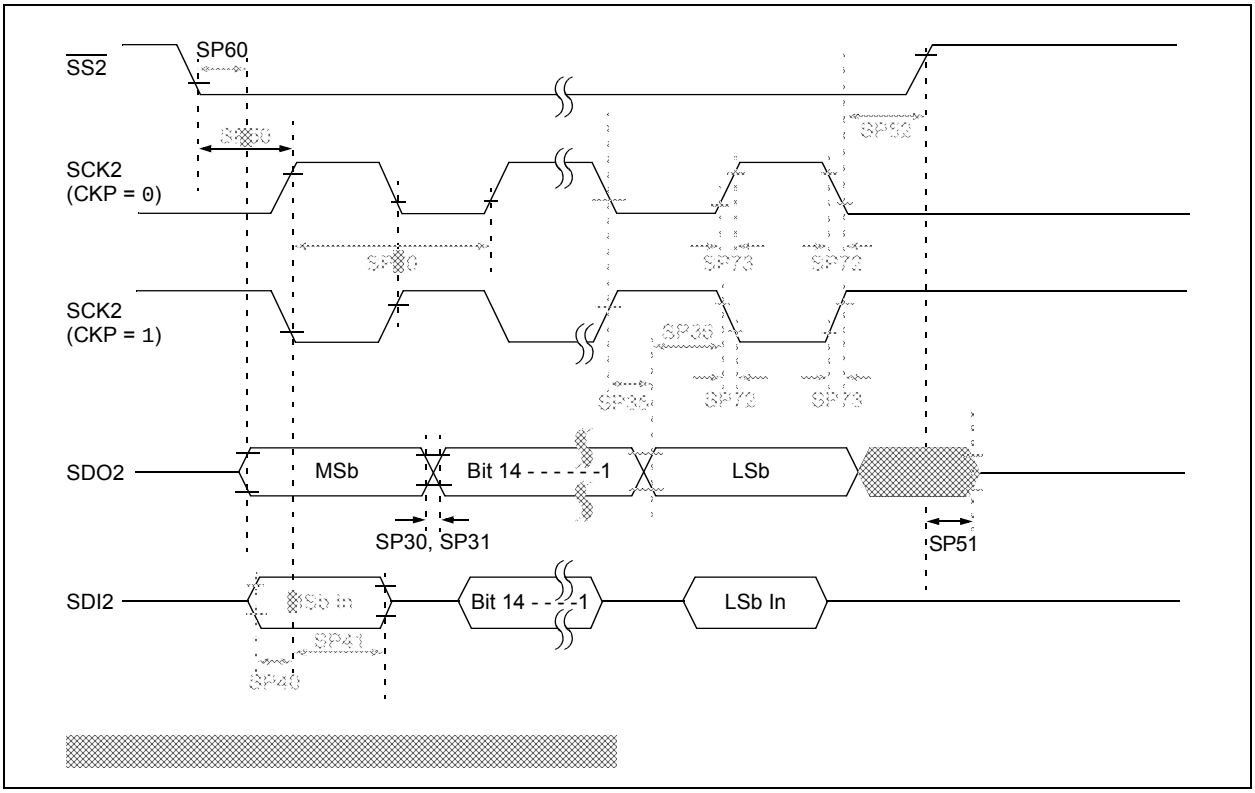


TABLE 30-47: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	**Symbol**	**Characteristic(3)**		**Min.**	**Max.**	**Units**	**Conditions**
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode(1)	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(1)	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(1)	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(1)	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode(1)	0.25		µs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode(1)	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(1)	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See **Note 2**

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

TABLE 30-54: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or VBOR	—	Lesser of: VDD + 0.3 or 5.5	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	4.5	—	5.5	V	VREFH = AVDD, VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – VBORMIN	V	See **Note 1**
AD06a			0	—	0	V	VREFH = AVDD, VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	4.5	—	5.5	V	VREF = VREFH – VREFL
AD08	IREF	Current Drain	— —	— —	10 600	μA μA	ADC off ADC on
AD09	IAD	Operating Current	— —	5 2	— —	mA mA	ADC operating in 10-bit mode (see **Note 1**) ADC operating in 12-bit mode (see **Note 1**)
Analog Input							
AD12	VINH	Input Voltage Range VINH	VINL	—	VREFH	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	Impedance to achieve maximum performance of ADC

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

33.3 IDOZE

FIGURE 33-9: TYPICAL IDOZE vs. VDD (DOZE 1:2, 70 MIPS)

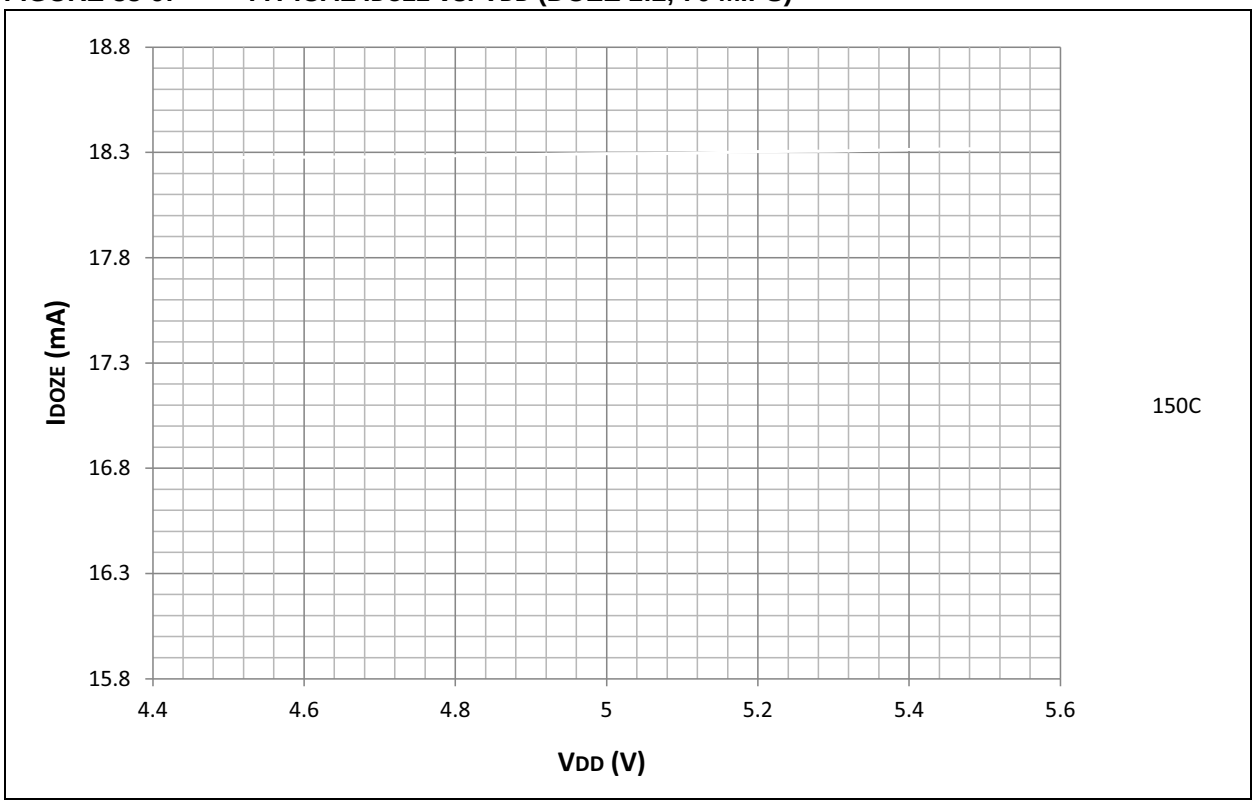
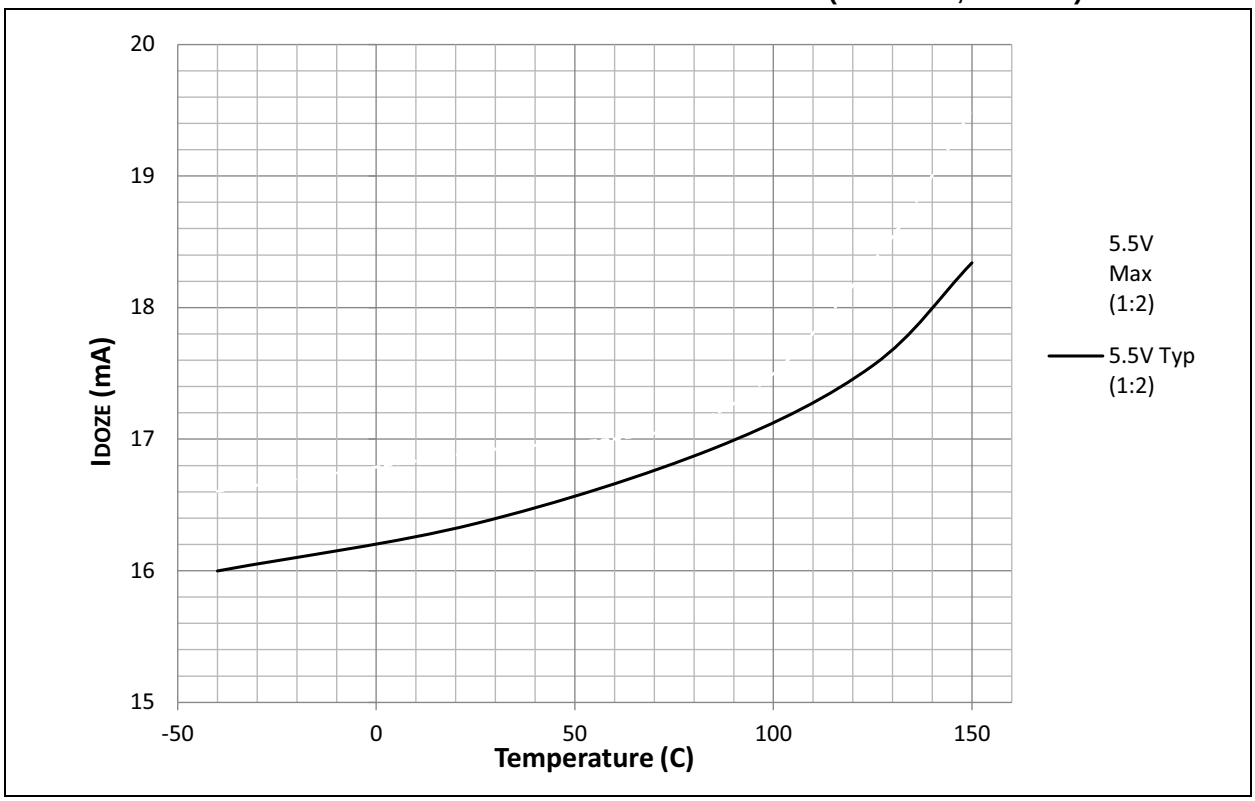


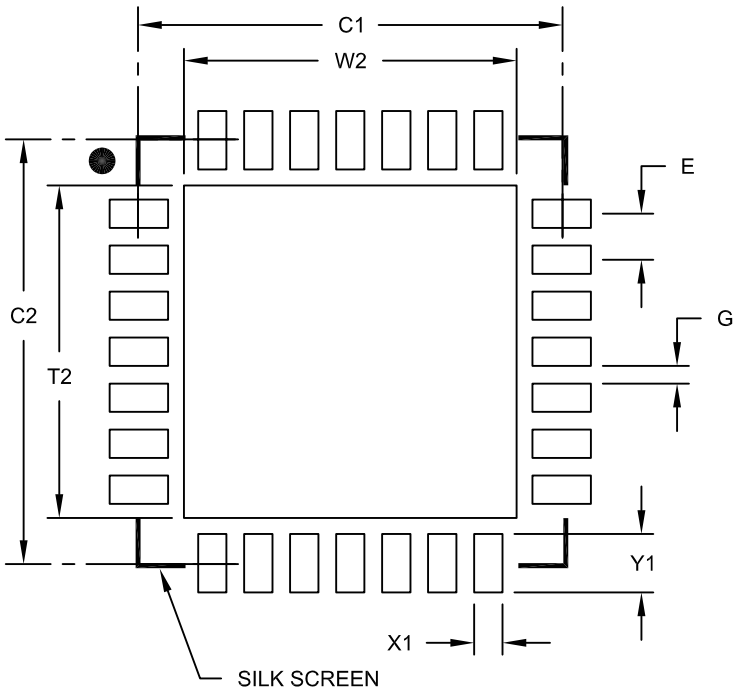
FIGURE 33-10: TYPICAL/MAXIMUM IDOZE vs. TEMPERATURE (DOZE 1:2, 70 MIPS)



NOTES:

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

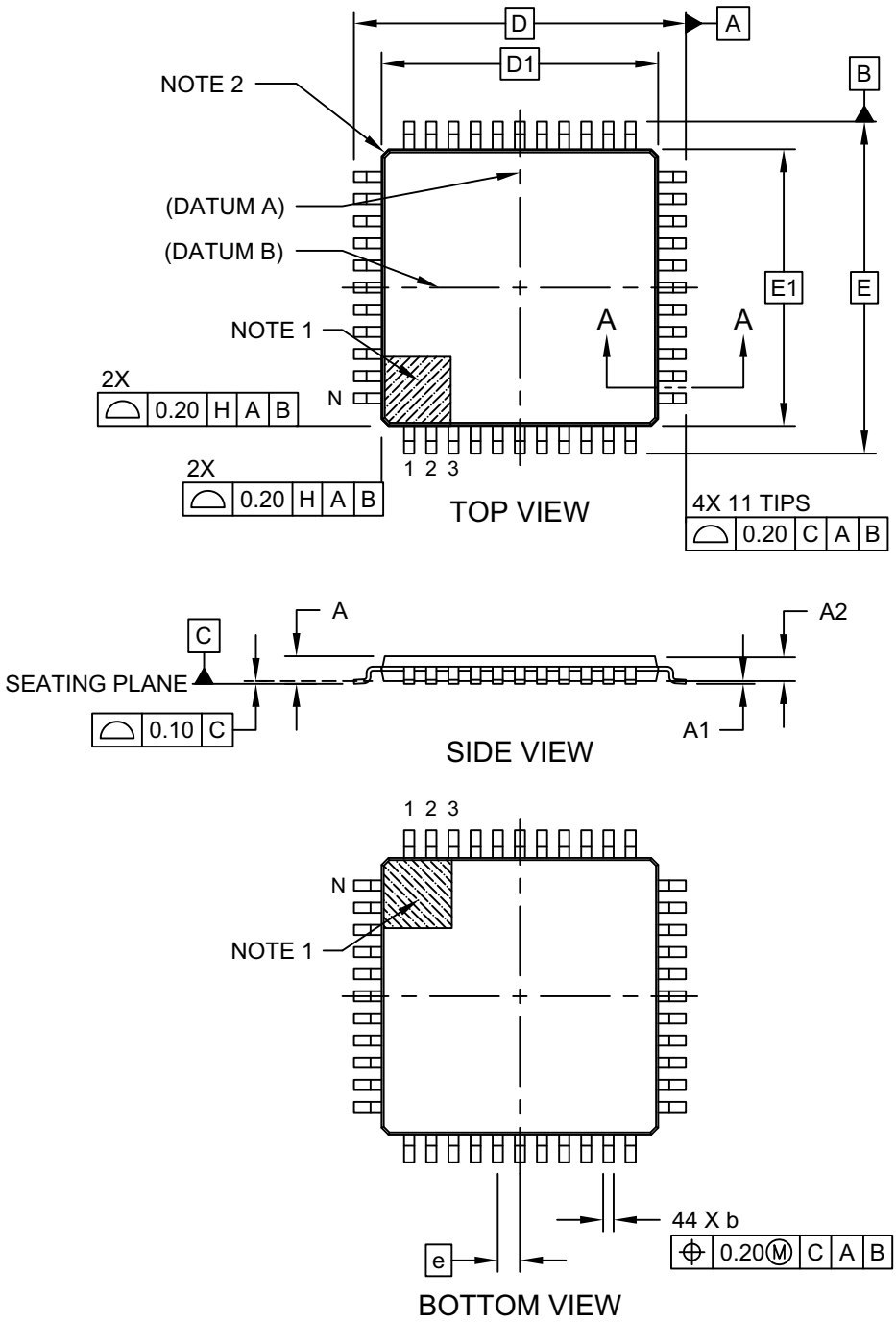
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

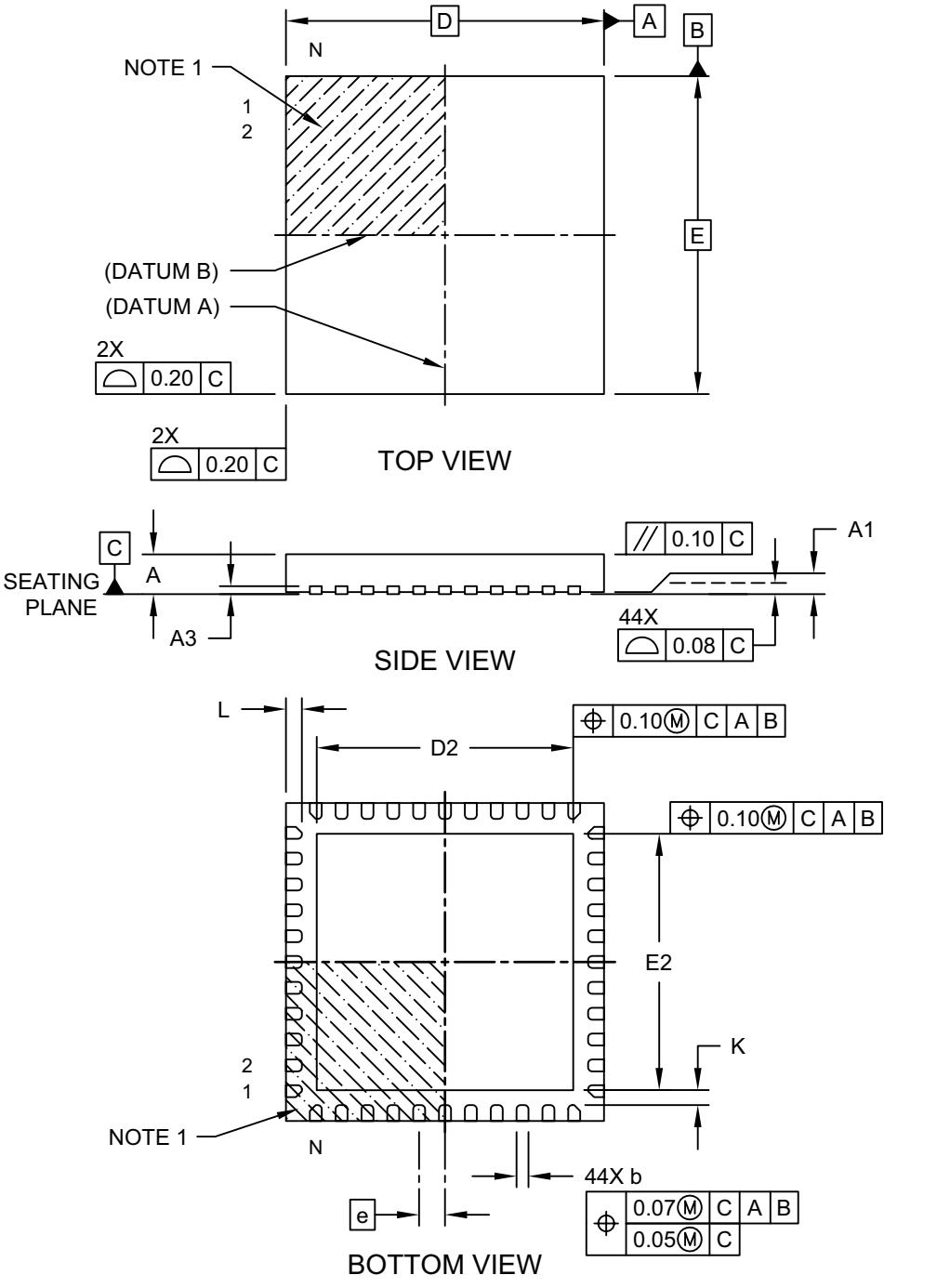
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-076C Sheet 1 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103D Sheet 1 of 2