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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	21
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 11x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm102-i-sp

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Pin Diagrams (Continued)



TADLE	4-3.					ROUGI		CAF	IUKE 4	REGIS								
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	_	_	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC1CON2	0142	_	—	—	—	—	—	_	IC32	ICTRIG	TRIGSTAT	_	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC1BUF	0144								Inp	ut Capture	1 Buffer Regi	ster						xxxx
IC1TMR	0146								Inp	ut Capture	1 Timer Regi	ster						0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0		—		ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC2CON2	014A	—	—	—	—	—	_		IC32	ICTRIG	TRIGSTAT	-	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC2BUF	014C								Inp	ut Capture	2 Buffer Regi	ster						xxxx
IC2TMR	014E								Inp	ut Capture	2 Timer Regi	ster						0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0		—		ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC3CON2	0152	—	—	—	—	—	_		IC32	ICTRIG	TRIGSTAT	-	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC3BUF	0154								Inp	ut Capture	3 Buffer Regi	ster						xxxx
IC3TMR	0156		Input Capture 3 Timer Register 00									0000						
IC4CON1	0158	_	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	_	_	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC4CON2	015A	_	—	_	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC4BUF	015C								Inp	ut Capture	4 Buffer Regi	ster						xxxx
IC4TMR	015E								Inp	ut Capture	4 Timer Regi	ster						0000

TABLE 4-3: INDUT CARTINE 1 THROUGH INDUT CARTINE A REGISTER MAD

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: **I2C1 REGISTER MAP**

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1CON1	0200	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CON2	0202	_	_	_	_	_	_	_	_	_	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	1000
I2C1STAT	0204	ACKSTAT	TRSTAT	ACKTIM	_	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	Р	S	R_W	RBF	TBF	0000
I2C1ADD	0206	—		—	_	—		I2C1 Address Register						0000				
I2C1MSK	0208	—	-	—	—	_					Ľ	2C1 Address	Mask Regi	ster				0000
I2C1BRG	020A							Baud Rate Generator Register 0							0000			
I2C1TRN	020C	_	_	_	_	_	_	— — I2C1 Transmit Register 0						OOFF				
I2C1RCV	020E		_	_		_	_	I2C1 Receive Register							0000			

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-5: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN		USIDL	IREN	RTSMD		UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0		UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—		—		—	_	_				UART1	Transmit Re	egister				xxxx
U1RXREG	0226	_	_	—	_	_	_	_				UART1	Receive Re	egister				0000
U1BRG	0228		UART1 Baud Rate Generator Prescaler Register 0000										0000					
U2MODE	0230	UARTEN	_	USIDL	IREN	RTSMD	_	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	_	_	—	_	_	_	_				UART2	Transmit Re	egister				xxxx
U2RXREG	0236	_	_	—	_	_	_	_				UART2	Receive Re	egister				0000
U2BRG	0238						L	JART2 Ba	ud Rate G	Senerator Pres	scaler Registe	r						0000

Legend: x = unknown value on Reset; --- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN		SPISIDL	_		SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242		—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—			—	FRMDLY	SPIBEN	0000
SPI1BUF	0248		SPI1 Transmit and Receive Buffer Register									0000						
SPI2STAT	0260	SPIEN	—	SPISIDL	—		SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262		—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	_	_	_	_	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register 00								0000								

Legend: - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

dsPIC33EVXXXGM00X/10X FAMILY

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



8.0 DIRECT MEMORY ACCESS (DMA)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Direct Memory Access (DMA)" (DS70348) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM. For the simplified DMA block diagram, refer to Figure 8-1.

In addition, DMA can access the entire data memory space. The data memory bus arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports 4 independent channels. Each channel can be configured for transfers to or from selected peripherals. The peripherals supported by the DMA Controller include:

- CAN
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: PERIPHERAL TO DMA CONTROLLER



x = Bit is unknown

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSADF	₹<23:16>			
bit 7							bit 0
Legend:							
R = Readable b	bit	W = Writable bit	t	U = Unimpler	nented bit. read	l as '0'	

'0' = Bit is cleared

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

bit 15-8 **Unimplemented:** Read as '0'

-n = Value at POR

bit 7-0 DSADR<23:16>: Most Recent DMA Address Accessed by DMA bits

'1' = Bit is set

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSAD)R<15:8>			
bit 15							bit 8
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
			DSA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimplen	nented bit, rea	d as '0'	
-n = Value at P	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	iown

bit 15-0 DSADR<15:0>: Most Recent DMA Address Accessed by DMA bits

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R5 ⁽¹⁾	RP120R4 ⁽¹⁾	RP120R3 ⁽¹⁾	RP120R2 ⁽¹⁾	RP120R1 ⁽¹⁾	RP120R0 ⁽¹⁾
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
-----------	----------------------------

bit 13-8	RP176R<5:0>: Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 11-3 for peripheral function numbers)
bit 7-6	Unimplemented: Read as '0'
bit 5-0	RP120R<5:0>: Peripheral Output Function is Assigned to RP120 Output Pin bits ⁽¹⁾

(see Table 11-3 for peripheral function numbers)

REGISTER 11-29: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0
bit 7							bit 0

Legend:				
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-14 Unimplemented: Read as '0'

- bit 13-8 **RP178R<5:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 11-3 for peripheral function numbers)
- bit 7-6 Unimplemented: Read as '0'
- bit 5-0 **RP177R<5:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: RP120R<5:0> is present in dsPIC33EVXXXGM006/106 devices only.

REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

- bit 2-0 OCM<2:0>: Output Compare x Mode Select bits
 - 111 = Center-Aligned PWM mode: Output sets high when OCxTMR = OCxR and sets low when OCxTMR = OCxRS⁽¹⁾
 - 110 = Edge-Aligned PWM mode: Output sets high when OCxTMR = 0 and sets low when OCxTMR = $OCxR^{(1)}$
 - 101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
 - 100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
 - 011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
 - 010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
 - 001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
 - 000 = Output compare channel is disabled
- Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Serial Peripheral Interface (SPI)" (DS70005185) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with the Motorola[®] SPI and SIOP interfaces.

The dsPIC33EVXXXGM00X/10X device family offers two SPI modules on a single device, SPI1 and SPI2, that are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of this module, but results in a lower maximum speed. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of the following four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- · SCKx: Shift Clock Input or Output
- SSx/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

Note: All of the 4 pins of the SPIx serial interface must be configured as digital in the ANSELx registers.

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, SSx is not used. In 2-pin mode, neither SDOx nor SSx is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0			
			RXOVF	-<15:8>						
bit 15							bit 8			
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0			
RXOVF<7:0>										
bit 7							bit 0			
Legend:		C = Writable I	oit, but only '0'	can be writter	n to clear the bit					

Logona.	o windbio bit, but only o	ball be written to orear the bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
			RXOV	F<31:24>			
bit 15							bit 8
R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
			RXOV	F<23:16>			
bit 7							bit 0
Legend:		C = Writable b	bit, but only '()' can be writter	n to clear the b	bit	
R = Readable	bit	W = Writable	bit	U = Unimpler	nented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits

1 = Module attempted to write to a full buffer (set by module)

0 = No overflow condition (cleared by user software)

REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

- **Note 1:** AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.
 - 2: If the op amp is selected (OPAEN bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.
 - 3: See the "Pin Diagrams" section for the available analog channels for each device.

TABLE 30-6:	DC CHARACTERISTICS: OPERATING CURRENT (IDD)	
-------------	---	--

DC CHARACT	ERISTICS		$\begin{array}{l} \mbox{Standard Operating Conditions: 4.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Тур. ⁽²⁾	Max.	Units	Units Conditions				
Operating Cur	rent (IDD) ⁽¹⁾							
DC20d	4.5	5.5	mA	-40°C				
DC20a	4.65	5.6	mA	+25°C	5.01/			
DC20b	4.85	6.0	mA	+85°C	5.00			
DC20c	5.6	7.2	mA	+125°C				
DC22d	8.6	10.6	mA	-40°C				
DC22a	8.8	10.8	mA	+25°C	5.0\/			
DC22b	9.1	11.1	mA	+85°C	5.00	20 MIF 3		
DC22c	9.8	12.6	mA	+125°C				
DC23d	16.8	18.5	mA	-40°C				
DC23a	17.2	19.0	mA	+25°C	5.0\/			
DC23b	17.55	19.2	mA	+85°C	5.0 V	40 MIF 3		
DC23c	18.3	21.0	mA	+125°C				
DC24d	25.15	28.0	mA	-40°C				
DC24a	25.5	28.0	mA	+25°C	5.0\/			
DC24b	25.5	28.0	mA	+85°C	5.0 v			
DC24c	25.55	28.5	mA	+125°C				
DC25d	29.0	31.0	mA	-40°C				
DC25a	28.5	31.0	mA	+25°C	5.0V	70 MIPS		
DC25b	28.3	31.0	mA	+85°C				

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

 Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)

- · CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- MCLR = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing
 - while(1)

```
{
NOP();
```

```
NOP ( )
```

2: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions (see Note 1): 4.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param No.	Symbol	Symbol Characteristic		Тур.	Max.	Units	Conditions	
		ADC A	Accuracy	(10-Bit	Mode)			
AD20b	Nr	Resolution	1() data bi	ts	bits		
AD21b	INL	Integral Nonlinearity	-1.5		+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V	
AD22b	DNL	Differential Nonlinearity	≥ 1	_	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V	
AD23b	Gerr	Gain Error	1	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V	
AD24b	EOFF	Offset Error	1	2	4	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V	
AD25b	—	Monotonicity ⁽²⁾	—		-		Guaranteed	
		Dynamic I	Performa	nce (10-	Bit Mod	e)		
AD30b	THD	Total Harmonic Distortion	_	_	-64	dB		
AD31b	SINAD	Signal to Noise and Distortion	57	58.5		dB		
AD32b	SFDR	Spurious Free Dynamic Range	72			dB		
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz		
AD34b	ENOB	Effective Number of Bits	9.16	9.4		bits		

TABLE 30-56: ADC MODULE SPECIFICATIONS (10-BIT MODE)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: The conversion result never decreases with an increase in the input voltage.

TABLE 31-17. OF ANN /CONN ANATON & SECONDATIONS	TABLE 31-17:	OP AMP/COMPARATOR x SPECIFICATIONS
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DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$							
Param No.	Symbol	Characteristic	Min.	Тур. ⁽¹⁾	Max.	Units	Conditions			
Comparator DC Characteristics										
HCM30	VOFFSET	Comparator Offset Voltage	-80	±60	80	mV				
HCM31	VHYST	Input Hysteresis Voltage	—	30	_	mV				
HCM34	VICM	Input Common-Mode Voltage	AVss	—	AVdd	V				
Op Amp DC Characteristics ⁽²⁾										
HCM40	VCMR	Common-Mode Input Voltage Range	AVss	_	AVDD	V				
HCM42	VOFFSET	Op Amp Offset Voltage	-50	±6	50	mV				

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

TABLE 31-18: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V(unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +150^{\circ}C$							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions			
ADC Accuracy (12-Bit Mode)										
HAD20a	Nr	Resolution	12 data bits		bits					
HAD21a	INL	Integral Nonlinearity	-2		+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V			
HAD22a	DNL	Differential Nonlinearity	> -1		< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V			
HAD23a	Gerr	Gain Error	-10	4	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V			
HAD24a	EOFF	Offset Error	-10	1.75	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V			

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

dsPIC33EVXXXGM00X/10X FAMILY

32.2 IIDLE

FIGURE 32-7: TYPICAL/MAXIMUM lidle vs. Fosc (EC MODE 10 MHz TO 70 MHz, 5.5V MAX)





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FIGURE 33-19: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V VDD)

33.7 Leakage Current





33.8 Pull-up/Pull-Down Current











33.15 CTMU Current V/S Temperature

33.16 CTMU Temperature Forward Diode (V)



44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	Limits	MIN	NOM	MAX		
Number of Leads	Ν	44				
Lead Pitch	е	0.80 BSC				
Overall Height	Α	-	-	1.20		
Standoff	A1	0.05 -		0.15		
Molded Package Thickness	A2	0.95	1.00	1.05		
Overall Width	E	12.00 BSC				
Molded Package Width	E1	10.00 BSC				
Overall Length	D	12.00 BSC				
Molded Package Length	D1	10.00 BSC				
Lead Width	b	0.30	0.37	0.45		
Lead Thickness	С	0.09	-	0.20		
Lead Length	L	0.45	0.60	0.75		
Footprint	L1	1.00 REF				
Foot Angle	θ	0°	3.5°	7°		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Exact shape of each corner is optional.

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

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