

Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XEI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm104-e-pt

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

#### TABLE 4-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM002/102 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	_	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0		_	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	_	_	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	_	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	_	_	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	_	_	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	_	_	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	_	_	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	_	_	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	_	_	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR10	0684	_	_			RP176	R<5:0>			_	_	_	_	_	_	_	_	0000
RPOR11	0686	_	_	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	_	_	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	_	_	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	_	_	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	_	—	—	—		_		_	_	_			RP181	R<5:0>			0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

#### TABLE 4-15: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM004/104 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	_	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	_	_	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	_	_	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	-	_	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	_	_	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	-	_	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676		—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	_	_	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	_	_	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	-	_	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR5	067A	_	_	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	-	_	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0	0000
RPOR6	067C	_	_	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	-	_	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0	0000
RPOR7	067E	_	_	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	-	_	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0	0000
RPOR10	0684	_	_			RP176	R<5:0>			-	_	_	_	_	_	_	_	0000
RPOR11	0686	_	_	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	_	_	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	_	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	_	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	_	_	_	_	_	_	_	_	_	_					0000		

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-22: PMD REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD <sup>(1)</sup>	AD1MD	0000
PMD2	0762	_	_	_	_	IC4MD	IC3MD	IC2MD	IC1MD	_	_	_	_	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	_	_	_	_	_	CMPMD	_	_	_	_	_	_	_	_	_	_	0000
PMD4	0766	_	_	_	_	_	_	_	_	_	_		_	REFOMD	CTMUMD	_	_	0000
PMD6	076A	_	_	_	_	_	PWM3MD	PWM2MD	PWM1MD	_	_	_	_	_	_	_	_	0000
PMD7	076C	_	_	_	_	_	_	_	_	_	_	_	DMA0MD	_	_	_	_	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					
PMD8	076E	_	_	_	SENT2MD	SENT1MD	_	_	DMTMD	_	_	_	_		_	_	_	0000

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

## 5.0 FLASH PROGRAM MEMORY

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/ 10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Flash Programming" (DS70609) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

The Flash memory can be programmed in the following three ways:

- In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows for a dsPIC33EVXXXGM00X/10X family device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (PGECx/PGEDx) lines, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed

devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

Enhanced ICSP uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, refer to the specific device programming specification.

RTSP is accomplished using the TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data as a double program memory word, a row of 64 instructions (192 bytes) and erase program memory in blocks of 512 instruction words (1536 bytes) at a time.

#### 5.1 Table Instructions and Flash Programming

The Flash memory read and the double-word programming operations make use of the TBLRD and TBLWT instructions, respectively. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of the program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of the program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

#### FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



© 2013-2016 Microchip Technology Inc.

## 7.0 INTERRUPT CONTROLLER

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Interrupts" (DS70000600) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EVXXXGM00X/10X CPU. The Interrupt Vector Table (IVT) provides 246 interrupt sources (unused sources are reserved for future use) that can be programmed with different priority levels.

The interrupt controller has the following features:

- · Interrupt Vector Table with up to 246 Vectors
- Alternate Interrupt Vector Table (AIVT)
- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- · Fixed Interrupt Entry and Return Latencies
- Software can Generate any Peripheral Interrupt
- Alternate Interrupt Vector Table (AIVT) is available if Boot Security is Enabled and AIVTEN = 1

### 7.1 Interrupt Vector Table

The dsPIC33EVXXXGM00X/10X family IVT, shown in Figure 7-2, resides in program memory, starting at location, 00004h. The IVT contains seven nonmaskable trap vectors and up to 187 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

## 7.2 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-1, is available if the Boot Segment (BS) is defined, the AIVTEN bit is set in the INTCON2 register and if the AIVTDIS Configuration bit is set to '1'. The AIVT begins at the start of the last page of the Boot Segment.

Input Name <sup>(1)</sup>	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<7:0>
External Interrupt 2	INT2	RPINR1	INT2R<7:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<7:0>
Input Capture 1	IC1	RPINR7	IC1R<7:0>
Input Capture 2	IC2	RPINR7	IC2R<7:0>
Input Capture 3	IC3	RPINR8	IC3R<7:0>
Input Capture 4	IC4	RPINR8	IC4R<7:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<7:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<7:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<7:0>
UART1 Receive	U1RX	RPINR18	U1RXR<7:0>
UART2 Receive	U2RX	RPINR19	U2RXR<7:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<7:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<7:0>
SPI2 Slave Select	SS2	RPINR23	SS2R<7:0>
CAN1 Receive	C1RX	RPINR26	C1RXR<7:0>
PWM Sync Input 1	SYNCI1	RPINR37	SYNCI1R<7:0>
PWM Dead-Time Compensation 1	DTCMP1	RPINR38	DTCMP1R<7:0>
PWM Dead-Time Compensation 2	DTCMP2	RPINR39	DTCMP2R<7:0>
PWM Dead-Time Compensation 3	DTCMP3	RPINR39	DTCMP3R<7:0>
SENT1 Input	SENT1R	RPINR44	SENT1R<7:0>
SENT2 Input	SENT2R	RPINR45	SENT2R<7:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

## 14.0 DEADMAN TIMER (DMT)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Deadman Timer (DMT)" (DS70005155) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical, and safetycritical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 14-1 shows a block diagram of the Deadman Timer module.



#### FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM

#### R/W-0 R/W-0 R/W-0 R/W-0 U-0 U-0 U-0 R/W-0 **FLTMD FLTOUT FLTTRIEN** OCINV \_\_\_\_ OC32 \_\_\_\_ \_\_\_\_ bit 15 bit 8 R/W-0 R/W-0, HS R/W-0 R/W-0 R/W-1 R/W-1 R/W-0 R/W-0 OCTRIG OCTRIS SYNCSEL4 SYNCSEL3 SYNCSEL2 TRIGSTAT SYNCSEL1 SYNCSEL0 bit 7 bit 0 Legend: HS = Hardware Settable bit R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown bit 15 FLTMD: Fault Mode Select bit 1 = Fault mode is maintained until the Fault source is removed; the OCFLTA bit is cleared in software and a new PWM period starts 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts bit 14 FLTOUT: Fault Out bit 1 = PWM output is driven high on a Fault 0 = PWM output is driven low on a Fault bit 13 FLTTRIEN: Fault Output State Select bit 1 = OCx pin is tri-stated on a Fault condition 0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition bit 12 **OCINV:** Output Compare x Invert bit 1 = OCx output is inverted 0 = OCx output is not inverted bit 11-9 Unimplemented: Read as '0' bit 8 OC32: Cascade Two OCx Modules Enable bit (32-bit operation) 1 = Cascade module operation is enabled 0 = Cascade module operation is disabled bit 7 OCTRIG: Output Compare x Trigger/Sync Select bit 1 = Triggers OCx from the source designated by the SYNCSELx bits 0 = Synchronizes OCx with the source designated by the SYNCSELx bits bit 6 TRIGSTAT: Timer Trigger Status bit 1 = Timer source has been triggered and is running 0 = Timer source has not been triggered and is being held clear bit 5 OCTRIS: Output Compare x Output Pin Direction Select bit 1 = Output Compare x is tri-stated 0 = Output Compare x module drives the OCx pin

#### REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

**Note 1:** Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

#### REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4	SYNCSRC<2:0>: Synchronous Source Selection bits <sup>(1)</sup>
	111 = Reserved
	•
	•
	•
	100 = Reserved
	011 = Reserved
	010 = Reserved
	001 = Reserved
	000 = SYNCI1 input from PPS
bit 3-0	SEVTPS<3:0>: Special Event Trigger Output Postscaler Select bits <sup>(1)</sup>
	1111 = 1:16 postscaler generates a Special Event Trigger on every sixteenth compare match event
	•
	•
	•
	0001 = 1:2 postscaler generates a Special Event Trigger on every second compare match event
	0000 = 1:1 postscaler generates a Special Event Trigger on every compare match event

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

#### REGISTER 17-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	_	_	_	_	—	—
						bit 8
U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	_	_	_	F	PCLKDIV<2:0>(1	)
						bit 0
	U-0 —	U-0 U-0 — — —	U-0 U-0 U-0 — — — —	U-0 U-0 U-0 U-0 — — — — —	U-0 U-0 U-0 U-0 R/W-0 — — — — — —	U-0 U-0 U-0 U-0 R/W-0 R/W-0 PCLKDIV<2:0>(1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 Unimplemented: Read as '0'

bit 2-0 PCLKDIV<2:0>: PWMx Input Clock Prescaler (Divider) Select bits<sup>(1)</sup>

- 111 = Reserved
- 110 = Divide-by-64
- 101 = Divide-by-32
- 100 = Divide-by-16
- 011 = Divide-by-8
- 010 = Divide-by-4
- 001 = Divide-by-2

000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

## 19.0 INTER-INTEGRATED CIRCUIT (I<sup>2</sup>C)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Inter-Integrated Circuit™ (I<sup>2</sup>C<sup>TM</sup>)" (DS70000195) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains one Inter-Integrated Circuit (I<sup>2</sup>C) module, I2C1.

The  $l^2C$  module provides complete hardware support for both Slave and Multi-Master modes of the  $l^2C$  serial communication standard, with a 16-bit interface.

The I<sup>2</sup>C module has the following 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I<sup>2</sup>C module offers the following key features:

- I<sup>2</sup>C Interface Supporting Both Master and Slave modes of Operation
- I<sup>2</sup>C Slave mode Supports 7 and 10-Bit Addressing
- I<sup>2</sup>C Master mode Supports 7 and 10-Bit Addressing
- I<sup>2</sup>C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I<sup>2</sup>C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I<sup>2</sup>C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- · Support for Address Bit Masking up to Lower 7 Bits
- I<sup>2</sup>C Slave Enhancements:
  - SDAx hold time selection of SMBus (300 ns or 150 ns)
  - Start/Stop bit interrupt enables

Figure 19-1 shows a block diagram of the I<sup>2</sup>C module.

## 19.1 I<sup>2</sup>C Baud Rate Generator

The Baud Rate Generator (BRG) used for I<sup>2</sup>C mode operation is used to set the SCL clock frequency for 100 kHz, 400 kHz and 1 MHz. The BRG reload value is contained in the I2CxBRG register. The BRG will automatically begin counting on a write to the I2CxTRN register.

Equation 19-1 and Equation 19-2 provide the BRG reload formula and FSCL frequency, respectively.

#### EQUATION 19-1: BRG FORMULA

$$I2CxBRG = \left( \left( \frac{1}{FSCL} - Delay \right) \times \frac{FCY}{2} \right) - 2$$

Where:

Delay varies from 110 ns to 130 ns.

#### EQUATION 19-2: FSCL FREQUENCY

FSCL = FCY/((I2CxBRG + 2) \* 2)

## 20.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)

- Note 1: This data sheet summarizes the features of this group of dsPIC33EVXXXGM00X/ 10X family devices. It is not intended to be a comprehensive reference source. For more information on Single-Edge Nibble Transmission, refer to "Single-Edge Nibble Transmission (SENT) Module" (DS70005145) in the "dsPIC33/ PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

## 20.1 Module Introduction

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, "SENT – Single-Edge Nibble Transmission for Automotive Applications". The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- · Selectable Transmit or Receive mode
- Synchronous or Asynchronous Transmit modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive mode
- Optional Hardware Calculation of CRC in Transmit mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive from 3 to 6 Nibbles
- Automatic Detection of Framing Errors

SENT protocol timing is based on a predetermined time unit, TTICK. Both the transmitter and receiver must be preconfigured for TTICK, which can vary from 3 to 90  $\mu$ s. A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in TTICK. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are 4 bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 20-1 shows a block diagram of the SENTx module.

Figure 20-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

## 22.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EVXXXGM10X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

### 22.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments. The dsPIC33EVXXXGM10X devices contain one CAN module.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details. The CAN module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0 to 8-Byte Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to Eight Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet<sup>™</sup> Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback Mode Supports Self-Test Operation
- Signaling through Interrupt Capabilities for All CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle Modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors, and then matched against filters to see if it should be received and stored in one of the Receive registers.

Figure 22-1 shows a block diagram of the CANx module.

## 25.0 OP AMP/COMPARATOR MODULE

- Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "**Op Amp/Comparator**" (DS70000357) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family devices contain up to five comparators that can be configured in various ways. CMP1, CMP2, CMP3 and CMP5 also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

The following options allow users to:

- Select the Edge for Trigger and Interrupt Generation
- Configure the Comparator Voltage Reference
- Configure Output Blanking and Masking
- Configure as a Comparator or Op Amp (CMP1, CMP2, CMP3 and CMP5 only)

Note: Not all op amp/comparator input/output connections are available on all devices. See the "Pin Diagrams" section for available connections.



#### FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM

DC CHA	RACTER	ISTICS	Standa (unless Operation	rd Opera otherwing tempe	ating Co ise state erature	anditions: 4.5V to 5.5V ad) $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended				
Param No.	Symbol	Characteristic Min. Typ. <sup>(1)</sup> Max. Uni		Units	Conditions					
		Program Flash Memory								
D130	Eр	Cell Endurance	10,000	—		E/W	-40°C to +125°C			
D131	Vpr	VDD for Read	4.5	—	5.5	V				
D132b	VPEW	VDD for Self-Timed Write	4.5	—	5.5	V				
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C			
D135	IDDP	Supply Current During Programming	-	10	—	mA				
D136a	Trw	Row Write Cycle Time	0.657	_	0.691	ms	Trw = 4965 FRC cycles, Ta = +85°C (see <b>Note 2)</b>			
D136b	Trw	Row Write Cycle Time	0.651	—	0.698	ms	Trw = 4965 FRC cycles, Ta = +125°C (see <b>Note 2)</b>			
D137a	TPE	Page Erase Time	19.44	—	20.44	ms	TPE = 146893 FRC cycles, TA = +85°C (see <b>Note 2)</b>			
D137b	TPE	Page Erase Time	19.24	-	20.65	ms	TPE = 146893 FRC cycles, TA = +125°C (see <b>Note 2)</b>			
D138a	Tww	Word Write Cycle Time	45.78	-	48.15	μs	Tww = 346 FRC cycles, TA = +85°C (see <b>Note 2)</b>			
D138b	Tww	Word Write Cycle Time	45.33	_	48.64	μs	Tww = 346 FRC cycles, TA = +125°C (see <b>Note 2)</b>			

#### TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

**Note 1:** Data in "Typ." column is at 5.0V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.3728 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 30-20) and the value of the FRC Oscillator Tuning register.

#### TABLE 30-14: ELECTRICAL CHARACTERISTICS: INTERNAL BAND GAP REFERENCE VOLTAGE

DC CHARACTERISTICS				$\begin{array}{l} \mbox{Standard Operating Conditions: 4.5V to 5.5V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$							
Param No.	Symbol	Characteristic	Min.	Тур.	Max.	Units	Conditions				
DVR10 VBG Internal Band Gap Reference Voltage			1.14	1.2	1.26	V					

# dsPIC33EVXXXGM00X/10X FAMILY

#### 32.2 IIDLE

FIGURE 32-7: TYPICAL/MAXIMUM lidle vs. Fosc (EC MODE 10 MHz TO 70 MHz, 5.5V MAX)





DS70005144E-page 416



FIGURE 32-12: TYPICAL lidle vs. Vdd (EC MODE, 70 MIPS)



## 32.8 Pull-up and Pull-Down Current









NOTES:

## 33.17 ADC DNL



## 33.18 ADC INL



FIGURE 33-38: TYPICAL INL (VDD = 5.5V, +150°C)

#### 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS				
[	MIN	NOM	MAX			
Number of Pins	N		28			
Pitch	e		0.65 BSC			
Overall Height	A	-	-	2.00		
Molded Package Thickness	A2	1.65	1.75	1.85		
Standoff	A1	0.05	-	-		
Overall Width	E	7.40	7.80	8.20		
Molded Package Width	E1	5.00	5.30	5.60		
Overall Length	D	9.90	10.20	10.50		
Foot Length	L	0.55	0.75	0.95		
Footprint	L1		1.25 REF			
Lead Thickness	С	0.09	-	0.25		
Foot Angle	φ	0°	4°	8°		
Lead Width	b	0.22	-	0.38		

#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.

- 3. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

#### 64-Lead Very Thin Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [VQFN] With 7.15 x 7.15 Exposed Pad [Also called QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-149D [MR] Sheet 1 of 2