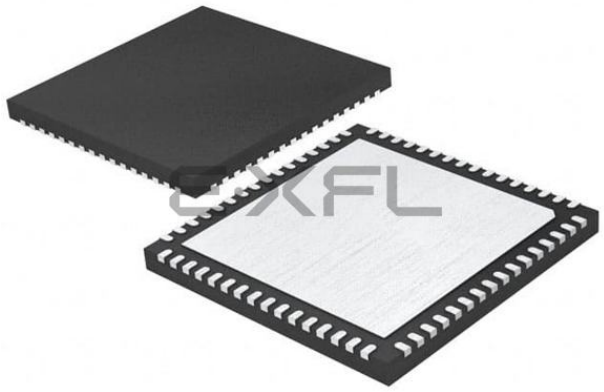

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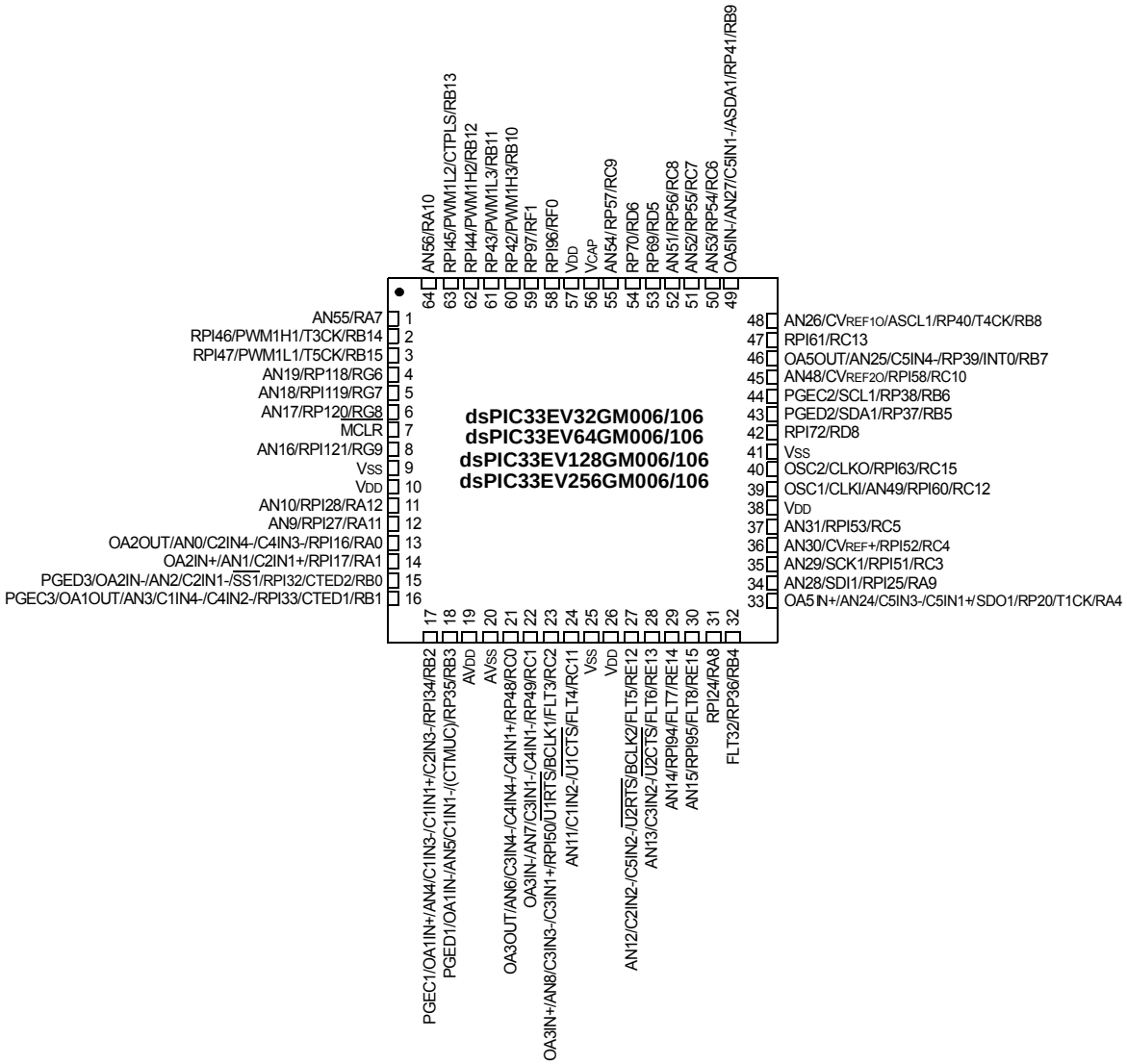
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (22K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 36x10/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ev64gm106-e-mr

Pin Diagrams (Continued)

64-Pin QFN(1,2,3,4)



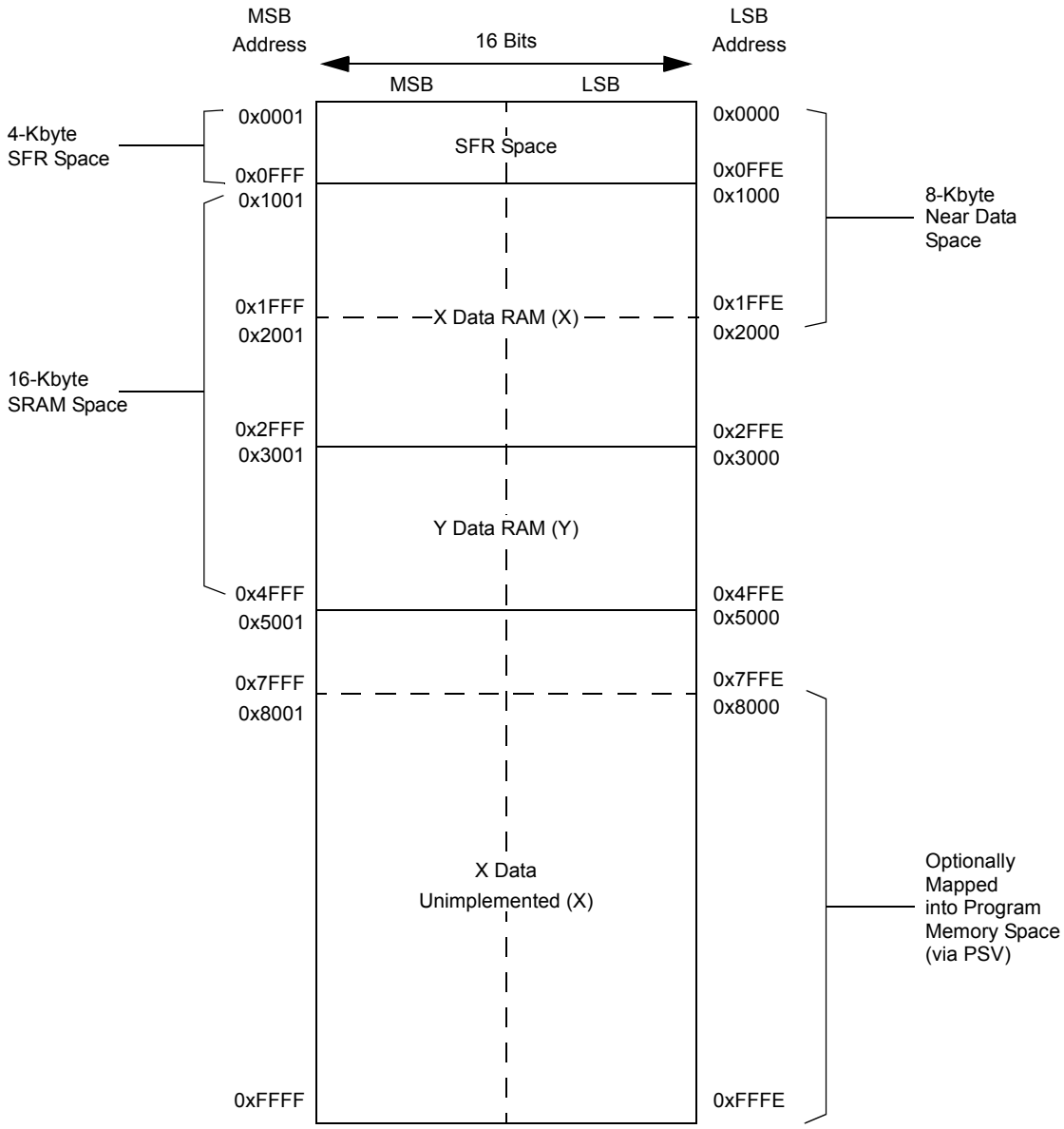
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON<10>) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

FIGURE 4-8: DATA MEMORY MAP FOR 256-Kbyte DEVICES(1)



Note 1: Memory areas are not shown to scale.

TABLE 4-24: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-41: PORTF REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E64	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF<1:0>		0003
PORTF	0E66	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF<1:0>		xxxx
LATF	0E68	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF<1:0>		xxxx
ODCF	0E6A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF<1:0>		0000
CNENF	0E6C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF<1:0>		0000
CNPUF	0E6E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF<1:0>		0000
CNPDF	0E70	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF<1:0>		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: PORTG REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E78	—	—	—	—	—	—	TRISG<9:6>				—	—	—	—	—	—	03C0
PORTG	0E7A	—	—	—	—	—	—	RG<9:6>				—	—	—	—	—	—	xxxx
LATG	0E7C	—	—	—	—	—	—	LATG<9:6>				—	—	—	—	—	—	xxxx
ODCG	0E7E	—	—	—	—	—	—	ODCG<9:6>				—	—	—	—	—	—	0000
CNENG	0E80	—	—	—	—	—	—	CNIEG<9:6>				—	—	—	—	—	—	0000
CNPUG	0E82	—	—	—	—	—	—	CNPUG<9:6>				—	—	—	—	—	—	0000
CNPDG	0E84	—	—	—	—	—	—	CNPDG<9:6>				—	—	—	—	—	—	0000
ANSELG	0E86	—	—	—	—	—	—	ANSG<9:6>				—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 11-8: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **U1RXR<7:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-9: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2RXR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **U2RXR<7:0>:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK2R<7:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **SDI2R<7:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-28: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R5(1)	RP120R4(1)	RP120R3(1)	RP120R2(1)	RP120R1(1)	RP120R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP176R<5:0>:** Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits(1) (see Table 11-3 for peripheral function numbers)

Note 1: RP120R<5:0> is present in dsPIC33EVXXXGM006/106 devices only.

REGISTER 11-29: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP178R<5:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP177R<5:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 11-3 for peripheral function numbers)

13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

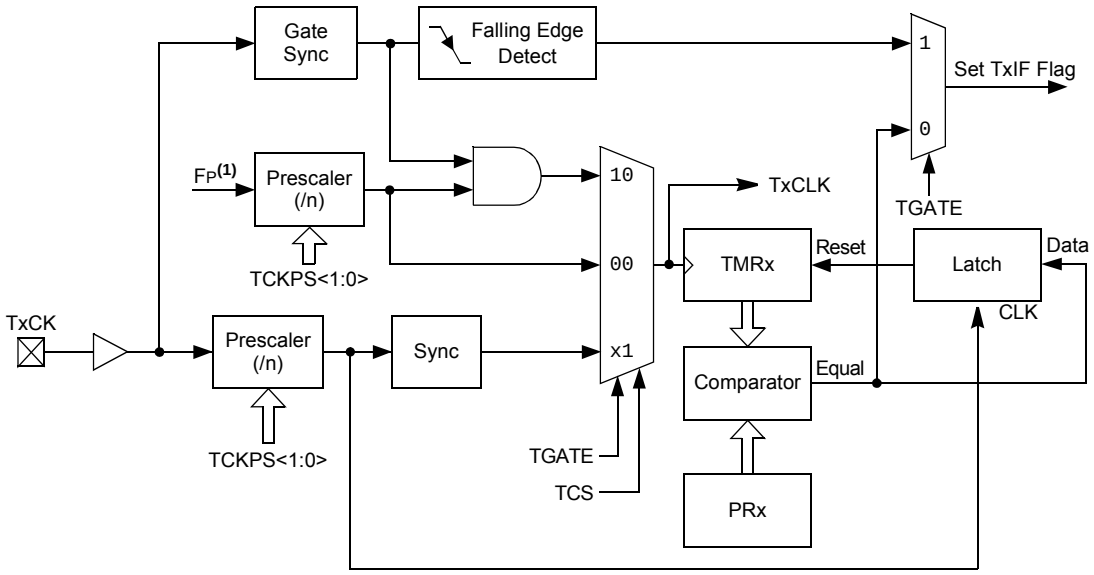
Note: For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

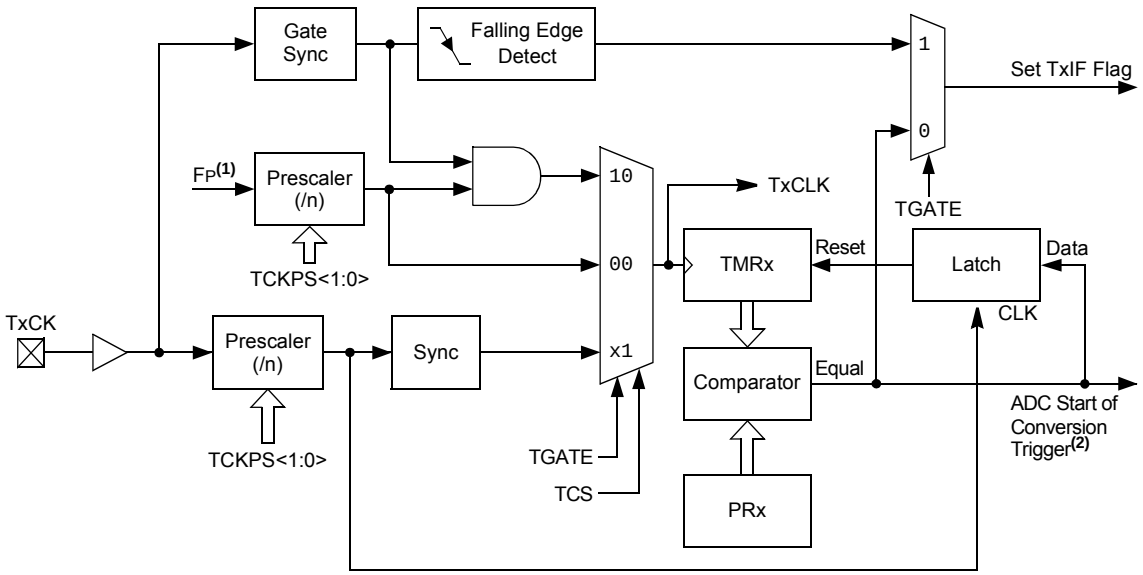
Note: Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)



Note 1: FP is the peripheral clock.

FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



Note 1: FP is the peripheral clock.
2: The ADC trigger is available on TMR3 and TMR5 only.

REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

bit 2-0 **OCM<2:0>:** Output Compare x Mode Select bits

111 = Center-Aligned PWM mode: Output sets high when OCxTMR = OCxR and sets low when OCxTMR = OCxRS(1)

110 = Edge-Aligned PWM mode: Output sets high when OCxTMR = 0 and sets low when OCxTMR = OCxR(1)

101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS

100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle

011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin

010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low

001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high

000 = Output compare channel is disabled

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER

HS-0, HC	HS-0, HC	HS-0, HC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(2)	MDCS(2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP(3)	—	—	CAM(2,4)	XPRES(5)	IUE(2)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = Fault interrupt is not pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = Current-limit interrupt is not pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = Trigger interrupt is not pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = Trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
3: DTC<1:0> = 11 for DTCP to be effective; else, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HSC	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C master; applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + $\overline{ACK}$)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^2C Slave mode only)
1 = Indicates I^2C bus is in an Acknowledge sequence, set on 8^{th} falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9^{th} rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^2C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a master or slave transmit operation
0 = Bus collision has not been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software
0 = Collision has not occurred

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = Overflow has not occurred

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Indicates that a Stop bit was not detected last

REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<15:8>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<7:0>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<15:0>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<31:24>							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF<23:16>							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF<31:16>:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

Figure 25-2, shows the user-programmable blanking function block diagram.

FIGURE 25-2: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

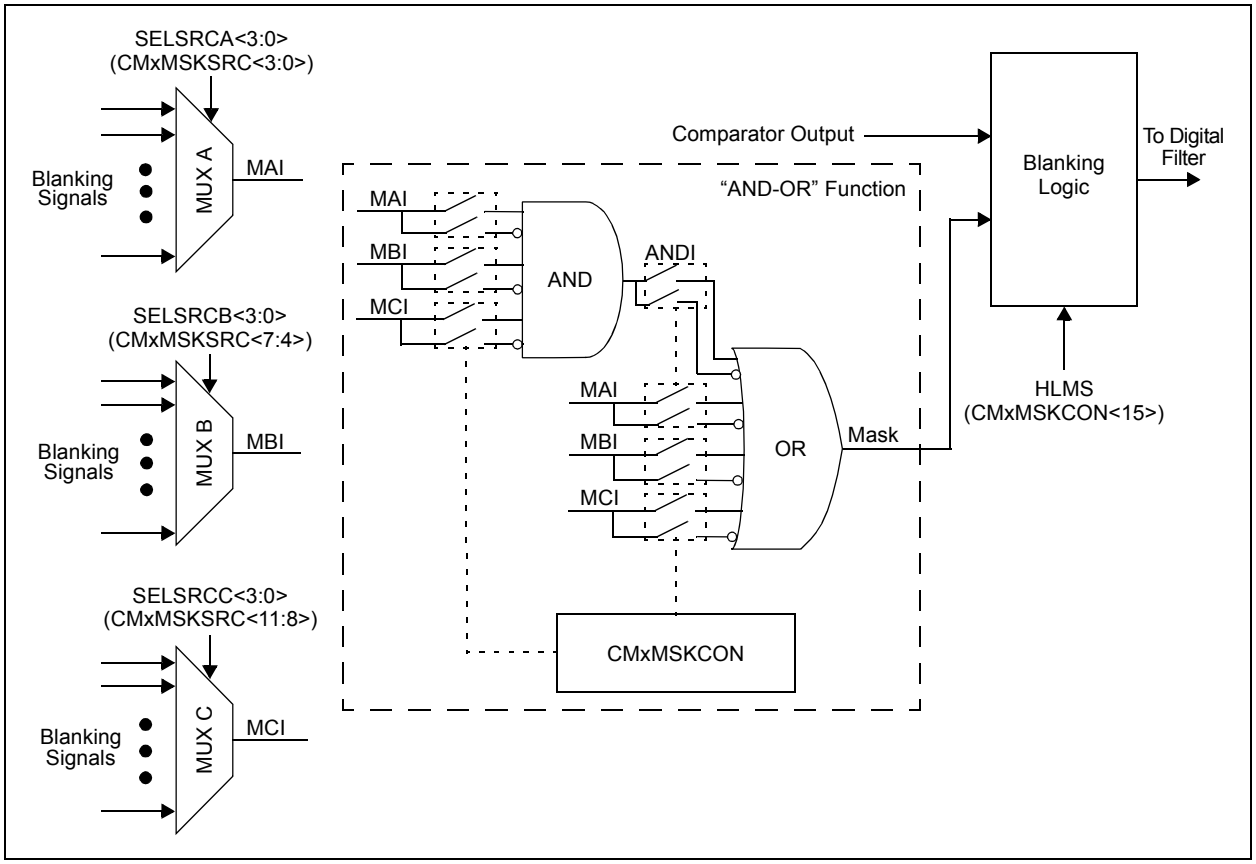
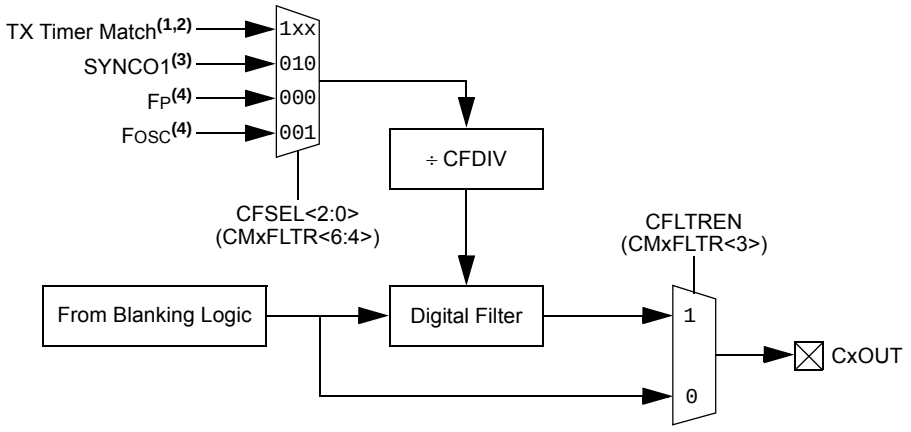


Figure 25-3, shows the digital filter interconnect block diagram.

FIGURE 25-3: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the PWMx Module Register Interconnect Diagram (Figure 17-2).
4: See the Oscillator System Diagram (Figure 9-1).

FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

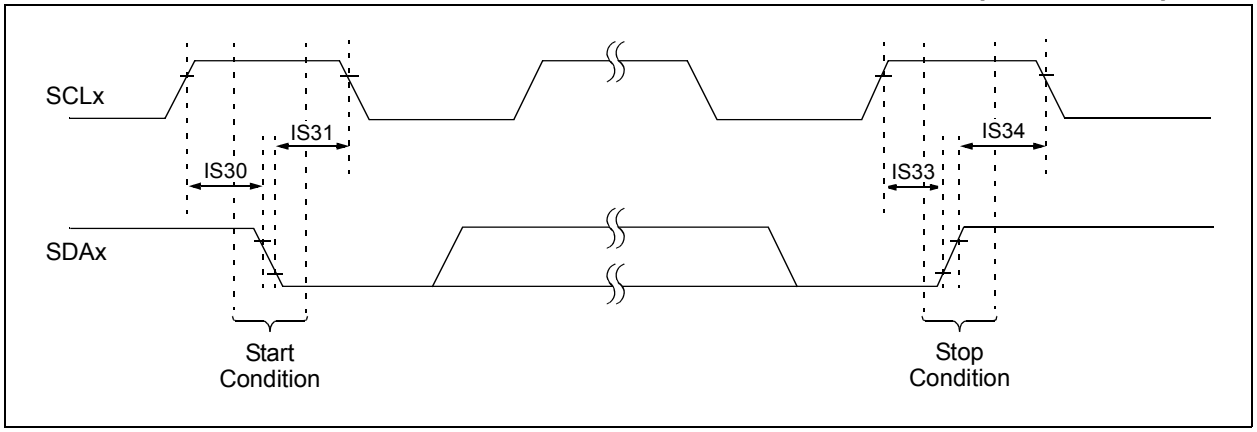


FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

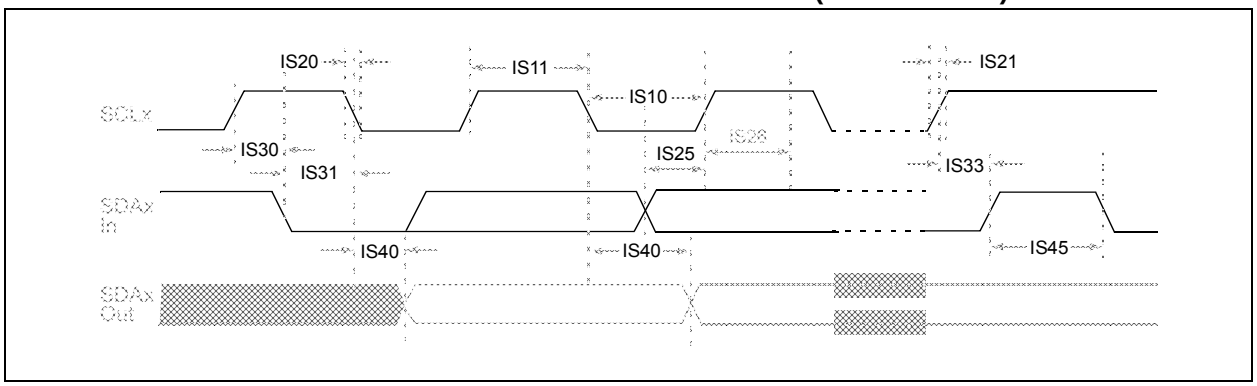


TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Power-Down Current (IPD)						
HDC60e	1300	2500	μA	+150°C	5V	Base Power-Down Current
HDC61c	10	50	μA	+150°C	5V	Watchdog Timer Current: ΔIWDT

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC40e	2.6	5.0	mA	+150°C	5V	10 MIPS
HDC42e	3.6	7.0	mA	+150°C	5V	20 MIPS

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC20e	5.9	8.0	mA	+150°C	5V	10 MIPS
HDC22e	10.3	15.0	mA	+150°C	5V	20 MIPS
HDC23e	19.0	25.0	mA	+150°C	5V	40 MIPS

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Parameter No.	**Typical**	**Max**	**Doze Ratio**	**Units**	**Conditions**		
HDC73a	18.5	22.0	1:2	mA	+150°C	5V	40 MIPS
HDC73g	8.35	12.0	1:128	mA			

31.2 AC Characteristics and Timing Parameters

The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

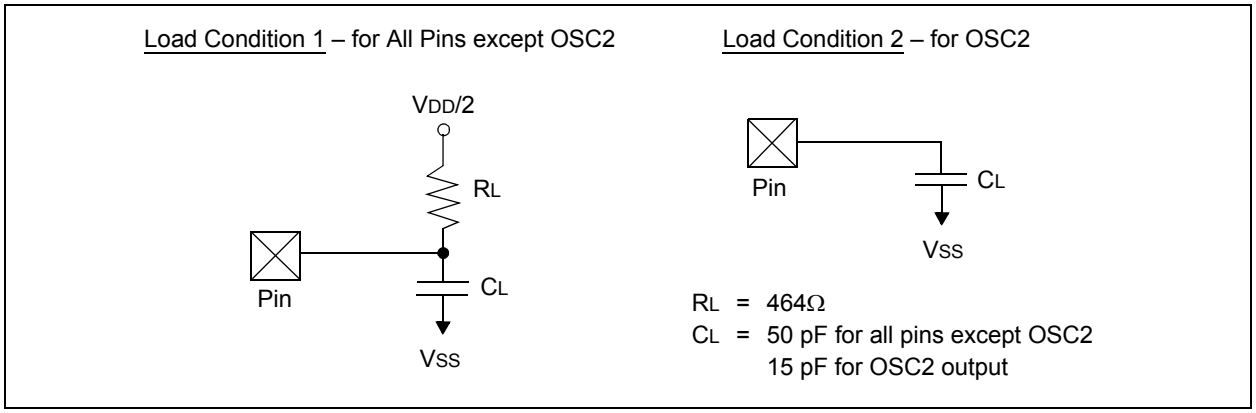


TABLE 31-13: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
HOS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
HOS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
HOS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
HOS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	

Note 1: Data in "Typ." column is at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{FOSC}{\text{Time Base or Communication Clock}}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$\text{Effective Jitter} = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 31-14: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
HF20C	FRC	-3	1	+3	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

TABLE 31-15: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
LPRC @ 32.768 kHz(1,2)							
HF21C	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 27.5 "Watchdog Timer (WDT)"** for more information.

FIGURE 33-27: TYPICAL V_{OH} 4x DRIVER PINS vs. I_{OH} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

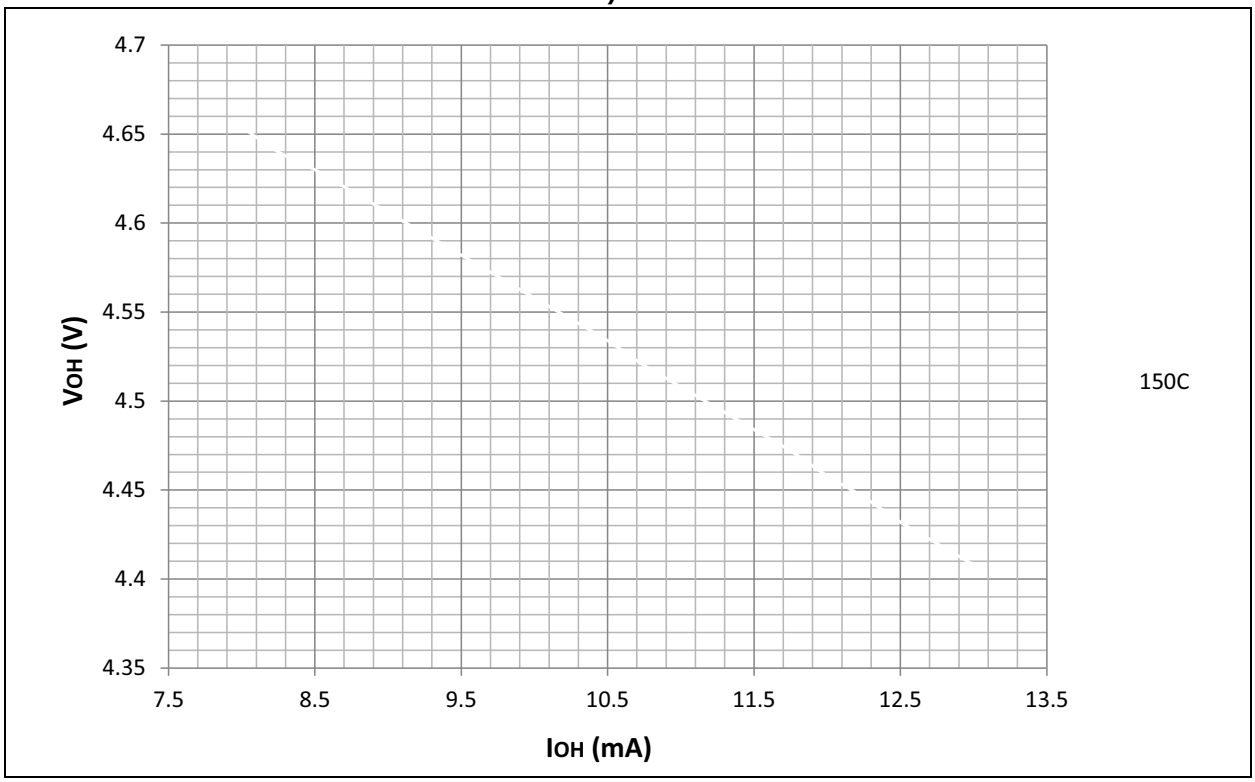
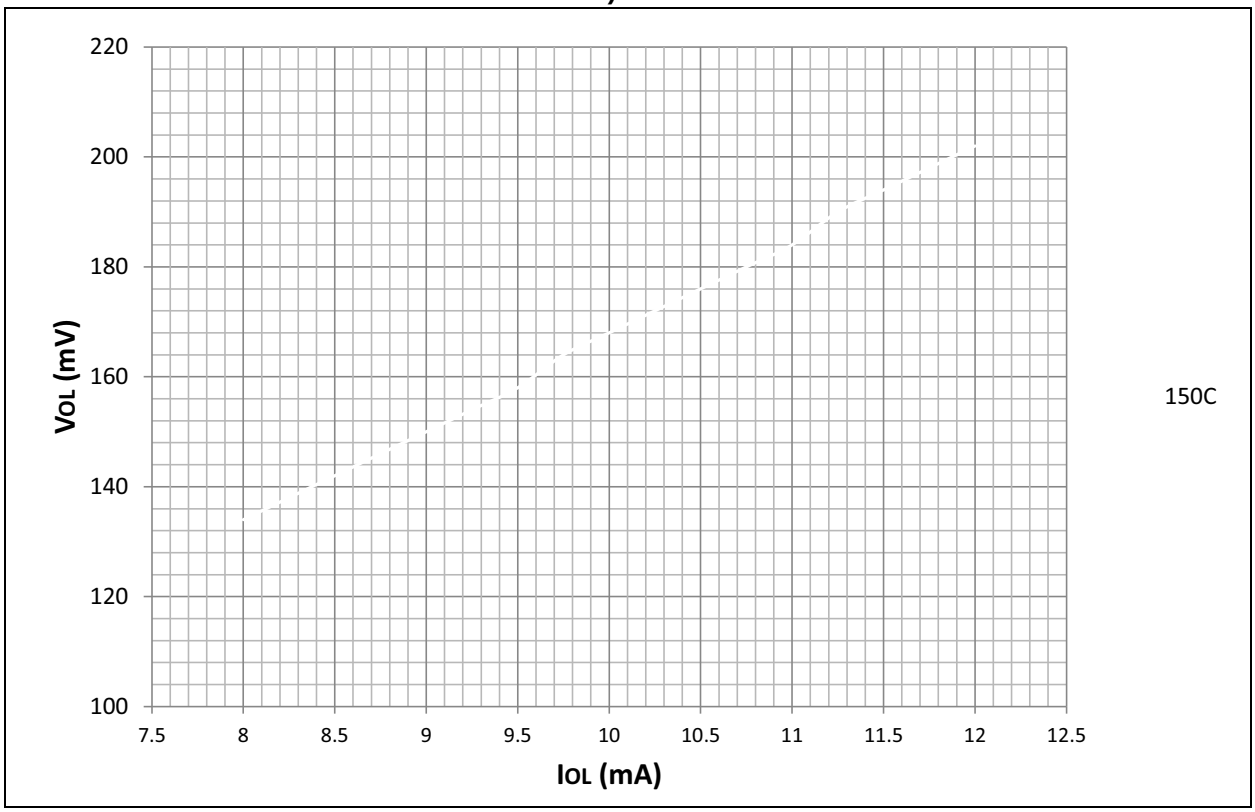


FIGURE 33-28: TYPICAL V_{OL} 8x DRIVER PINS vs. I_{OL} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



33.14 Comparator Op Amp Offset

FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. VCM

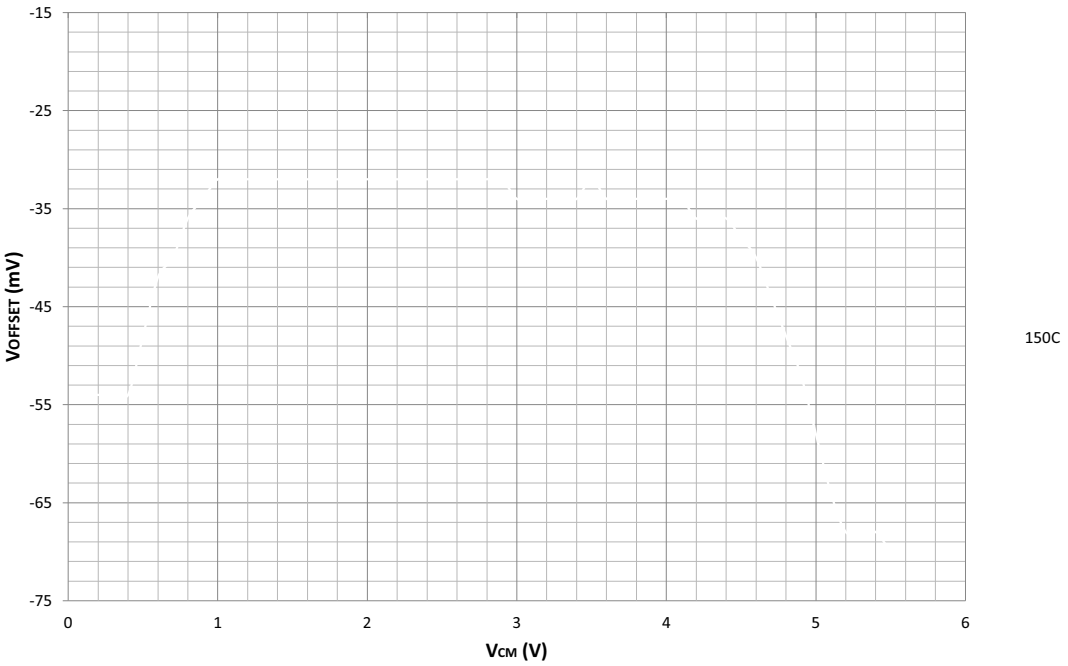


FIGURE 33-34: TYPICAL OP AMP OFFSET vs. VCM