Infineon Technologies - C164CM4EFABFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	P-TQFP-64-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c164cm4efabfxuma1

Data Sheet, V1.0, May 2001

C164CM/SM

16-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

16-Bit Single-Chip Microcontroller **C164CM**
C166 Family

C164CM, C164SM

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 32 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
  - 2 KBytes On-Chip Internal RAM (IRAM)
  - 32 KBytes On-Chip Program Mask ROM or OTP Memory
- On-Chip Peripheral Modules
  - 8-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - 12-Channel General Purpose Capture/Compare Unit (CAPCOM2)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 3 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - On-Chip CAN Interface (Rev. 2.0B active) with 15 Message Objects (Full CAN/Basic CAN)
  - On-Chip Real Time Clock
- Up to 64 KBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed External Address/Data Bus with
    - 8-Bit Data Bus Width (2 KBytes Address Space, A10 … A0, Serial Interfaces)
    - 16-Bit Data Bus Width (64 KBytes Address Space, A15 … A0)
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 50 General Purpose I/O Lines

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C164CM please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C164CM derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers are especially suited for cost sensitive applications. They combine high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM or OTP, internal RAM, and extension RAM.

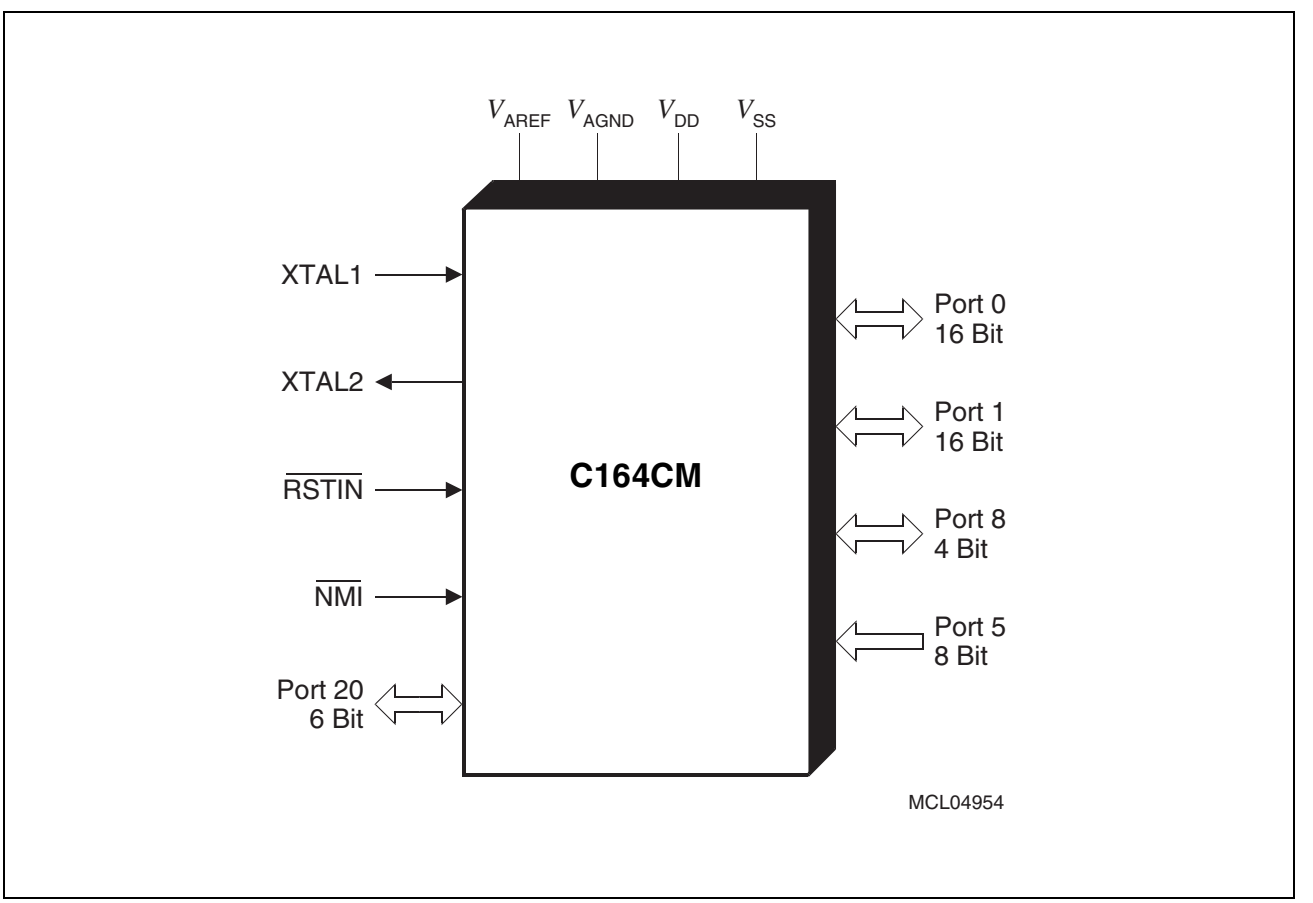

Figure 1 Logic Symbol

Table 2 Pin Definitions and Functions

Symbol	Pin No.	Input Outp.	Function	
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes.	
P0H.7	8	(I)/O	A(D)15	Most Significant Address(/Data) Line
		I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P0H.6	9	(I)/O	A(D)14	Address(/Data) Line
		I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P0H.5	10	(I)/O	A(D)13	Address(/Data) Line
		I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P0H.4	11	(I)/O	A(D)12	Address(/Data) Line
		I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P0H.3	12	(I)/O	A(D)11	Address(/Data) Line
		O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P0H.2	13	(I)/O	A(D)10	Address(/Data) Line
P0H.1	14	(I)/O	A(D)9	Address(/Data) Line
P0H.0	15	(I)/O	A(D)8	Address(/Data) Line
P0L.7	18	I/O	AD7	Address/Data Line
P0L.6	19	I/O	AD6	Address/Data Line
P0L.5	20	I/O	AD5	Address/Data Line
P0L.4	21	I/O	AD4	Address/Data Line
P0L.3	22	I/O	AD3	Address/Data Line
P0L.2	23	I/O	AD2	Address/Data Line
P0L.1	24	I/O	AD1	Address/Data Line
P0L.0	25	I/O	AD0	Least Significant Address/Data Line
$\overline{\text{NMI}}$	26	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C164CM into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.	

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P20		IO	Port 20 is a 6-bit bidirectional I/O port (no P20.5 output driver in the OTP versions). It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 20 pins also serve for alternate functions:
P20.0	28	O	$\overline{RD}$ External Memory Read Strobe, activated for every external instruction or data read access.
P20.1	29	O	$\overline{WR}$ External Memory Write Strobe, activated for every external data write access.
P20.4	30	O	ALE Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P20.5	31	I	$\overline{EA}$ External Access Enable pin. **A low level** at this pin during and after Reset forces the C164CM to latch the configuration from PORT0 and pin $\overline{RD}$, and to begin instruction execution out of external memory. **A high level** forces the C164CM to latch the configuration from pins $\overline{RD}$, ALE, and $\overline{WR}$, and to begin instruction execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
		–	V_{PP} OTP Programming voltage The OTP versions of the C164CM receive the programming voltage via this pin. (No output driver for P20.5 in this case!)
P20.8	34	O	CLKOUT System Clock Output (= CPU Clock),
		O	FOUT Programmable Frequency Output
P20.12	35	O	$\overline{RSTOUT}$ Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{RSTOUT}$ remains low until the EINIT (end of initialization) instruction is executed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following PORT1 pins also serve for alt. functions:
P1L.0	36	I/O	CC60 CAPCOM6: Input / Output of Channel 0
P1L.1	37	O	COUT60 CAPCOM6: Output of Channel 0
P1L.2	38	I/O	CC61 CAPCOM6: Input / Output of Channel 1
P1L.3	39	O	COUT61 CAPCOM6: Output of Channel 1
P1L.4	40	I/O	CC62 CAPCOM6: Input / Output of Channel 2
P1L.5	41	O	COUT62 CAPCOM6: Output of Channel 2
P1L.6	42	O	COUT63 Output of 10-bit Compare Channel
P1L.7	43	I	$\overline{\text{CTRAP}}$ CAPCOM6: Trap Input $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
P1H.0	44	I	$\overline{\text{CC6POS0}}$ CAPCOM6: Position 0 Input,
		I	EX0IN Fast External Interrupt 0 Input,
		I/O	$\overline{\text{CC28IO}}$ CAPCOM2: CC28 Capture Inp./Compare Outp.
P1H.1	45	I	$\overline{\text{CC6POS1}}$ CAPCOM6: Position 1 Input,
		I	EX1IN Fast External Interrupt 1 Input,
		I/O	$\overline{\text{CC29IO}}$ CAPCOM2: CC29 Capture Inp./Compare Outp.
P1H.2	46	I	$\overline{\text{CC6POS2}}$ CAPCOM6: Position 2 Input,
		I	EX2IN Fast External Interrupt 2 Input,
		I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P1H.3	47	I	EX3IN Fast External Interrupt 3 Input,
		I	T7IN CAPCOM2: Timer T7 Count Input,
		I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P1H.4	52	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	53	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	54	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	55	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	49	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	50	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P8		IO	Port 8 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The following Port 8 pins also serve for alternate functions:
P8.0	56	I/O I	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp., CAN1_RxD CAN1 Receive Data Input
P8.1	57	I/O O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp., CAN1_TxD CAN1 Transmit Data Output
P8.2	58	I/O I	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp., CAN1_RxD CAN1 Receive Data Input
P8.3	59	I/O O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp., CAN1_TxD CAN1 Transmit Data Output *Note: The CAN interface lines are only available in the C164CM.*
P5		I	Port 5 is an 8-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	62	I	AN0
P5.1	63	I	AN1
P5.2	64	I	AN2, T3EUD GPT1 Timer T3 Ext. Up/Down Ctrl. Inp.
P5.3	1	I	AN3, T3IN GPT1 Timer T3 Count Input
P5.4	2	I	AN4, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.5	3	I	AN5, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.6	4	I	AN6, T2IN GPT1 Timer T2 Count Input
P5.7	5	I	AN7, T4IN GPT1 Timer T4 Count Input
V_{AGND}	60	–	Reference ground for the A/D converter.
V_{AREF}	61	–	Reference voltage for the A/D converter.
V_{DD}	7, 16, 32, 48	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥2.5 V during power down mode.
V_{SS}	6, 17, 33, 51	–	Digital Ground.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of two different external memory access modes, which are as follows:

– 16-bit Addresses, 16-bit Data, Multiplexed
– 11-bit Addresses, 8-bit Data, Multiplexed

Both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.

In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Note: The programmable bus features and the window mechanism are standard features of the C166 architecture. Due to the C164CM's limited external address space, however, they can be utilized only to a small extend.

The C164CM will preferably be used in single-chip mode. Applications which require access to external resources such as peripherals or small memories, will use the 8-bit data bus with 11-bit address bus in most cases. In this case the upper pins of PORT0 can be used for the serial interfaces. If a wider address or a 16-bit data bus is required the serial interfaces cannot be used.

Table 3 C164CM Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM 6 Timer 12	T12IR	T12IE	T12INT	$00'0134_H$	$4D_H$
CAPCOM 6 Timer 13	T13IR	T13IE	T13INT	$00'0138_H$	$4E_H$
CAPCOM 6 Emergency	CC6EIR	CC6EIE	CC6EINT	$00'013C_H$	$4F_H$

The Capture/Compare Unit CAPCOM2

The general purpose CAPCOM2 unit supports generation and control of timing sequences on up to 12 channels with a maximum resolution of 16 TCL. The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.
Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.
Each dual purpose capture/compare register, which may be individually allocated to either CAPCOM timer and programmed for capture or compare function, has one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘capture’d) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers. When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

Table 5 Compare Modes (CAPCOM)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare time overflow; only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; pin toggles on each compare match; several compare events per timer period are possible. Registers CC16 & CC24 → pin CC16IO Registers CC17 & CC25 → pin CC17IO Registers CC18 & CC26 → pin CC18IO Registers CC19 & CC27 → pin CC19IO

CAN-Module

The integrated CAN-Module handles the completely autonomous transmission and reception of CAN frames in accordance with the CAN specification V2.0 part B (active), i.e. the on-chip CAN-Modules can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

The module provides Full CAN functionality on up to 15 message objects. Message object 15 may be configured for Basic CAN functionality. Both modes provide separate masks for acceptance filtering which allows to accept a number of identifiers in Full CAN mode and also allows to disregard a number of identifiers in Basic CAN mode. All message objects can be updated independent from the other objects and are equipped for the maximum message length of 8 bytes.

The bit timing is derived from the XCLK and is programmable up to a data rate of 1 Mbit/s. Each CAN-Module uses two pins of Port 4 or Port 8 to interface to an external bus transceiver. The interface pins are assigned via software.

Note: When the CAN interface is assigned to Port 8, the respective CAPCOM IO lines on Port 8 cannot be used.

Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after a reset of the chip, and can only be disabled in the time interval until the EINIT (end of initialization) instruction has been executed. Thus, the chip's start-up procedure is always monitored. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates an internal hardware reset and pulls the $\overline{\text{RSTOUT}}$ pin low in order to allow external hardware components to be reset.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 2/4/128/256. The high byte of the Watchdog Timer register can be set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the high byte of the Watchdog Timer is reloaded. Thus, time intervals between 20 µs and 336 ms can be monitored (@ 25 MHz).
The default Watchdog Timer interval after reset is 5.24 ms (@ 25 MHz).

Oscillator Watchdog

The Oscillator Watchdog (OWD) monitors the clock signal generated by the on-chip oscillator (either with a crystal or via external clock drive). For this operation the PLL provides a clock signal which is used to supervise transitions on the oscillator clock. This PLL clock is independent from the XTAL1 clock. When the expected oscillator clock transitions are missing the OWD activates the PLL Unlock/OWD interrupt node and supplies the CPU with the PLL clock signal. Under these circumstances the PLL will oscillate with its basic frequency.

In direct drive mode the PLL base frequency is used directly (f_{CPU} = 2 … 5 MHz).
In prescaler mode the PLL base frequency is divided by 2 (f_{CPU} = 1 … 2.5 MHz).

Note: The CPU clock source is only switched back to the oscillator clock after a hardware reset.

The oscillator watchdog can be disabled by setting bit OWDDIS in register SYSCON. In this case (OWDDIS = ‘1’) the PLL remains idle and provides no clock signal, while the CPU clock signal is derived directly from the oscillator clock or via prescaler or SDD. Also no interrupt request will be generated in case of a missing oscillator clock.

Note: At the end of a reset bit OWDDIS reflects the inverted level of pin $\overline{RD}$ at that time. Thus the oscillator watchdog may also be disabled via hardware by (externally) pulling the $\overline{RD}$ line low upon a reset, similar to the standard reset configuration via PORT0.

Special Function Registers Overview

Table 7 lists all SFRs which are implemented in the C164CM in alphabetical order. **Bit-addressable** SFRs are marked with the letter "**b**" in column "Name". SFRs within the **Extended SFR-Space** (ESFRs) are marked with the letter "**E**" in column "Physical Address". Registers within on-chip X-peripherals are marked with the letter "**X**" in column "Physical Address".

An SFR can be specified via its individual mnemonic name. Depending on the selected addressing mode, an SFR can be accessed via its physical address (using the Data Page Pointers), or via its short 8-bit address (without using the Data Page Pointers).

Table 7 C164CM Registers, Ordered by Name

Name	Physical Address	8-Bit Addr.	Description	Reset Value
ADCIC b	$FF98_H$	CC_H	A/D Converter End of Conversion Interrupt Control Register	0000_H
ADCON b	$FFA0_H$	$D0_H$	A/D Converter Control Register	0000_H
ADDAT	$FEA0_H$	50_H	A/D Converter Result Register	0000_H
ADDAT2	$F0A0_H$ **E**	50_H	A/D Converter 2 Result Register	0000_H
ADDRSEL1	$FE18_H$	$0C_H$	Address Select Register 1	0000_H
ADDRSEL2	$FE1A_H$	$0D_H$	Address Select Register 2	0000_H
ADDRSEL3	$FE1C_H$	$0E_H$	Address Select Register 3	0000_H
ADDRSEL4	$FE1E_H$	$0F_H$	Address Select Register 4	0000_H
ADEIC b	$FF9A_H$	CD_H	A/D Converter Overrun Error Interrupt Control Register	0000_H
BUSCON0 b	$FF0C_H$	86_H	Bus Configuration Register 0	0000_H
BUSCON1 b	$FF14_H$	$8A_H$	Bus Configuration Register 1	0000_H
BUSCON2 b	$FF16_H$	$8B_H$	Bus Configuration Register 2	0000_H
BUSCON3 b	$FF18_H$	$8C_H$	Bus Configuration Register 3	0000_H
BUSCON4 b	$FF1A_H$	$8D_H$	Bus Configuration Register 4	0000_H
C1BTR	$EF04_H$ **X**	---	CAN1 Bit Timing Register	$UUUU_H$
C1CSR	$EF00_H$ **X**	---	CAN1 Control / Status Register	$XX01_H$
C1GMS	$EF06_H$ **X**	---	CAN1 Global Mask Short	$UFUU_H$
C1LARn	$EFn4_H$ **X**	---	CAN Lower Arbitration Register (msg. **n)**	$UUUU_H$
C1LGML	$EF0A_H$ **X**	---	CAN Lower Global Mask Long	$UUUU_H$
C1LMLM	$EF0E_H$ **X**	---	CAN Lower Mask of Last Message	$UUUU_H$

Table 7 C164CM Registers, Ordered by Name (cont'd)

Name	Physical Address	8-Bit Addr.	Description	Reset Value
S0RIC b	$FF6E_H$	$B7_H$	Serial Channel 0 Receive Interrupt Control Register	0000_H
S0TBIC b	$F19C_H$ E	CE_H	Serial Channel 0 Transmit Buffer Interrupt Control Register	0000_H
S0TBUF	$FEB0_H$	58_H	Serial Channel 0 Transmit Buffer Reg. (write only)	0000_H
S0TIC b	$FF6C_H$	$B6_H$	Serial Channel 0 Transmit Interrupt Control Register	0000_H
SP	$FE12_H$	09_H	CPU System Stack Pointer Register	$FC00_H$
SSCBR	$F0B4_H$ E	$5A_H$	SSC Baudrate Register	0000_H
SSCCON b	$FFB2_H$	$D9_H$	SSC Control Register	0000_H
SSCEIC b	$FF76_H$	BB_H	SSC Error Interrupt Control Register	0000_H
SSCRB	$F0B2_H$ E	59_H	SSC Receive Buffer	$XXXX_H$
SSCRIC b	$FF74_H$	BA_H	SSC Receive Interrupt Control Register	0000_H
SSCTB	$F0B0_H$ E	58_H	SSC Transmit Buffer	0000_H
SSCTIC b	$FF72_H$	$B9_H$	SSC Transmit Interrupt Control Register	0000_H
STKOV	$FE14_H$	$0A_H$	CPU Stack Overflow Pointer Register	$FA00_H$
STKUN	$FE16_H$	$0B_H$	CPU Stack Underflow Pointer Register	$FC00_H$
SYSCON b	$FF12_H$	89_H	CPU System Configuration Register	[1] $0xx0_H$
SYSCON1 b	$F1DC_H$ E	EE_H	CPU System Configuration Register 1	0000_H
SYSCON2 b	$F1D0_H$ E	$E8_H$	CPU System Configuration Register 2	0000_H
SYSCON3 b	$F1D4_H$ E	EA_H	CPU System Configuration Register 3	0000_H
T12IC b	$F190_H$ E	$C8_H$	CAPCOM 6 Timer 12 Interrupt Ctrl. Reg.	0000_H
T12OF	$F034_H$ E	$1A_H$	CAPCOM 6 Timer 12 Offset Register	0000_H
T12P	$F030_H$ E	18_H	CAPCOM 6 Timer 12 Period Register	0000_H
T13IC b	$F198_H$ E	CC_H	CAPCOM 6 Timer 13 Interrupt Ctrl. Reg.	0000_H
T13P	$F032_H$ E	19_H	CAPCOM 6 Timer 13 Period Register	0000_H
T14	$F0D2_H$ E	69_H	RTC Timer 14 Register	no
T14REL	$F0D0_H$ E	68_H	RTC Timer 14 Reload Register	no
T2	$FE40_H$	20_H	GPT1 Timer 2 Register	0000_H
T2CON b	$FF40_H$	$A0_H$	GPT1 Timer 2 Control Register	0000_H

Power Consumption C164CM (ROM)

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	1 + 2.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX}	–	1 + 1.1 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]
Sleep and Power-down mode supply current with RTC running	I_{PDR}[2]	–	200 + 25 × f_{OSC}	µA	V_{DD} = V_{DDmax} f_{OSC} in [MHz][3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	V_{DD} = V_{DDmax}[3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 9**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

Power Consumption C164CM (OTP)

(Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Conditions
		min.	max.		
Power supply current (active) with all peripherals active	I_{DD}	–	10 + 3.5 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IL} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals active	I_{IDX}	–	5 + 1.25 × f_{CPU}	mA	$\overline{RSTIN}$ = V_{IH1} f_{CPU} in [MHz][1]
Idle mode supply current with all peripherals deactivated, PLL off, SDD factor = 32	I_{IDO}[2]	–	500 + 50 × f_{OSC}	µA	$\overline{RSTIN}$ = V_{IH1} f_{OSC} in [MHz][1]

Power Consumption C164CM (OTP) (cont'd)
(Operating Conditions apply)

Parameter	Sym-bol	Limit Values		Unit	Test Conditions
		min.	max.		
Sleep and Power-down mode supply current with RTC running	I_{PDR} [2]	–	200 + 25 × f_{OSC}	µA	$V_{DD} = V_{DDmax}$ f_{OSC} in [MHz] [3]
Sleep and Power-down mode supply current with RTC disabled	I_{PDO}	–	50	µA	$V_{DD} = V_{DDmax}$ [3]

1) The supply current is a function of the operating frequency. This dependency is illustrated in **Figure 10**. These parameters are tested at V_{DDmax} and maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}.

2) This parameter is determined mainly by the current consumed by the oscillator (see **Figure 8**). This current, however, is influenced by the external oscillator circuitry (crystal, capacitors). The values given refer to a typical circuitry and may change in case of a not optimized external oscillator circuitry.

3) This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} - 0.1 V to V_{DD}, V_{REF} = 0 V, all outputs (including pins configured as outputs) disconnected.

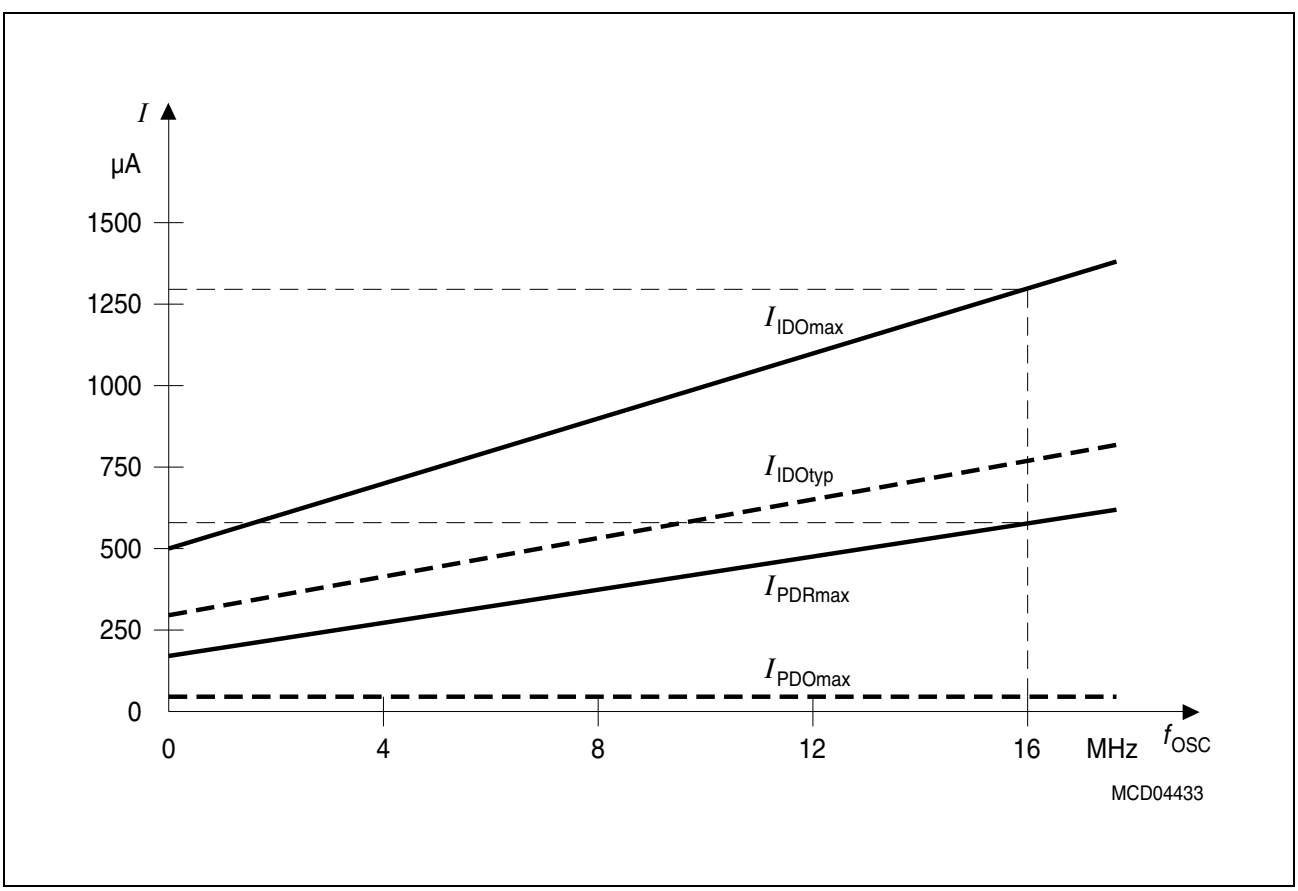

Figure 8 **Idle and Power Down Supply Current as a Function of Oscillator Frequency**

Direct Drive

When direct drive is configured (CLKCFG = 011_B) the on-chip phase locked loop is disabled and the CPU clock is directly driven from the internal oscillator with the input clock signal.
The frequency of f_{CPU} directly follows the frequency of f_{OSC} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{OSC}.
The timings listed below that refer to TCLs therefore must be calculated using the minimum TCL that is possible under the respective circumstances. This minimum value can be calculated via the following formula:

$$TCL_{min} = 1/f_{OSC} \times DC_{min} \qquad \text{(DC = duty cycle)}$$

For two consecutive TCLs the deviation caused by the duty cycle of f_{OSC} is compensated so the duration of 2TCL is always $1/f_{OSC}$. The minimum value TCL_{min} therefore has to be used only once for timings that require an odd number of TCLs (1, 3, …). Timings that require an even number of TCLs (2, 4, …) may use the formula $2TCL = 1/f_{OSC}$.

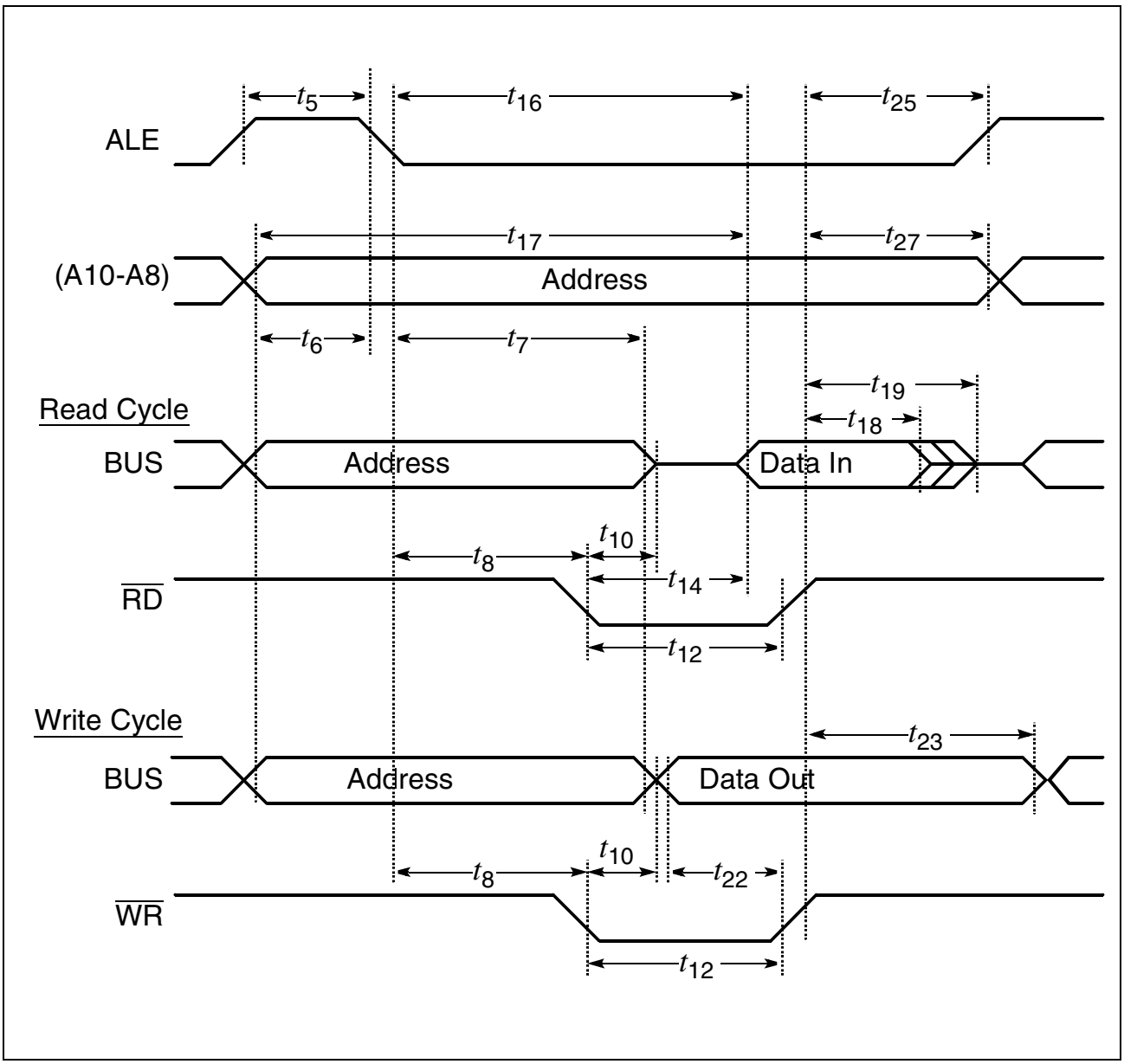

Figure 17 External Memory Cycle:
Multiplexed Bus, With Read/Write Delay, Extended ALE

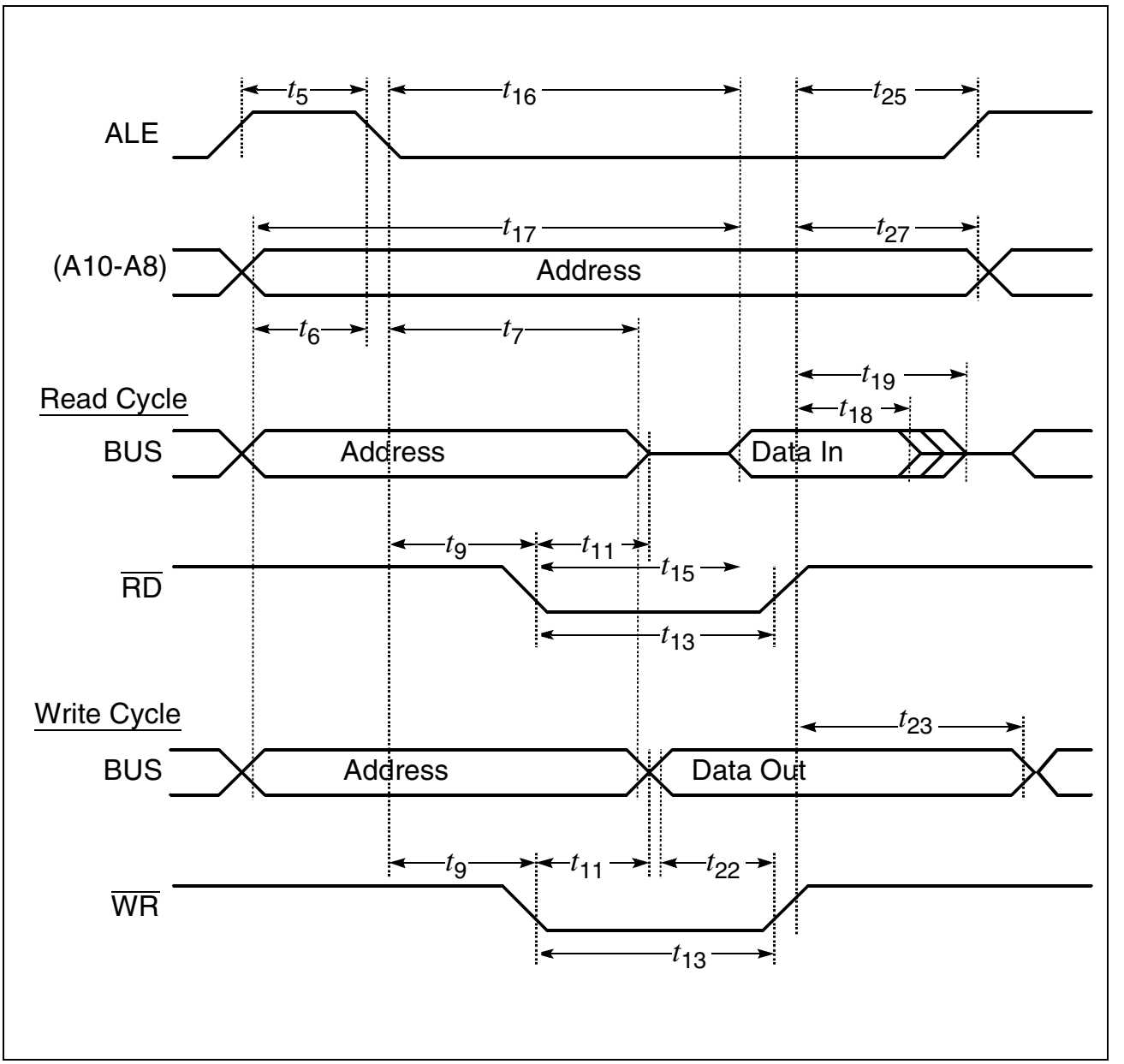

Figure 19 External Memory Cycle:
Multiplexed Bus, No Read/Write Delay, Extended ALE

AC Characteristics

CLKOUT

(Operating Conditions apply)

Parameter	Symbol		Max. CPU Clock = 25 MHz		Variable CPU Clock 1 / 2TCL = 1 to 25 MHz		Unit
			min.	max.	min.	max.	
CLKOUT cycle time	t_{29}	CC	40	40	2TCL	2TCL	ns
CLKOUT high time	t_{30}	CC	14	–	TCL - 6	–	ns
CLKOUT low time	t_{31}	CC	10	–	TCL - 10	–	ns
CLKOUT rise time	t_{32}	CC	–	4	–	4	ns
CLKOUT fall time	t_{33}	CC	–	4	–	4	ns
CLKOUT rising edge to ALE falling edge	t_{34}	CC	0 + t_A	10 + t_A	0 + t_A	10 + t_A	ns

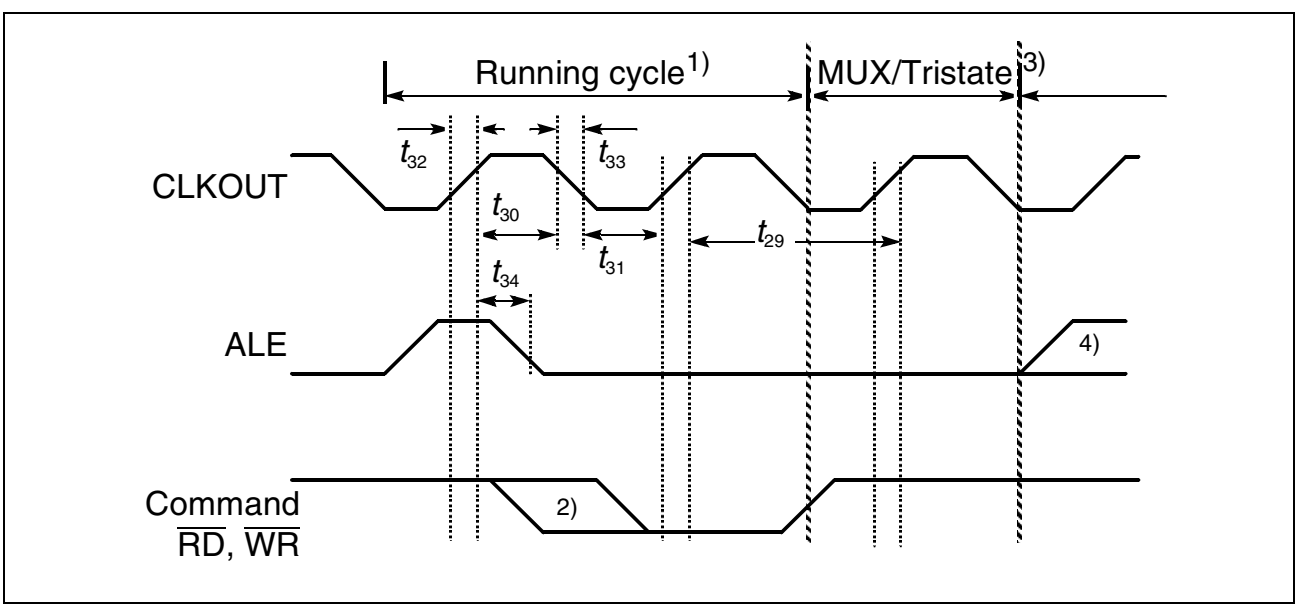

Figure 20 CLKOUT Timing

Notes

1) Cycle as programmed, including MCTC waitstates (Example shows 0 MCTC WS).
2) The leading edge of the respective command depends on RW-delay.
3) Multiplexed bus modes have a MUX waitstate added after a bus cycle, and an additional MTTC waitstate may be inserted here.
   For a multiplexed bus with MTTC waitstate this delay is 2 CLKOUT cycles.
4) The next external bus cycle may start here.