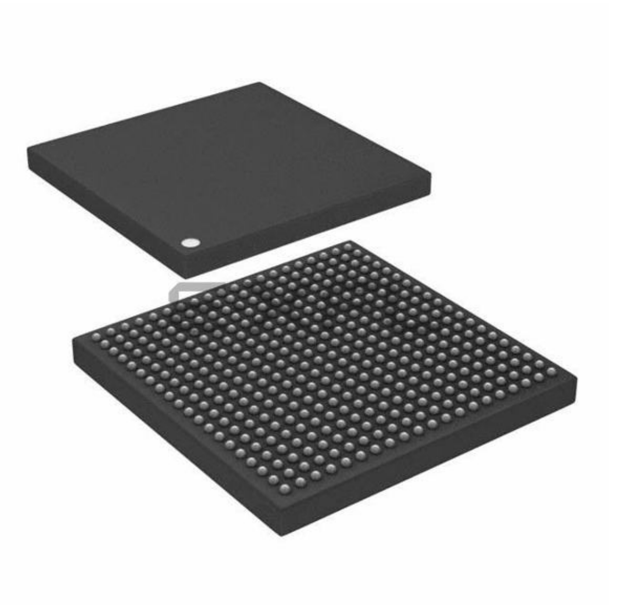

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC1400 Core
Interface	Host Interface, I²C, UART
Clock Rate	200MHz
Non-Volatile Memory	External
On-Chip RAM	400kB
Voltage - I/O	3.30V
Voltage - Core	1.20V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	400-LFBGA
Supplier Device Package	400-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc7115vm800

1 Pin Assignments

This section includes diagrams of the MSC7115 package ball grid array layouts and pinout allocation tables.

1.1 MAP-BGA Ball Layout Diagrams

Top and bottom views of the MAP-BGA package are shown in **Figure 2** and **Figure 3** with their ball location index numbers.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	GND	GND	DQM1	DQS2	CK	$\overline{CK}$	HD15	HD12	HD10	HD7	HD6	HD4	HD1	HD0	GND	NC	NC	NC	NC	NC
B	V_{DDM}	NC	$\overline{CS0}$	DQM2	DQS3	DQS0	CKE	$\overline{WE}$	HD14	HD11	HD8	HD5	HD2	NC	NC	NC	NC	NC	NC	NC
C	D24	D30	D25	$\overline{CS1}$	DQM3	DQM0	DQS1	$\overline{RAS}$	$\overline{CAS}$	HD13	HD9	HD3	NC	NC	NC	NC	NC	NC	NC	NC
D	V_{DDM}	D28	D27	GND	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
E	GND	D26	D31	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
F	V_{DDM}	D15	D29	V_{DDC}	V_{DDC}	V_{DDC}	GND	GND	GND	V_{DDM}	V_{DDM}	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	NC	NC	NC
G	GND	D13	GND	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	NC	NC
H	D14	D12	D11	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	NC	HA2	HA1
J	D10	V_{DDM}	D9	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	HA3	$\overline{HACK}$	$\overline{HREQ}$
K	D0	GND	D8	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	HA0	HDDS	$\overline{HDS}$
L	D1	GND	D3	V_{DDC}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{HCS2}$	$\overline{HCS1}$	HRW
M	D2	V_{DDM}	D5	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDC}	V_{DDC}	SDA	UTXD	URXD
N	D4	D6	V_{REF}	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDC}	V_{DDC}	CLKIN	SCL	V_{SSPLL}
P	D7	D17	D16	V_{DDM}	V_{DDM}	V_{DDM}	GND	GND	GND	GND	GND	GND	GND	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	$\overline{PORESET}$	TPSEL	V_{DDPLL}
R	GND	D19	D18	V_{DDM}	V_{DDM}	V_{DDM}	GND	V_{DDM}	GND	V_{DDM}	GND	GND	V_{DDIO}	GND	V_{DDIO}	V_{DDIO}	V_{DDC}	TDO	EE0	TEST0
T	V_{DDM}	D20	D22	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDC}	V_{DDM}	V_{DDM}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDIO}	V_{DDC}	V_{DDC}	NC	TMS	$\overline{HRESET}$
U	GND	D21	D23	V_{DDM}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	V_{DDC}	NC	TCK	$\overline{TRST}$
V	V_{DDM}	NC	A13	A11	A10	A5	A2	BA0	NC	EVNT0	EVNT4	T0TCK	T1RFS	T1TD	T2RD	T2TD	GPIA22	GPIA24	NC	TDI
W	GND	V_{DDM}	A12	A8	A7	A6	A3	NC	EVNT1	EVNT2	T0RFS	T0TFS	T1RD	T1TFS	T2RFS	T2TFS	GPIA19	GPIA23	GPIA26	H8BIT
Y	V_{DDM}	GND	A9	A1	A0	A4	BA1	$\overline{NMI}$	EVNT3	T0RCK	T0RD	T0TD	T1RCK	T1TCK	T2RCK	T2TCK	GPIA20	GPIA21	GND	GPIA25

Figure 2. MSC7115 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

Table 1. MSC7115 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
D13	V_{DDIO}					
D14	V_{DDIO}					
D15	V_{DDIO}					
D16	V_{DDIO}					
D17	V_{DDC}					
D18	NC					
D19	NC					
D20	NC					
E1	GND					
E2	D26					
E3	D31					
E4	V_{DDM}					
E5	V_{DDM}					
E6	V_{DDC}					
E7	V_{DDC}					
E8	V_{DDC}					
E9	V_{DDC}					
E10	V_{DDM}					
E11	V_{DDIO}					
E12	V_{DDIO}					
E13	V_{DDIO}					
E14	V_{DDIO}					
E15	V_{DDIO}					
E16	V_{DDC}					
E17	V_{DDC}					
E18	NC					
E19	NC					
E20	NC					
F1	V_{DDM}					
F2	D15					
F3	D29					
F4	V_{DDC}					
F5	V_{DDC}					
F6	V_{DDC}					
F7	GND					
F8	GND					
F9	GND					
F10	V_{DDM}					

Table 1. MSC7115 Signals by Ball Designator (continued)

Number	Signal Names					
	End of Reset	Software Controlled			Hardware Controlled	
		GPI Enabled (Default)	Interrupt Enabled	GPO Enabled	Primary	Alternate
M3	D5					
M4	V_{DDM}					
M5	V_{DDM}					
M6	GND					
M7	GND					
M8	GND					
M9	GND					
M10	GND					
M11	GND					
M12	GND					
M13	GND					
M14	GND					
M15	GND					
M16	V_{DDC}					
M17	V_{DDC}					
M18	GPIA14		$\overline{IRQ15}$	GPOA14	SDA	
M19	GPIA12		$\overline{IRQ3}$	GPOA12	UTXD	
M20	GPIA13		$\overline{IRQ2}$	GPOA13	URXD	
N1	D4					
N2	D6					
N3	V_{REF}					
N4	V_{DDM}					
N5	V_{DDM}					
N6	V_{DDM}					
N7	GND					
N8	GND					
N9	GND					
N10	GND					
N11	GND					
N12	GND					
N13	GND					
N14	GND					
N15	V_{DDIO}					
N16	V_{DDC}					
N17	V_{DDC}					
N18	CLKIN					
N19	GPIA15		$\overline{IRQ14}$	GPOA15	SCL	
N20	V_{SSPLL}					

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Value	Unit
Core supply voltage	V_{DDC}	1.14 to 1.26	V
Memory supply voltage	V_{DDM}	2.38 to 2.63	V
PLL supply voltage	V_{DDPLL}	1.14 to 1.26	V
I/O supply voltage	V_{DDIO}	3.14 to 3.47	V
Reference voltage	V_{REF}	1.19 to 1.31	V
Operating temperature range	T_J T_A	maximum: 105 minimum: –40	°C °C

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC7115 for the MAP-BGA package.

Table 4. Thermal Characteristics for MAP-BGA Package

Characteristic	Symbol	MAP-BGA 17 × 17 mm[5]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	39	31	°C/W
Junction-to-ambient, four-layer board[1, 3]	$R_{\theta JA}$	23	20	°C/W
Junction-to-board[4]	$R_{\theta JB}$	12		°C/W
Junction-to-case[5]	$R_{\theta JC}$	7		°C/W
Junction-to-package-top[6]	Ψ_{JT}	2		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD 51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Section 3.1, *Thermal Design Considerations* explains these characteristics in detail.

2.5 AC Timings

This section presents timing diagrams and specifications for individual signals and parallel I/O outputs and inputs. All AC timings are based on a 30 pF load, except where noted otherwise, and a 50 Ω transmission line. For any additional pF, use the following equations to compute the delay:

- Standard interface: $2.45 + (0.054 \times C_{load})$ ns
- DDR interface: $1.6 + (0.002 \times C_{load})$ ns

2.5.1 Clock and Timing Signals

The following tables describe clock signal characteristics. **Table 7** shows the maximum frequency values for internal (core, reference, and peripherals) and external (CLKO) clocks. You must ensure that maximum frequency values are not exceeded (see for the allowable ranges when using the PLL).

Table 7. Maximum Frequencies

Characteristic	Maximum in MHz	
	Mask Set 1L44X	Mask Set 1M88B
Core clock frequency (CLOCK)	200	266
External output clock frequency (CLKO)	50	67
Memory clock frequency (CK, $\overline{CK}$)	100	133
TDM clock frequency (TxRCK, TxTCK)	50	67

Table 8. Clock Frequencies in MHz

Characteristic	Symbol	Min	Max	
			Mask Set 1L44X	Mask Set 1M88B
CLKIN frequency	F_{CLKIN}	10	100	100
CLOCK frequency	F_{CORE}	—	200	266
CK, $\overline{CK}$ frequency	F_{CK}	—	100	133
TDMxRCK, TDMxTCK frequency	F_{TDMCK}	—	50	50
CLKO frequency	F_{CKO}	—	50	67
AHB/IPBus/APB clock frequency	F_{BCK}	—	100	133
Note: The rise and fall time of external clocks should be 5 ns maximum				

Table 9. System Clock Parameters

Characteristic	Min	Max	Unit
CLKIN frequency	10	100	MHz
CLKIN slope	—	5	ns
CLKIN frequency jitter (peak-to-peak)	—	1000	ps
CLKO frequency jitter (peak-to-peak)	—	150	ps

2.5.2 Configuring Clock Frequencies

This section describes important requirements for configuring clock frequencies in the MSC7115 device when using the PLL block. To configure the device clocking, you must program four fields in the Clock Control Register (CLKCTL):

- PLLDVF field. Specifies the PLL division factor. The output of the divider block is the input to the multiplier block.
- PLLMLTF field. Specifies the PLL multiplication factor. The output from the multiplier block is the VCO.
- RNG field. Selects the available PLL frequency range.
- CKSEL field. Selects the source for the core clock.

There are restrictions on the frequency range permitted at the beginning of the multiplication portion of the PLL that affect the allowable values for the PLLDVF and PLLMLTF fields. The following sections define these restrictions and provide guidelines to configure the device clocking when using the PLL. Refer to the Clock and Power Management chapter in the *MSC711x Reference Manual* for details on the clock programming model.

Table 21. TDM Timing

No.	Characteristic	Expression	Min	Max	Units
307	TDMxTCK High to TDMxTD output valid		—	14.0	ns
308	TDMxTD hold time		2.0	—	ns
309	TDMxTCK High to TDMxTD output high impedance		—	10.0	ns
310	TDMXTFS/TDMxRFS output valid		—	13.5	ns
311	TDMxTFS/TDMxRFS output hold time		2.5	—	ns

Notes:
1. Output values are based on 30 pF capacitive load.
2. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. Refer to the *MSC711x Reference Manual* for details. TDMxTCK and TDMxRCK are shown using the rising edge.

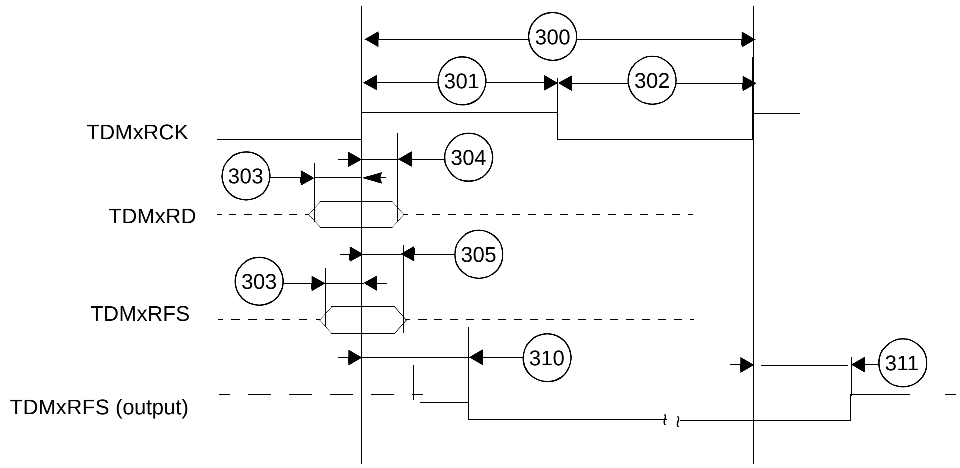

Figure 8. TDM Receive Signals

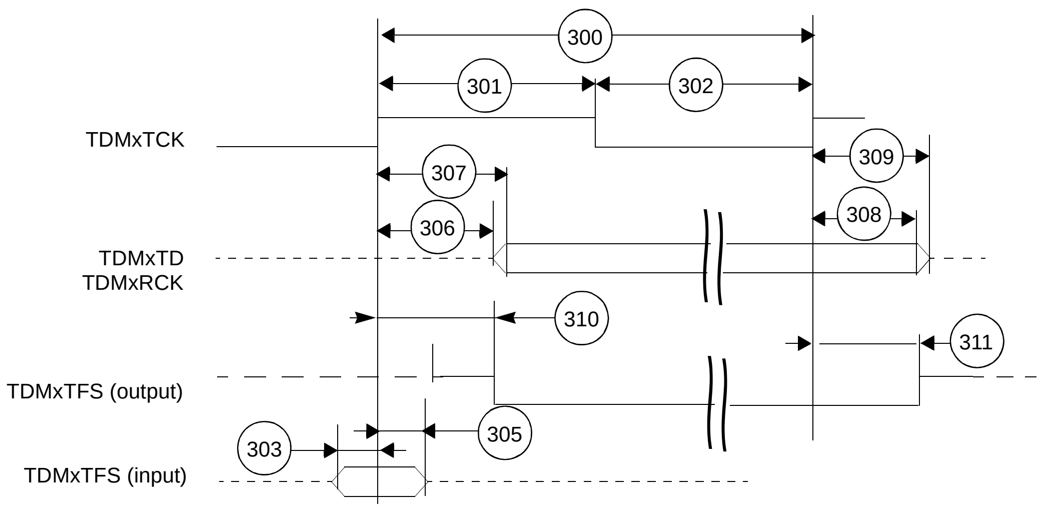

Figure 9. TDM Transmit Signals

Table 22. Host Interface (HDI16) Timing[1, 2] (continued)

No.	Characteristics[3]	Mask Set 1L44X		Mask Set 1M88B		Unit
		Expression	Value	Expression	Value	

Notes:
1. T_{HCLK} = 2/ (Core Clock). At 200 MHz, T_{HCLK} = 10 ns. T_{CORE} = core clock period. At 266 MHz, T_{CORE} = 3.75 ns.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. V_{DD} = 3.3 V ± 0.15 V; T_J = –40°C to +105 °C, C_L = 30 pF for maximum delay timings and C_L = 0 pF for minimum delay timings.
4. The read data strobe is $\overline{\text{HRD}}$/HRD in the dual data strobe mode and $\overline{\text{HDS}}$/HDS in the single data strobe mode.
5. For 64-bit transfers, The “last data register” is the register at address 0x7, which is the last location to be read or written in data transfers. This is RX0/TX0 in the little endian mode (HBE = 0), or RX3/TX3 in the big endian mode (HBE = 1).
6. This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the $\overline{\text{HREQ}}$/HREQ signal.
7. This timing is applicable only if two consecutive reads from one of these registers are executed.
8. The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.
9. The data strobe is host read ($\overline{\text{HRD}}$/HRD) or host write ($\overline{\text{HWR}}$/HWR) in the dual data strobe mode and host data strobe ($\overline{\text{HDS}}$/HDS) in the single data strobe mode.
10. The host request is $\overline{\text{HREQ}}$/HREQ in the single host request mode and $\overline{\text{HRRQ}}$/HRRQ and $\overline{\text{HTRQ}}$/HTRQ in the double host request mode. $\overline{\text{HRRQ}}$/HRRQ is deasserted only when HOTX fifo is empty, $\overline{\text{HTRQ}}$/HTRQ is deasserted only if HORX fifo is full (treat as level Host Request).
11. Compute the value using the expression.
12. For mask set 1M88B, the read and write data strobe minimum deassertion width for non-”last data register” accesses in single and dual data strobe modes is based on timings 57 and 58.

Figure 10 and **Figure 11** show HDI16 read signal timing. **Figure 12** and **Figure 13** show HDI16 write signal timing.

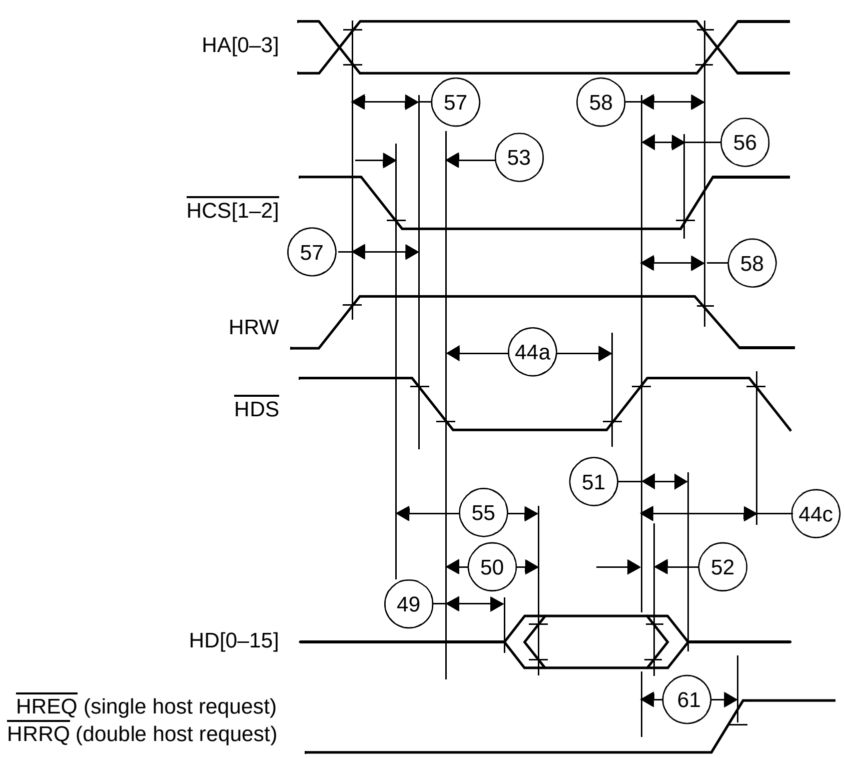

Figure 10. Read Timing Diagram, Single Data Strobe

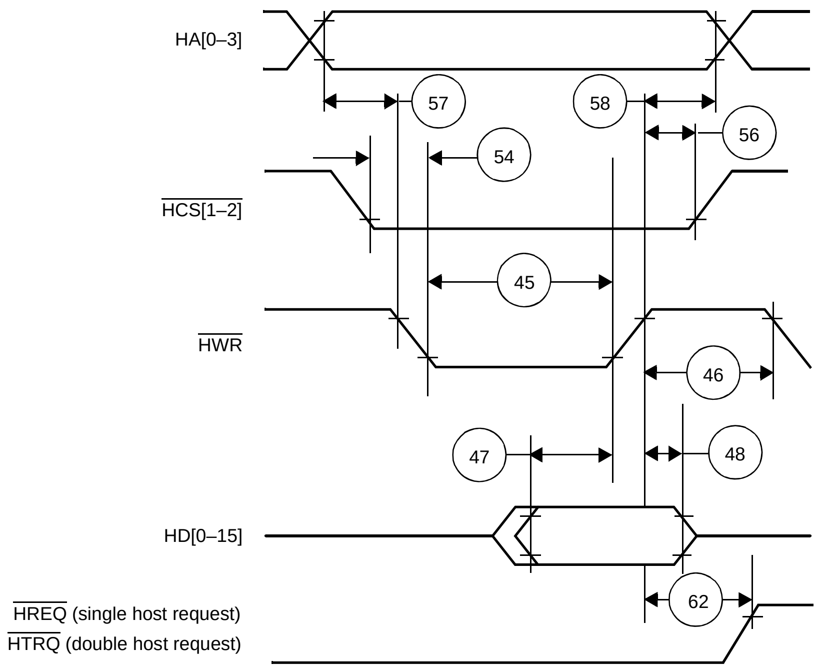

Figure 13. Write Timing Diagram, Double Data Strobe

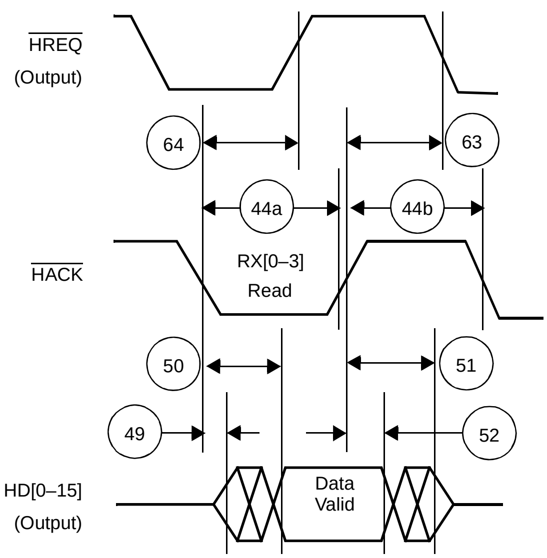

Figure 14. Host DMA Read Timing Diagram, HPCR[OAD] = 0

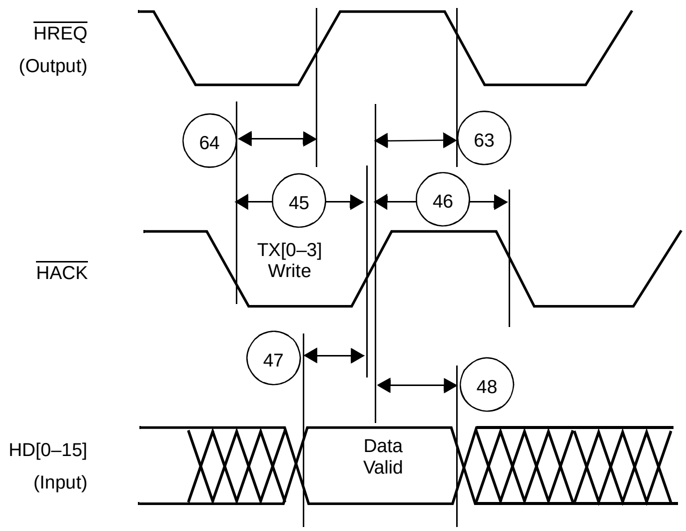

Figure 15. Host DMA Write Timing Diagram, HPCR[OAD] = 0

2.5.7 I2C Timing

Table 23. I2C Timing

No.	Characteristic	Fast		Unit
		Min	Max	
450	SCL clock frequency	0	400	kHz
451	Hold time START condition	(Clock period/2) – 0.3	—	µs
452	SCL low period	(Clock period/2) – 0.3	—	µs
453	SCL high period	(Clock period/2) – 0.1	—	µs
454	Repeated START set-up time (not shown in figure)	$2 \times 1/F_{BCK}$	—	µs
455	Data hold time	0	—	µs
456	Data set-up time	250	—	ns
457	SDA and SCL rise time	—	700	ns
458	SDA and SCL fall time	—	300	ns
459	Set-up time for STOP	(Clock period/2) – 0.7	—	µs
460	Bus free time between STOP and START	(Clock period/2) – 0.3	—	µs
Note:	SDA set-up time is referenced to the rising edge of SCL. SDA hold time is referenced to the falling edge of SCL. Load capacitance on SDA and SCL is 400 pF.			

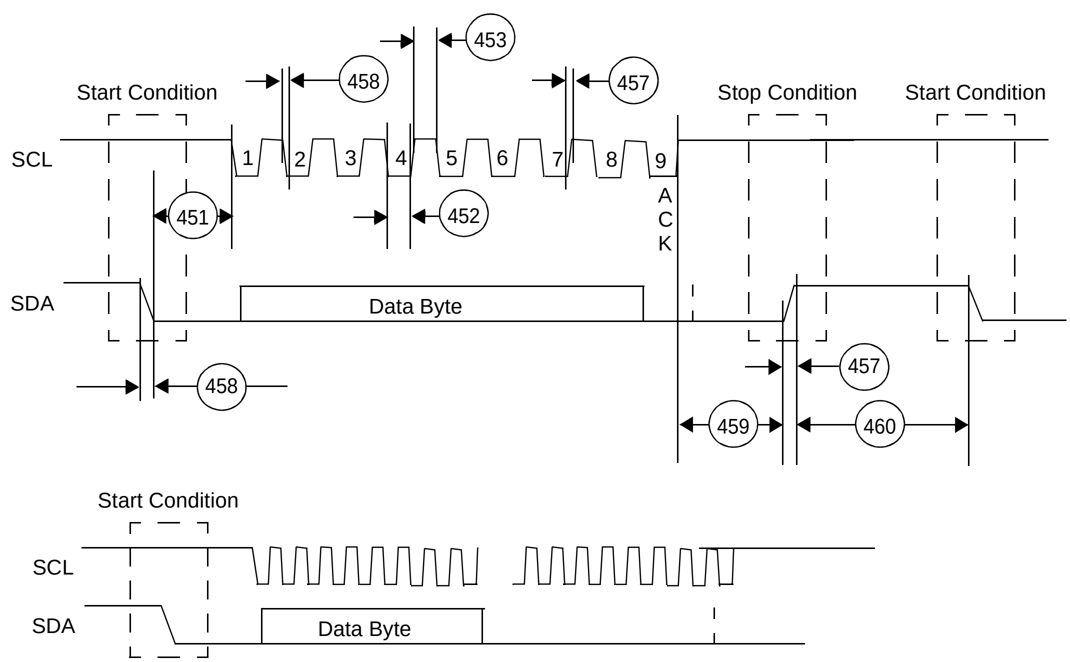

Figure 16. I2C Timing Diagram

2.5.8 UART Timing

Table 24. UART Timing

No.	Characteristics	Expression	Mask Set 1L44X		Mask Set 1M88B		Unit
			Min	Max	Min	Max	
—	Internal bus clock (APBCLK)	$F_{CORE}/2$	—	100	—	133	MHz
—	Internal bus clock period (1/APBCLK)	T_{APBCLK}	10.0	—	7.52	—	ns
400	URXD and UTXD inputs high/low duration	$16 \times T_{APBCLK}$	160.0	—	120.3	—	ns
401	URXD and UTXD inputs rise/fall time		—	5	—	5	ns
402	UTXD output rise/fall time		—	5	—	5	ns

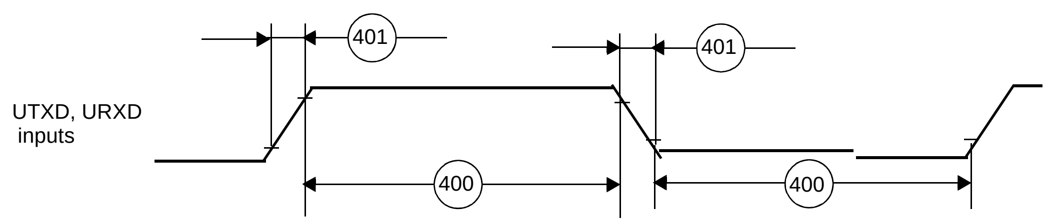

Figure 17. UART Input Timing

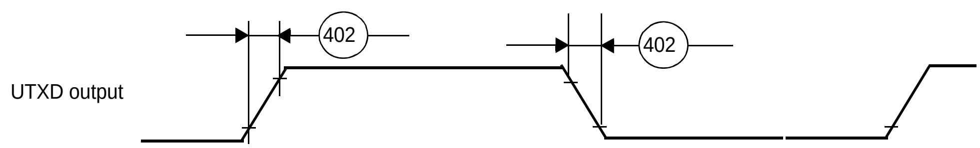

Figure 18. UART Output Timing

2.5.9 EE Timing

Table 25. EE0 Timing

Number	Characteristics	Type	Min
65	EE0 input to the core	Asynchronous	4 core clock periods
66	EE0 output from the core	Synchronous to core clock	1 core clock period

Notes:
1. The core clock is the SC1400 core clock. The ratio between the core clock and CLKOUT is configured during power-on-reset.
2. Configure the direction of the EE pin in the EE_CTRL register (see the *SC1400 Core Reference Manual* for details.
3. Refer to **Table 15** for details on EE pin functionality.

Figure 19 shows the signal behavior of the EE pin.

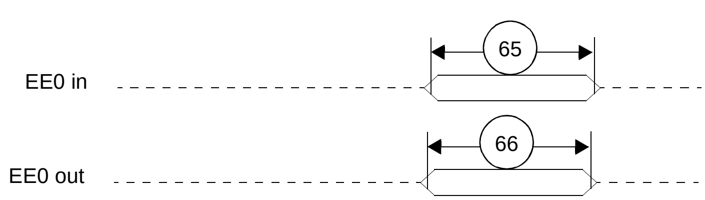

Figure 19. EE Pin Timing

2.5.10 Event Timing

Table 26. EVNT Signal Timing

Number	Characteristics	Type	Min
67	EVNT as input	Asynchronous	1.5 × APBCLK periods
68	EVNT as output	Synchronous to core clock	1 APBCLK period

Notes:
1. Refer to **Table 24** for a definition of the APBCLK period.
2. Direction of the EVNT signal is configured through the GPIO and Event port registers.
3. Refer to the *MSC711x Reference Manual* for details on EVNT pin functionality.

Figure 20 shows the signal behavior of the EVNT pin.

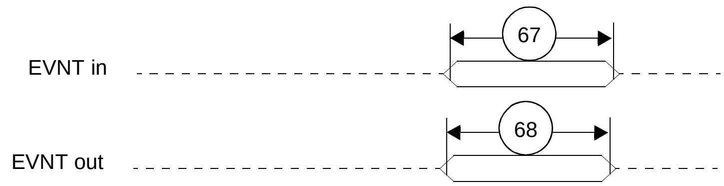

Figure 20. EVNT Pin Timing

2.5.11 GPIO Timing

Table 27. GPIO Signal Timing[1,2,3]

Number	Characteristics	Type	Min
601	GPI[4,5]	Asynchronous	1.5 × APBCLK periods
602	GPO[5]	Synchronous to core clock	1 APBCLK period
603	Port A edge-sensitive interrupt	Asynchronous	1.5 × APBCLK periods
604	Port A level-sensitive interrupt	Asynchronous	3 × APBCLK periods[6]

Notes:
1. Refer to **Table 24** for a definition of the APBCLK period.
2. Direction of the GPIO signal is configured through the GPIO port registers.
3. Refer to *MSC711x Reference Manual* for details on GPIO pin functionality.
4. GPI data is synchronized to the APBCLK internally and the minimum listed is the capability of the hardware to capture data into a register when the GPA_DR is read. The specification is not tested due to the asynchronous nature of the input and dependence on the state of the DSP core. It is guaranteed by design.
5. The input and output signals cannot toggle faster than 50 MHz.
6. Level-sensitive interrupts should be held low until the system determines (via the service routine) that the interrupt is acknowledged.

Figure 21 shows the signal behavior of the GPI/GPO pin.

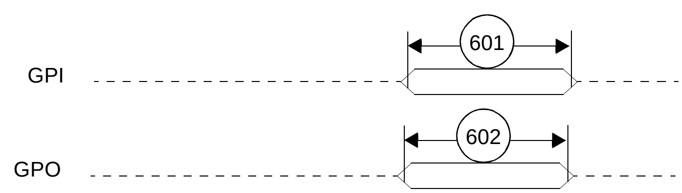

Figure 21. GPI/GPO Pin Timing

3 Hardware Design Considerations

This section described various areas to consider when incorporating the MSC7115 device into a system design.

3.1 Thermal Design Considerations

An estimation of the chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \text{Eqn. 1}$$

where

T_A = ambient temperature near the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$P_D = P_{INT} + P_{I/O}$ = power dissipation in the package (W)

$P_{INT} = I_{DD} \times V_{DD}$ = internal power dissipation (W)

$P_{I/O}$ = power dissipated from device on output pins (W)

The power dissipation values for the MSC7115 are listed in **Table 4**. The ambient temperature for the device is the air temperature in the immediate vicinity that would cool the device. The junction-to-ambient thermal resistances are JEDEC standard values that provide a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. The value that more closely approximates a specific application depends on the power dissipated by other components on the printed circuit board (PCB). The value obtained using a single layer board is appropriate for tightly packed PCB configurations. The value obtained using a board with internal planes is more appropriate for boards with low power dissipation (less than 0.02 W/cm^2 with natural convection) and well separated components. Based on an estimation of junction temperature using this technique, determine whether a more detailed thermal analysis is required. Standard thermal management techniques can be used to maintain the device thermal junction temperature below its maximum. If T_J appears to be too high, either lower the ambient temperature or the power dissipation of the chip.

You can verify the junction temperature by measuring the case temperature using a small diameter thermocouple (40 gauge is recommended) or an infrared temperature sensor on a spot on the device case. Use the following equation to determine T_J:

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \text{Eqn. 2}$$

where

T_T = thermocouple (or infrared) temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

3.2.2.4 Case 4

The power-up sequence is as follows:

1. Turn on the V_{DDIO} (3.3 V) supply first.
2. Turn on the V_{DDC} (1.2 V), V_{DDM} (2.5 V), and V_{REF} (1.25 V) supplies simultaneously (second).

Note: Make sure that the time interval between the ramp-up of V_{DDIO} and V_{DDC} is less than 10 ms.

The power-down sequence is as follows:

1. Turn off the V_{DDC} (1.2 V), V_{REF} (1.25 V), and V_{DDM} (2.5 V) supplies simultaneously (first).
2. Turn of the V_{DDIO} (3.3 V) supply last.

Use the following guidelines:

- Make sure that the time interval between the ramp-up or ramp-down time for V_{DDC} and V_{DDM} is less than 10 ms for power-up and power-down.
- Refer to **Figure 29** for relative timing for Case 4.

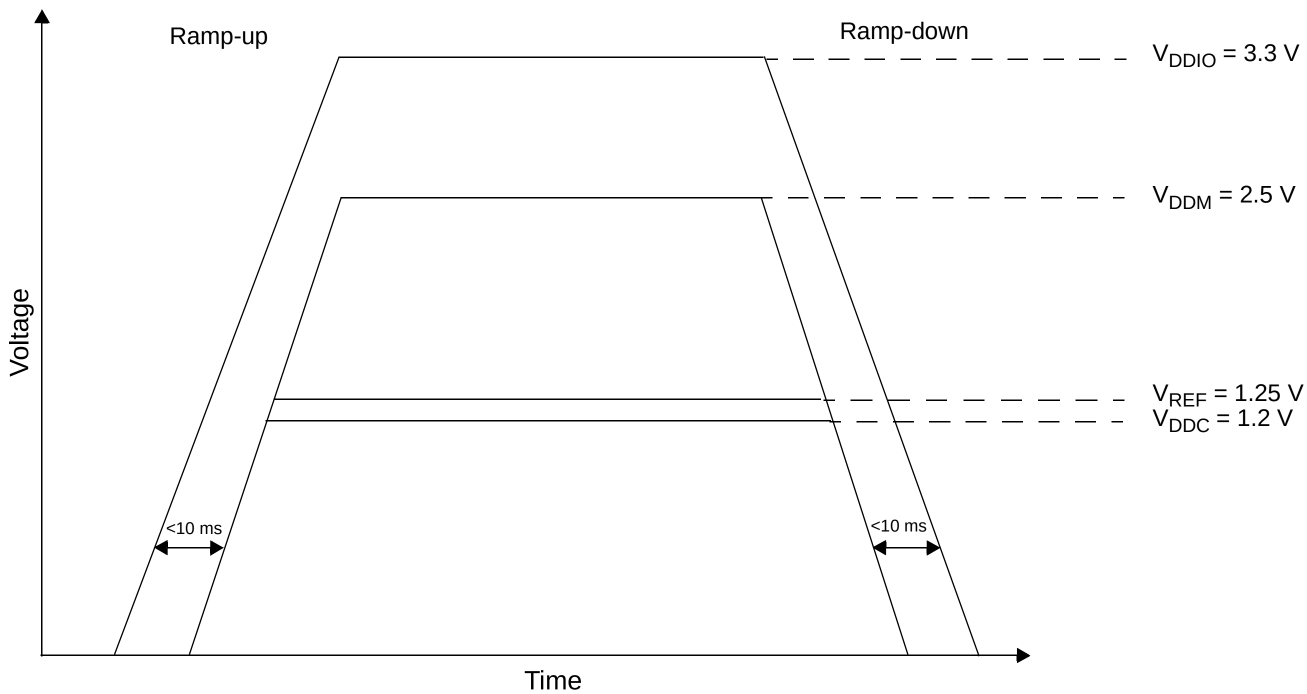

Figure 29. Voltage Sequencing Case 4

3.2.7 Power Supply Design

One of the most common ways to derive power is to use either a simple fixed or adjustable linear regulator. For the system I/O voltage supply, a simple fixed 3.3 V supply can be used. However, a separate adjustable linear regulator supply for the core voltage V_{DDC} should be implemented. For the memory power supply, regulators are available that take care of all DDR power requirements.

Table 30. Recommended Power Supply Ratings

Supply	Symbol	Nominal Voltage	Current Rating
Core	V_{DDC}	1.2 V	1.5 A per device
Memory	V_{DDM}	2.5 V	0.5 A per device
Reference	V_{REF}	1.25 V	10 µA per device
I/O	V_{DDIO}	3.3 V	1.0 A per device

3.3 Estimated Power Usage Calculations

The following equations permit estimated power usage to be calculated for individual design conditions. Overall power is derived by totaling the power used by each of the major subsystems:

$$P_{TOTAL} = P_{CORE} + P_{PERIPHERALS} + P_{DDRIO} + P_{IO} + P_{LEAKAGE} \qquad \text{Eqn. 3}$$

This equation combines dynamic and static power. Dynamic power is determined using the generic equation:

$$C \times V^2 \times F \times 10^{-3}\ mW \qquad \text{Eqn. 4}$$

where,

C = load capacitance in pF

V = peak-to-peak voltage swing in V

F = frequency in MHz

3.3.1 Core Power

Estimation of core power is straightforward. It uses the generic dynamic power equation and assumes that the core load capacitance is 750 pF, core voltage swing is 1.2 V, and the core frequency is 200 MHz or 266 MHz. This yields:

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 200\ MHz \times 10^{-3} = 216\ mW \qquad \text{Eqn. 5}$$

$$P_{CORE} = 750\ pF \times (1.2\ V)^2 \times 266\ MHz \times 10^{-3} = 287\ mW \qquad \text{Eqn. 6}$$

This equation allows for adjustments to voltage and frequency if necessary.

3.3.4 External I/O Power

The estimation of the I/O power is similar to the computation of the peripheral power estimates. The power consumption per signal line is computed assuming a maximum load of 20 pF, a voltage swing of 3.3 V, and a switching frequency of 25 MHz or 33 MHz, which yields:

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 25\ MHz \times 10^{-3} = 5.44\ mW\ per\ I/O\ line \qquad \text{Eqn. 16}$$

$$P_{IO} = 20\ pF \times (3.3\ V)^2 \times 33\ MHz \times 10^{-3} = 7.19\ mW\ per\ I/O\ line \qquad \text{Eqn. 17}$$

Multiply this number by the number of I/O signal lines used in the application design to compute the total I/O power.

Note: The signal loading depends on the board routing. For systems using a single DDR device, the load could be as low as 7 pF.

3.3.5 Leakage Power

The leakage power is for all power supplies combined at a specific temperature. The value is temperature dependent. The observed leakage value at room temperature is 64 mW.

3.3.6 Example Total Power Consumption

Using the examples in this section and assuming four peripherals and 10 I/O lines active, a total power consumption value is estimated as the following:

$$P_{TOTAL}\ (200\ MHz\ core) = 216 + (4 \times 2.88) + 324{,}2 + (10 \times 5.44) + 64 = 670.12\ mW \qquad \text{Eqn. 18}$$

$$P_{TOTAL}\ (266\ MHz\ core) = 287 + (4 \times 3.83) + 326.3 + (10 \times 7.19) + 64 = 764.52\ mW \qquad \text{Eqn. 19}$$

3.4 Reset and Boot

This section describes the recommendations for configuring the MSC7115 at reset and boot.

3.4.1 Reset Circuit

$\overline{\text{HRESET}}$ is a bidirectional signal and, if driven as an input, should be driven with an open collector or open-drain device. For an open-drain output such as $\overline{\text{HRESET}}$, take care when driving many buffers that implement input bus-hold circuitry. The bus-hold currents can cause enough voltage drop across the pull-up resistor to change the logic level to low. Either a smaller value of pull-up or less current loading from the bus-hold drivers overcomes this issue. To avoid exceeding the MSC7115 output current, the pull-up value should not be too small (a 1 KΩ pull-up resistor is used in the MSC711xADS reference design).

3.4.3.2 I2C Boot

When the MSC7115 device is configured to boot from the I2C port, the boot program configures the GPIO pins shared with the I2C pins as I2C pins. The I2C interface is configured as follows:

- I2C in master mode.
- EPROM in slave mode.

For details on the boot procedure, see the "Boot Program" chapter of the *MSC711x Reference Manual*.

3.5 DDR Memory System Guidelines

MSC7115 devices contain a memory controller that provides a glueless interface to external double data rate (DDR) SDRAM memory modules with Class 2 Series Stub Termination Logic 2.5 V (SSTL_2). There are two termination techniques, as shown in Figure 32. Technique B is the most popular termination technique.

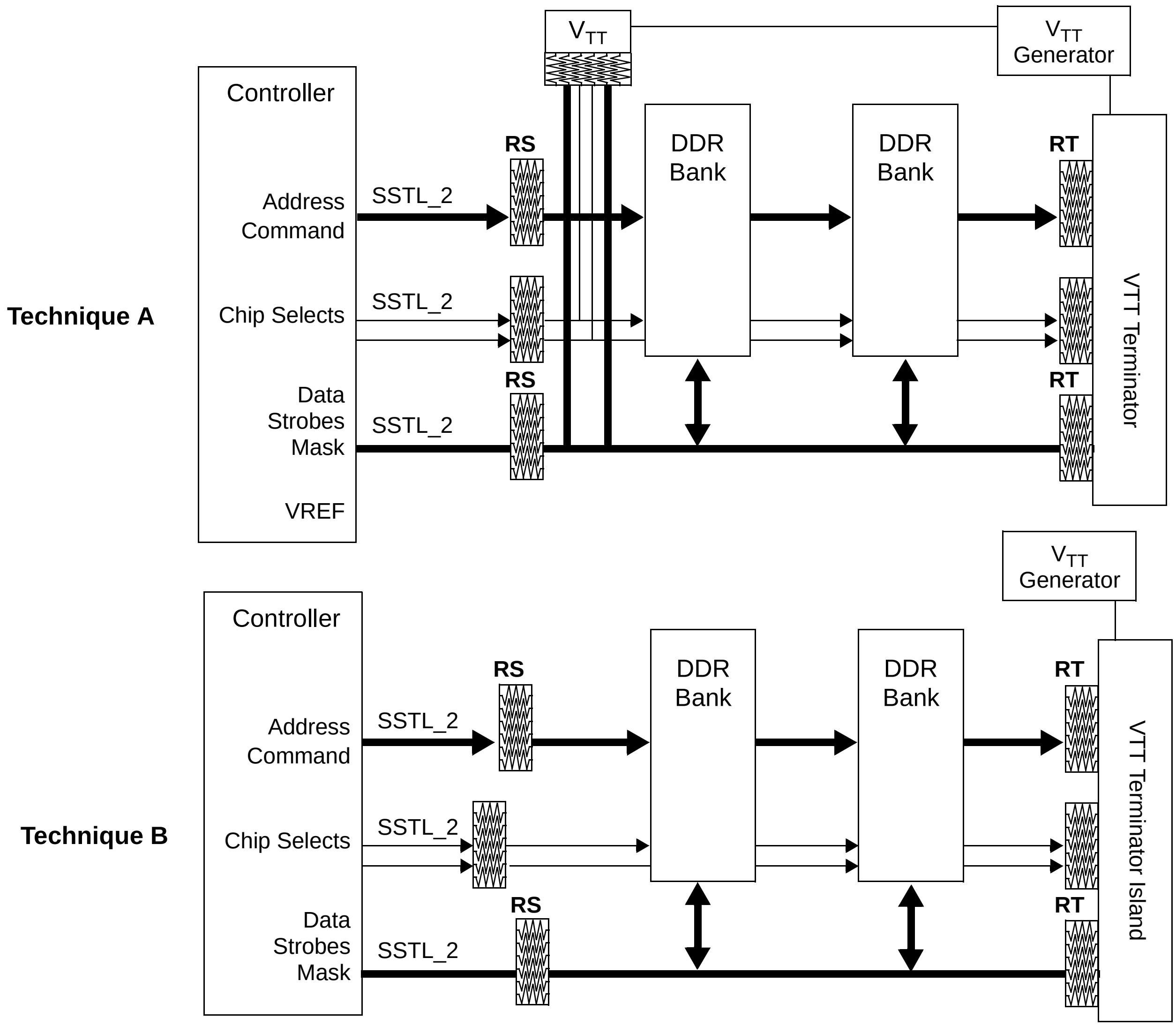

Figure 32. SSTL Termination Techniques

Figure 33 illustrates the power wattage for the resistors. Typical values for the resistors are as follows:

- RS = 22 Ω
- RT = 24 Ω

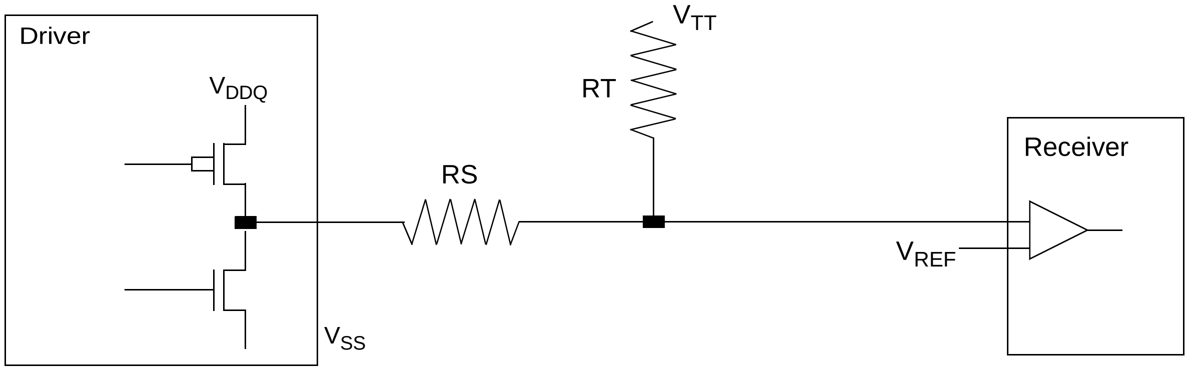

Figure 33. SSTL Power Value

3.5.1 V_{REF} and V_{TT} Design Constraints

V_{TT} and V_{REF} are isolated power supplies at the same voltage, with V_{TT} as a high current power source. This section outlines the voltage supply design needs and goals:

- Minimize the noise on both rails.
- V_{TT} must track variation in the V_{REF} DC offsets. Although they are isolated supplies, one possible solution is to use a single IC to generate both signals.
- Both references should have minimal drift over temperature and source supply.
- It is important to minimize the noise from coupling onto V_{REF} as follows:
  - Isolate V_{REF} and shield it with a ground trace.
  - Use 15–20 mm track.
  - Use 20–30 mm clearance between other traces for isolating.
  - Use the outer layer route when possible.
  - Use distributed decoupling to localize transient currents and return path and decouple with an inductance less than 3 nH.
- Max source/sink transient currents of up to 1.8 A for a 32-bit data bus.
- Use a wide island trace on the outer layer:
  - Place the island at the end of the bus.
  - Decouple both ends of the bus.
  - Use distributed decoupling across the island.
  - Place SSTL termination resistors inside the V_{TT} island and ensure a good, solid connection.
- Place the V_{TT} regulator as closely as possible to the termination island.
  - Reduce inductance and return path.
  - Tie current sense pin at the midpoint of the island.

3.5.2 Decoupling

The DDR decoupling considerations are as follows:

- DDR memory requires significantly more burst current than previous SDRAMs.
- In the worst case, up to 64 drivers may be switching states.
- Pay special attention and decouple discrete ICs per manufacturer guidelines.
- Leverage V_{TT} island topology to minimize the number of capacitors required to supply the burst current needs of the termination rail.
- See the Micron DesignLine publication entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* (`http://download.micron.com/pdf/pubs/designline/3Q00dl1-4.pdf`).

7 Revision History

Table 33 provides a revision history for this data sheet.

Table 33. Document Revision History

Revision	Date	Description
0	Apr 2004	• Initial public release.
1	May 2004	• Added ordering information and new package options.
2	Aug. 2004	• Updated clock parameter values. • Updated DDR timing specifications. • Updated I^2C timing specifications.
3	Sep. 2004	• Updated **Figures 1-2** and **1-2** to correct HDSP and DBREQ. • Corrected EE0 port reference. • Updated ball location for HDSP.
4	Jan. 2005	• Added signal HA3. • Updated absolute maximum ratings, DDR DRAM capacitance specifications, clock parameters, reset timing, and TDM timing. • Added note for timing reference for I^2C interface. • Expanded GPIO timing information. • Corrected pin T20 and K20 signal designation. • Corrected signal names to GPAO15 and $\overline{\text{IRQ2}}$. • Expanded design guidelines in Chapter 4.
5	Mar. 2005	• Updated features list. • Updated power specifications. • Changed CLKIN frequency range. • Added clock configuration information. • Updated JTAG timings.
6	Apr. 2005	• Added recommended power supply ratings and updated equations to estimate power consumption.
7	Oct. 2005	• Updated core and total power consumption examples.
8	Dec. 2005	• Added information about signals GPIOA16, GPIOA17, GPIOA27, GPIOA28, and GPIOA29 to signal description and pinout location lists.
9	Nov. 2006	• Updated Reference Manual reference to MSC711x Reference Manual. • Updated arrows in Host DMA Writing Timing figure. • Updated boot overview.
10	Aug. 2007	• Updated to new data sheet format. Reorganized and renumbered sections, figures, and tables. • Added a note to clarify the definition of TCK timing 700 in new **Table 31**. • The power-up and power-down sequences have been expanded to five possible design scenarios/cases. These cases replace the previously recommended power-up/power-down sequence recommendations. The section has been clarified by adding subsection headings.
11	Apr 2008	• Change the PLL filter resistor from 20 Ω to 2 Ω in **Section 3.2.5**.

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