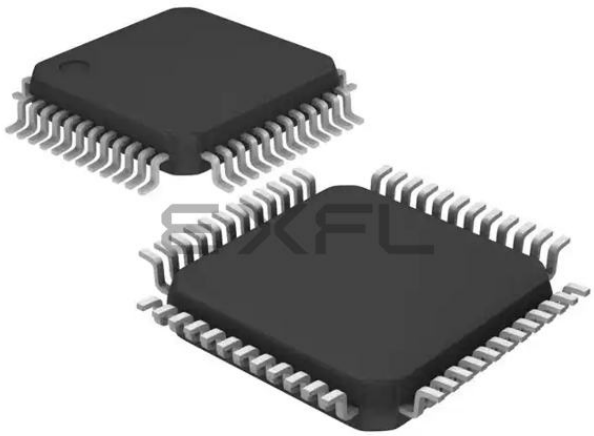

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Details	
Product Status	Obsolete
Applications	USB Host/Slave Controller
Core Processor	-
Program Memory Type	-
Controller Series	USB-Hosts
RAM Size	256 x 8
Interface	USB
Number of I/O	8
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 65°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/sl811hst-axc

Functional Overview

Data Port, Microprocessor Interface

The SL811HS[1] microprocessor interface provides an 8-bit bidirectional data path along with appropriate control lines to interface to external processors or controllers. Programmed I/O or memory mapped I/O designs are supported through the 8-bit interface, chip select, read and write input strobes, and a single address line, A0.

Access to memory and control register space is a simple two step process, requiring an address Write with A0 = ’0’, followed by a register/memory Read or Write cycle with address line A0 = ’1’.

In addition, a DMA bidirectional interface in slave mode [2] is available with handshake signals such as nDRQ, nDACK, nWR, nRD, nCS and INTRQ.

The SL811HS WRITE or READ operation terminates when either nWR or nCS goes inactive. For devices interfacing to the SL811HS that deactivate the Chip Select nCS before the Write nWR, the data hold timing must be measured from the nCS and is the same value as specified. Therefore, both Intel® - and Motorola-type CPUs work easily with the SL811HS without any external glue logic requirements.

DMA Controller (slave mode only)

In applications that require transfers of large amounts of data such as scanner interfaces, the SL811HS provides a DMA interface. This interface supports DMA READ or WRITE transfers to the SL811HS internal RAM buffer, it is done through the microprocessor data bus via two control lines (nDRQ - Data Request and nDACK - Data Acknowledge), along with the nWR line and controls the data flow into the SL811HS. The SL811HS has a count register that allows selection of programmable block sizes for DMA transfer. The control signals, both nDRQ and nDACK, are designed for compatibility with standard DMA interfaces.

Interrupt Controller

The SL811HS interrupt controller provides a single output signal (INTRQ) that is activated by a number of programmable events that may occur as result of USB activity. Control and status registers are provided to allow the user to select single or multiple events, which generate an interrupt (assert INTRQ) and let the user view interrupt status. The interrupts are cleared by writing to the Interrupt Status Register.

Notes
1. Errata: In a noisy environment, the SL811HS has the potential to occasionally miss a packet. Please refer to Errata on page 33 for details on errata and suggested work-around.
2. Errata: The DMA interface can be unreliable in slave mode. Please refer to Errata on page 33 for details on errata and suggested work-around.

PLL Clock Generator

Either a 12 MHz [4] or a 48 MHz external crystal is used with the SL811HS [5]. Two pins, X1 and X2, are provided to connect a low cost crystal circuit to the device as shown in Figure 2 and Figure 2. Use an external clock source if available in the application instead of the crystal circuit by connecting the source directly to the X1 input pin. When a clock is used, the X2 pin is not connected.

When the CM pin is tied to a logic 0, the internal PLL is bypassed so the clock source must meet the timing requirements specified by the USB specification.

Figure 2. Full Speed 48 MHz Crystal Circuit

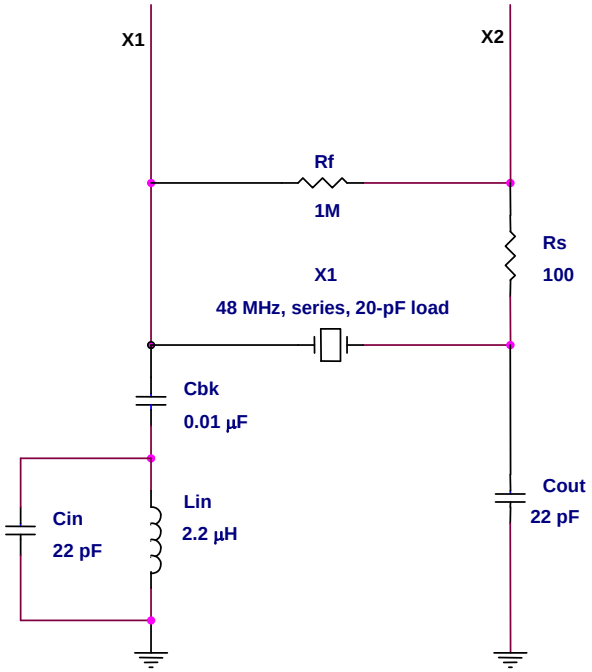
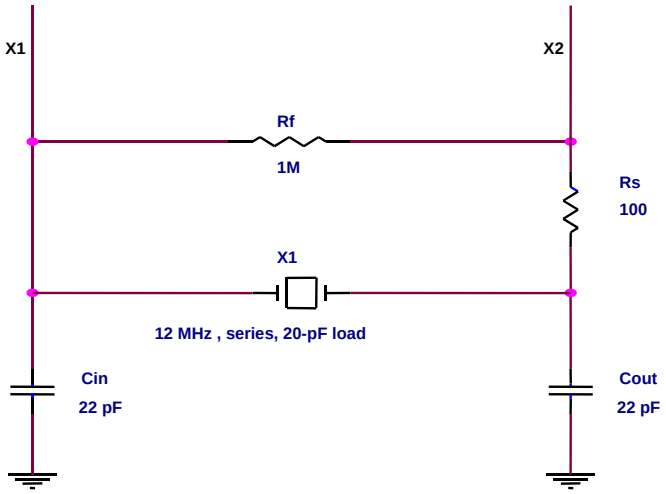


Figure 3. Optional 12 MHz Crystal Circuit



Typical Crystal Requirements

The following are examples of 'typical requirements.' Note that these specifications are generally found as standard crystal values and are less expensive than custom values. If crystals are used in series circuits, load capacitance is not applicable. Load capacitance of parallel circuits is a requirement. 48 MHz third overtone crystals require the Cin/Lin filter to guarantee 48 MHz operation.

12 MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0 °C to 70 °C
Frequency:	12 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	60Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	fundamental

48 MHz Crystals:

Frequency Tolerance:	±100 ppm or better
Operating Temperature Range:	0 °C to 70 °C
Frequency:	48 MHz
Frequency Drift over Temperature:	± 50 ppm
ESR (Series Resistance):	40 Ω
Load Capacitance:	10 pF min.
Shunt Capacitance:	7 pF max.
Drive Level:	0.1–0.5 mW
Operating Mode:	third overtone

Notes

4. Errata: The internal PLL is very sensitive. The PLL causes any high frequency noise on the VDD pins to result in clock jitter. Please refer to Errata on page 33 for details on errata and suggested work-around.
5. CM (Clock Multiply) pin of the SL811HS must be tied to GND when 48 MHz crystal circuit or 48 MHz clock source is used.

USB Transceiver

The SL811HS has a built in transceiver that meets USB Specification 1.1. The transceiver is capable of transmitting and receiving serial data at USB full speed [6] (12 Mbits) and low speed [7] (1.5 Mbits). The driver portion of the transceiver is differential while the receiver section is comprised of a differential receiver and two single-ended receivers. Internally, the transceiver interfaces to the Serial Interface Engine (SIE) logic. Externally, the transceiver connects to the physical layer of the USB.

SL811HS Registers

Operation and control of the SL811HS is managed through internal registers. When operating in Master/Host mode, the first 16 address locations are defined as register space. In Slave/Peripheral mode, the first 64 bytes are defined as register space. The register definitions vary greatly between each mode of operation and are defined separately in this document (section Table 1 describes Host register definitions, while Table 19 on page 15 describes Slave register definitions). Access to the registers are through the microprocessor interface similar to normal RAM accesses (see "Bus Interface Timing Requirements" on page 26) and provide control and status information for USB transactions.

Any write to control register 0FH enables the SL811HS full features bit. This is an internal bit of the SL811HS that enables additional features.

Table 1 shows the memory map and register mapping of the SL811HS in master/host mode.

Table 1. SL811HS Master (Host) Mode Registers

Register Name SL811HS	SL811HS (hex) Address
USB-A Host Control Register	00h
USB-A Host Base Address	01h
USB-A Host Base Length	02h
USB-A Host PID, Device Endpoint (Write)/USB Status (Read)	03h
USB-A Host Device Address (Write)/Transfer Count (Read)	04h
Control Register 1	05h
Interrupt Enable Register	06h
Reserved Register	Reserved
USB-B Host Control Register	08h
USB-B Host Base Address	09h
USB-B Host Base Length	0Ah
USB-B Host PID, Device Endpoint (Write)/USB Status (Read)	0Bh
USB-B Host Device Address (Write)/Transfer Count (Read)	0Ch
Status Register	0Dh
SOF Counter LOW (Write)/HW Revision Register (Read)	0Eh
SOF Counter HIGH and Control Register 2	0Fh
Memory Buffer	10H-FFh

The registers in the SL811HS are divided into two major groups. The first group is referred to as USB Control registers. These registers enable and provide status for control of USB transactions and data flow. The second group of registers provides control and status for all other operations.

Register Values on Power-up and Reset

The following registers initialize to zero on power-up and reset:

- USB-A/USB-B Host Control Register [00H, 08H] bit 0 only
- Control Register 1 [05H]
- USB Address Register [07H]
- Current Data Set/Hardware Revision/SOF Counter LOW Register [0EH]

All other register's power-up and reset in an unknown state and firmware for initialization.

Notes

6. Errata: The SYNC to SOF bit (bit 5) of the USB Host Control Registers [00H, 08H], is only designed for full-speed support. In full-speed mode, this bit should only be used when the software cannot fit a packet within the remaining 1 ms frame. Please refer to Errata on page 33 for details on errata and suggested work-around.
7. Errata: Some hubs that send SE0s upstream during the EOF1 time frame may cause the SL811HS to stop sending SOFs. This problem occurs when operating with low-speed devices attached downstream of such a hub. Please refer to Errata on page 33 for details on errata and suggested work-around.

USB-A/USB-B Host Base Length [Address = 02h, 0Ah].

Table 5. USB-A / USB-B Host Base Length Definition [Address 02h, 0Ah]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HBL7	HBL6	HBL5	HBL4	HBL3	HBL2	HBL1	HBL0

The USB A/B Host Base Length register contains the maximum packet size transferred between the SL811HS and a slave USB peripheral. Essentially, this designates the largest packet size that is transferred by the SL811HS. Base Length designates the size of data packet sent or received. For example, in full speed BULK mode, the maximum packet length is 64 bytes. In ISO mode, the maximum packet length is 1023 bytes since the SL811HS only has an 8-bit length; the maximum packet size for the ISO mode using the SL811HS is 255 – 16 bytes (register space). When the Host Base length register is set to zero, a Zero-Length packet is transmitted.

USB-A/USB-B USB Packet Status (Read) and Host PID, Device Endpoint (Write) [Address = 03h, 0Bh]. This register has two modes dependent on whether it is read or written. When read, this register provides packet status and contains information relative to the last packet that has been received or transmitted. This register is not valid for reading until after the Done interrupt occurs, which causes the register to update.

Table 6. USB-A/USB-B USB Packet Status Register Definition when READ [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STALL	NAK	Overflow	Setup	Sequence	Time-out	Error	ACK

Bit Position	Bit Name	Function
7	STALL	Slave device returned a STALL.
6	NAK	Slave device returned a NAK.
5	Overflow	Overflow condition - maximum length exceeded during receives. For underflow, see USB-A/USB-B Host Transfer Count Register (Read), USB Address (Write) [Address = 04h, 0Ch].
4	Setup	This bit is not applicable for Host operation since a SETUP packet is generated by the host.
3	Sequence	Sequence bit. ’0’ if DATA0, ’1’ if DATA1.
2	Time-out	Timeout occurred. A timeout is defined as 18-bit times without a device response (in full speed).
1	Error	Error detected in transmission. This includes CRC5, CRC16, and PID errors.
0	ACK	Transmission Acknowledge.

When written, this register provides the PID and Endpoint information to the USB SIE engine used in the next transaction. All 16 Endpoints can be addressed by the SL811HS.

Table 7. USB-A / USB-B Host PID and Device Endpoint Register when WRITTEN [Address 03h, 0Bh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PID3	PID2	PID1	PID0	EP3	EP2	EP1	EP0

PID[3:0]: 4-bit PID Field (See following table), EP[3:0]: 4-bit Endpoint Value in Binary.

PID TYPE	D7-D4
SETUP	1101 (D Hex)
IN	1001 (9 Hex)
OUT	0001 (1 Hex)
SOF	0101 (5 Hex)
PREAMBLE	1100 (C Hex)
NAK	1010 (A Hex)
STALL	1110 (E Hex)
DATA0	0011 (3 Hex)
DATA1	1011 (B Hex)

Control Register 1 [Address = 05h]. The Control Register 1 enables/disables USB transfer operation with control bits defined as follows.

Table 11. Control Register 1 [Address 05h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Suspend	USB Speed	J-K state force	USB Engine Reset	Reserved	Reserved	SOF ena/dis

Bit Position	Bit Name	Function
7	Reserved	‘0’
6	Suspend	’1’ = enable, ’0’ = disable.
5	USB Speed	’0’ setup for full speed, ’1’ setup low speed.
4	J-K state force	See Table 12.
3	USB Engine Reset	USB Engine reset = ’1’. Normal set ’0’. When a device is detected, the first thing that to do is to send it a USB Reset to force it into its default address of zero. The USB 2.0 specification states that for a root hub a device must be reset for a minimum of 50 mS.
2	Reserved	Some existing firmware examples set bit 2, but it is not necessary.
1	Reserved	‘0’
0	SOF ena/dis	’1’ = enable auto Hardware SOF generation; ’0’ = disable. In the SL811HS, bit 0 is used to enable hardware SOF autogeneration. The generation of SOFs continues when set to ‘0’, but SOF tokens are not output to USB.

At power-up this register is cleared to all zeros.

Low-power Modes [Bit 6 Control Register, Address 05h]

When bit 6 (Suspend) is set to ’1’, the power of the transmit transceiver is turned off, the internal RAM is in suspend mode, and the internal clocks are disabled.

Note Any activity on the USB bus (that is, K-State, etc.) resumes normal operation. To resume normal operation from the CPU side, a Data Write cycle (i.e., A0 set HIGH for a Data Write cycle) is done. This is a special case and not a normal direct write where the address is first written and then the data. To resume normal operation from the CPU side, you must do a Data Write cycle only.

Low Speed/Full Speed Modes [Bit 5 Control Register 1, Address 05h]

The SL811HS is designed to communicate with either full- or low speed devices. At power-up bit 5 is LOW, i.e., for full speed.

There are two cases when communicating with a low speed device. When a low speed device is connected directly to the SL811HS, bit 5 of Register 05h is set to ’1’ and bit 6 of register 0Fh, Polarity Swap, is set to ’1’ in order to change the polarity of D+ and D–. When a low speed device is connected via a HUB to SL811HS, bit 5 of Register 05h is set to ’0’ and bit 6 of register 0Fh is set to ’0’ in order to keep the polarity of D+ and D– for full speed. In addition, make sure that bit 7 of USB-A/USB-B Host Control registers [00h, 08h] is set to ’1’ for preamble generation.

J-K Programming States [Bits 4 and 3 of Control Register 1, Address 05h]

The J-K force state control and USB Engine Reset bits are used to generate a USB reset condition. Forcing K-state is used for Peripheral device remote wake up, resume, and other modes. These two bits are set to zero on power-up.

Table 12. Bus Force States

USB Engine Reset	J-K Force State	Function
0	0	Normal operating mode
0	1	Force USB Reset, D+ and D– are set LOW (SE0)
1	0	Force J-State, D+ set HIGH, D– set LOW[8]
1	1	Force K-State, D– set HIGH, D+ set LOW[9]

Notes
8. Force K-State for low speed.
9. Force J-State for low speed.

USB Reset Sequence

After a device is detected, write 08h to the Control register (05h) to initiate the USB reset, then wait for the USB reset time (root hub should be 50 ms) and additionally some types of devices such as a Forced J-state. Lastly, set the Control register (05h) back to 0h. After the reset is complete, the auto-SOF generation is enabled.

SOF Packet Generation

The SL811HS automatically computes the frame number and CRC5 by hardware. No CRC or SOF generation is required by external firmware for the SL811HS, although it can be done by sending an SOF PID in the Host PID, Device Endpoint register.

To enable SOF generation, assuming host mode is configured:

1. Set up the SOF interval in registers 0x0F and 0x0E.
2. Enable the SOF hardware generation in this register by setting bit 0 = ‘1’.
3. Set the Arm bit in the USB-A Host Control register.

Interrupt Enable Register [Address = 06h]. The SL811HS provides an Interrupt Request Output, which is activated for a number of conditions. The Interrupt Enable register allows the user to select conditions that result in an interrupt that is issued to an external CPU through the INTRQ pin. A separate Interrupt Status register reflects the reason for the interrupt. Enabling or disabling these interrupts does not have an effect on whether or not the corresponding bit in the Interrupt Status register is set or cleared; it only determines if the interrupt is routed to the INTRQ pin. The Interrupt Status register is normally used in conjunction with the Interrupt Enable register and can be polled in order to determine the conditions that initiated the interrupt (See the description for the Interrupt Status Register). When a bit is set to ’1’ the corresponding interrupt is enabled. So when the enabled interrupt occurs, the INTRQ pin is asserted. The INTRQ pin is a level interrupt, meaning it is not deasserted until all enabled interrupts are cleared.

Table 13. Interrupt Enable Register [Address 06h]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Device Detect/Resume	Inserted/ Removed	SOF Timer	Reserved	Reserved	USB-B DONE	USB-A DONE

Bit Position	Bit Name	Function
7	Reserved	‘0’
6	Device Detect/Resume	Enable Device Detect/Resume Interrupt. When bit 6 of register 05h (Control Register 1) is equal to ’1’, bit 6 of this register enables the Resume Detect Interrupt. Otherwise, this bit is used to enable Device Detection status as defined in the Interrupt Status register bit definitions.
5	Inserted/Removed	Enable Slave Insert/Remove Detection is used to enable/disable the device inserted/removed interrupt.
4	SOF Timer	1 = Enable Interrupt for SOF Timer. This is typically at 1 mS intervals, although the timing is determined by the SOF Counter high/low registers. To use this bit function, bit 0 of register 05h must be enabled and the SOF counter registers 0E hand 0Fh must be initialized.
3	Reserved	‘0’
2	Reserved	‘0’
1	USB-B DONE	USB-B Done Interrupt (see USB-A Done interrupt).
0	USB-A DONE	USB-A Done Interrupt. The Done interrupt is triggered by one of the events that are logged in the USB Packet Status register. The Done interrupt causes the Packet Status register to update.

USB Address Register, Reserved, Address [Address = 07h]. This register is reserved for the device USB Address in Slave operation. It should not be written by the user in host mode.

Registers 08h-0Ch Host-B registers. Registers 08h-0Ch have the same definition as registers 00h-04h except they apply to Host-B instead of Host-A.

Interrupt Status Register, Address [Address = 0Dh]. The Interrupt Status register is a READ/WRITE register providing interrupt status. Interrupts are cleared by writing to this register. To clear a specific interrupt, the register is written with corresponding bit set to '1'.

Table 14. Interrupt Status Register [Address 0Dh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D+	Device Detect/Resume	Insert/Remove	SOF timer	Reserved	Reserved	USB-B	USB-A

Bit Position	Bit Name	Function
7	D+	Value of the Data+ pin. Bit 7 provides continuous USB Data+ line status. Once it is determined that a device is inserted (as described below) with bits 5 and 6, bit 7 is used to detect if the inserted device is low speed (0) or full speed (1).
6	Device Detect/Resume	Device Detect/Resume Interrupt. Bit 6 is shared between Device Detection status and Resume Detection interrupt. When bit-6 of register 05h is set to one, this bit is the Resume detection Interrupt bit. Otherwise, this bit is used to indicate the presence of a device, '1' = device 'Not present' and '0' = device 'Present.' In this mode, check this bit along with bit 5 to determine whether a device has been inserted or removed.
5	Insert/Remove	Device Insert/Remove Detection. Bit 5 is provided to support USB cable insertion/removal for the SL811HS in host mode. This bit is set when a transition from SE0 to IDLE (device inserted) or from IDLE to SE0 (device removed) occurs on the bus.
4	SOF timer	'1' = Interrupt on SOF Timer.
3	Reserved	'0'
2	Reserved	'0'
1	USB-B	USB-B Done Interrupt. (See description in Interrupt Enable Register [address 06h].)
0	USB-A	USB-A Done Interrupt. (See description in Interrupt Enable Register [address 06h].)

Current Data Set Register/Hardware Revision/SOF Counter LOW [Address = 0Eh]. This register has two modes. Read from this register indicates the current SL811HS silicon revision.

Table 15. Hardware Revision when Read [Address 0Eh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hardware Revision				Reserved			

Bit Position	Bit Name	Function
7-4	Hardware Revision	SL811HS rev1.2 Read = 1H; SL811HS rev1.5 Read = 2.
3-2	Reserved	Read is zero.
1-0	Reserved	Reserved for slave.

Writing to this register sets up auto generation of SOF to all connected peripherals. This counter is based on the 12 MHz clock and is not dependent on the crystal frequency. To set up a 1 ms timer interval, the software must set up both SOF counter registers to the proper values.

Table 16. SOF Counter LOW Address when Written [Address 0Eh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOF7	SOF6	SOF5	SOF4	SOF3	SOF2	SOF1	SOF0

Example: To set up SOF for 1 ms interval, SOF counter register 0Eh should be set to E0h.

SOF Counter High/Control Register 2 [Address = 0Fh]. When read, this register returns the value of the SOF counter divided by 64. The software must use this register to determine the available bandwidth in the current frame before initiating any USB transfer. In this way, the user is able to avoid babble conditions on the USB. For example, to determine the available bandwidth left in a frame do the following.

Maximum number of clock ticks in 1 ms time frame is 12000 (1 count per 12 MHz clock period, or approximately 84 ns.) The value read back in Register 0FH is the (count × 64) × 84 ns = time remaining in current frame. USB bit time = one 12 MHz period.

Value of register 0FH	Available bit times left are between
BBH	12000 bits to 11968 (187 × 64) bits
BAH	11968 bits to 11904 (186 × 64) bits

Note: Any write to the 0Fh register clears the internal frame counter. Write register 0Fh at least once after power-up. The internal frame counter is incremented after every SOF timer tick. The internal frame counter is an 11-bit counter, which is used to track the frame number. The frame number is incremented after each timer tick. Its contents are transmitted to the slave every millisecond in a SOF packet.

Table 17. SOF High Counter when Read [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C13	C12	C11	C10	C9	C8	C7	C6

When writing to this register the bits definition are defined as follows.

Table 18. Control Register 2 when Written [Address 0Fh]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SL811HS Master/Slave selection	SL811HS D+/D– Data Polarity Swap	SOF High Counter Register					

Bit Position	Bit Name	Function
7	SL811HS Master/Slave selection	Master = 1, Slave = 0.
6	SL811HS D+/D– Data Polarity Swap	’1’ = change polarity (low speed) ’0’ = no change of polarity (full speed).
5-0	SOF High Counter Register	Write a value or read it back to SOF High Counter Register.

Note Any write to Control register 0Fh enables the SL811HS full features bit. This is an internal bit of the SL811HS that enables additional features.

The USB-B register set is used when SL811HS full feature bit is enabled.

Example. To set up host to generate 1 ms SOF time:

The register 0Fh contains the upper 6 bits of the SOF timer. Register 0Eh contains the lower 8 bits of the SOF timer. The timer is based on an internal 12 MHz clock and uses a counter, which counts down to zero from an initial value. To set the timer for 1 ms time, the register 0Eh is loaded with value E0h and register 0Fh (bits 0–5) is loaded with 2Eh. To start the timer, bit 0 of register 05h (Control Register 1) is set to ’1’, which enables hardware SOF generation. To load both HIGH and LOW registers with the proper values, the user must follow this sequence:

1. Write E0h to register 0Eh. This sets the lower byte of the SOF counter
2. Write AEh to register 0Fh, AEh configures the part for full speed (no change of polarity) Host with bits 5–0 = 2Eh for upper portion of SOF counter.
3. Enable bit 0 in register 05h. This enables hardware generation of SOF.
4. Set the ARM bit at address 00h. This starts the SOF generation.

Endpoint Control Registers

Endpoint n Control Register [Address a = (EP# * 10h), b = (EP# * 10h)+8]. Each endpoint set has a Control register defined as follows:

Table 22. Endpoint Control Register [Address EP0a/b:00h/08h, EP1a/b:10h/18h, EP2a/b:20h/28h, EP3a/b:30h/38h]

7	6	5	4	3	2	1	0
Reserved	Sequence	Send STALL	ISO	Next Data Set	Direction	Enable	Arm

Bit Position	Bit Name	Function
7	Reserved	
6	Sequence	Sequence bit. '0' if DATA0, '1' if DATA1.
5	Send STALL	When set to ‘1’, sends Stall in response to next request on this endpoint.
4	ISO	When set to '1', allows Isochronous mode for this endpoint.
3	Next Data Set	'0' if next data set is ‘A’, '1' if next data set is 'B'.
2	Direction	When Direction = '1', transmit to Host (IN). When Direction = '0', receive from Host (OUT).
1	Enable	When Enable = '1', allows transfers for this endpoint. When set to ‘0’, USB transactions are ignored. If Enable = '1' and Arm = '0', the endpoint returns NAKs to USB transmissions.
0	Arm	Allows enabled transfers when set =’1’. Clears to '0' when transfer is complete.

Endpoint Base Address [Address a = (EP# * 10h)+1, b = (EP# * 10h)+9]]. Pointer to memory buffer location for USB reads and writes.

Table 23. Endpoint Base Address Reg [Address; EP0a/b:01h/09h, EP1a/b:11h/19h, EP2a/b:21h/29h, EP3a/b:31h/39h]

7	6	5	4	3	2	1	0
EPxADD7	EPxADD6	EPxADD5	EPxADD4	EPxADD3	EPxADD2	EPxADD1	EPxADD0

Endpoint Base Length [Address a = (EP# * 10h)+2, b = (EP# * 10h)+A]. The Endpoint Base Length is the maximum packet size for IN/OUT transfers with the host. Essentially, this designates the largest packet size that is received by the SL811HS with an OUT transfer, or it designates the size of the data packet sent to the host for IN transfers.

Table 24. Endpoint Base Length Reg [Address EP0a/b:02h/0Ah, EP1a/b:12h/1Ah, EP2a/b:22h/2Ah, EP3a/b:32h/3Ah]

7	6	5	4	3	2	1	0
EPxLEN7	EPxLEN6	EPxLEN5	EPxLEN4	EPxLEN3	EPxLEN2	EPxLEN1	EPxLEN0

Bit Position	Bit Name	Function
7	SL811HS Master/Slave selection	Master = ‘1’ Slave = ‘0’
6	SL811HS D+/D– Data Polarity Swap	’1’ = change polarity (low speed) ’0’ = no change of polarity (full speed)
5-0	Reserved	NA

SOF Low Register, Address [15h]. Read only register contains the 7 low order bits of Frame Number in positions: bit 7:1. Bit 0 is undefined. Register is updated when a SOF packet is received. Do not write to this register.

SOF High Register, Address [16h]. Read only register contains the 4 low order bits of Frame Number in positions: bit 7:4. Bits 3:0 are undefined and should be masked when read by the user. This register is updated when a SOF packet is received. The user should not write to this register.

DMA Total Count Low Register, Address [35h]. The DMA Total Count Low register contains the low order 8 bits of DMA count. DMA total count is the total number of bytes to be transferred between a peripheral to the SL811HS. The count may sometimes require up to 16 bits, therefore the count is represented in two registers: Total Count Low and Total Count High. EP3 is only supported with DMA operation.

DMA Total Count High Register, Address [36h]. The DMA Total Count High register contains the high order 8 bits of DMA count. When written, this register enables DMA if the DMA Enable bit is set in Control Register 1. The user should always write Low Count register first, followed by a write to High Count register, even if high count is 00h.

Electrical Specifications

Absolute Maximum Ratings

This section lists the absolute maximum ratings of the SL811HS. Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested..

Description	Condition
Storage Temperature	–40°C to 125°C
Voltage on any pin with respect to ground	–0.3 V to 6.0 V
Power Supply Voltage (V_{DD})	4.0 V
Power Supply Voltage (V_{DD1})	4.0 V
Lead Temperature (10 seconds)	180°C

Recommended Operating Condition

Parameter	Min	Typical	Max
Power Supply Voltage, VDD	3.0 V	3.3 V	3.45 V
Power Supply Voltage, VDD1	3.0 V		3.45 V
Operating Temperature	0°C		65°C

Crystal Requirements, (X1, X2)	Min	Typical	Max
Operating Temperature Range	0°C		65°C
Parallel Resonant Frequency		48 MHz	
Frequency Drift over Temperature			±50 ppm
Accuracy of Adjustment			±30 ppm
Series Resistance			100 Ohms
Shunt Capacitance	3 pF		6 pF
Load Capacitance		20 pF	
Drive Level	20 μW		5 mW
Mode of Vibration Third Overtone[15]			

External Clock Input Characteristics (X1)

Parameter	Min	Typical	Max
Clock Input Voltage at X1 (X2 Open)	1.5 V		
Clock Frequency[16]		48 MHz	

Notes
15. Fundamental mode for 12 MHz Crystal.
16. The SL811HS can use a 12 MHz Clock Source.

DC Characteristics

Parameter	Description	Min	Typ	Max
V_{IL}	Input Voltage LOW	–0.3 V		0.8 V
V_{IH}	Input Voltage HIGH (5 V Tolerant I/O)	2.0 V		6.0 V
V_{OL}	Output Voltage LOW (I_{OL} = 4 mA)			0.4 V
V_{OH}	Output Voltage HIGH (I_{OH} = –4 mA)	2.4 V		
I_{OH}	Output Current HIGH	4 mA		
I_{OL}	Output Current LOW	4 mA		
I_{LL}	Input Leakage			±1 µA
C_{IN}	Input Capacitance			10 pF
I_{CC}[17]	Supply Current (V_{DD}) inc USB at FS		21 mA	25 mA
I_{CCsus1}[18]	Supply Current (V_{DD}) Suspend w/Clk & Pll Enb		4.2 mA	5 mA
I_{CCsus2}[19]	Supply Current (V_{DD}) Suspend no Clk & Pll Dis		50 µA	60 µA
I_{USB}	Supply Current (V_{DD1})			10 mA
I_{USBSUS}	Transceiver Supply Current in Suspend			10 µA

USB Host Transceiver Characteristics

Parameter	Description	Min	Typ[20]	Max
V_{IHYS}	Differential Input Sensitivity (Data+, Data–)	0.2 V		200 mV
V_{USBIH}	USB Input Voltage HIGH Driven	2.0 V		
V_{USBIL}	USB Input Voltage LOW	0.8 V		
V_{USBOH}	USB Output Voltage HIGH	2.0 V		
V_{USBOL}	USB Output Voltage LOW	0.0 V		0.3 V
Z_{USBH}[21]	Output Impedance HIGH STATE	36 Ohms		42 Ohms
Z_{USBL}[21]	Output Impedance LOW STATE	36 Ohms		42 Ohms
I_{USB}	Transceiver Supply p-p Current (3.3 V)			10 mA at FS

Every V_{DD} pin, including USB V_{DD}, must have a decoupling capacitor to ensure clean V_{DD} (free of high frequency noise) at the chip input point (pin) itself.

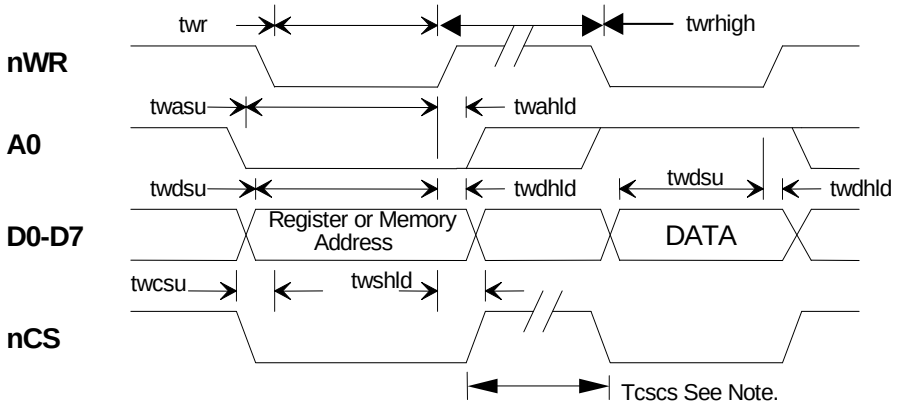
The best way to do this is to connect a ceramic capacitor (0.1 µF, 6 V) between the pin itself and a good ground. Keep capacitor leads as short as possible. Use surface mount capacitors with the shortest traces possible (the use of a ground plane is strongly recommended).

This product was tested as compliant to the USB-IF specification under the test identification number (TID) of 40000689 and is listed on the USB-IF's integrators list.

Notes
17. I_{CC} measurement includes USB Transceiver current (I_{USB}) operating at full speed.
18. I_{CCsus1} measured with 12 MHz Clock Input and Internal PLL enabled. Suspend set –(USB transceiver and internal Clocking disabled).
19. I_{CCsus2} measured with external Clock, PLL disabled, and Suspend set. For absolute minimum current consumption, ensure that all inputs to the device are at static logic level.
20. All typical values are V_{DD} = 3.3 V and T_{AMB}= 25°C.
21. Z_{USBX} impedance values includes an external resistor of 24 Ohms ± 1% (SL811HS revision 1.2 requires external resistor values of 33 Ohms ±1%).

Bus Interface Timing Requirements

I/O Write Cycle

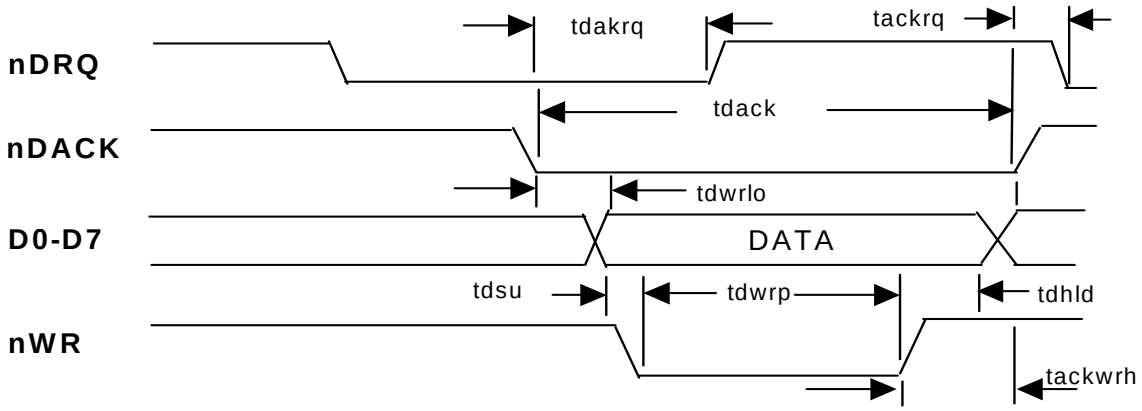


I/O Write Cycle to Register or Memory Buffer

Parameter	Description	Min	Typ	Max
t_{WR}	Write pulse width	85 ns		
t_{WCSU}	Chip select set-up to nWR LOW	0 ns		
t_{WSHLD}	Chip select hold time After nWR HIGH	0 ns		
t_{WASU}	A0 address set-up time	85 ns		
t_{WAHLD}	A0 address hold time	10 ns		
t_{WDSU}	Data to Write HIGH set-up time	85 ns		
t_{WDHLD}	Data hold time after Write HIGH	5 ns		
t_{CSCS}	nCS inactive to nCS* asserted	85 ns		
t_{WRHIGH}	NWR HIGH	85 ns		

Note nCS an be held LOW for multiple Write cycles provided nWR is cycled. Write Cycle Time for Auto Inc Mode Writes is 170 ns minimum.

DMA Write Cycle

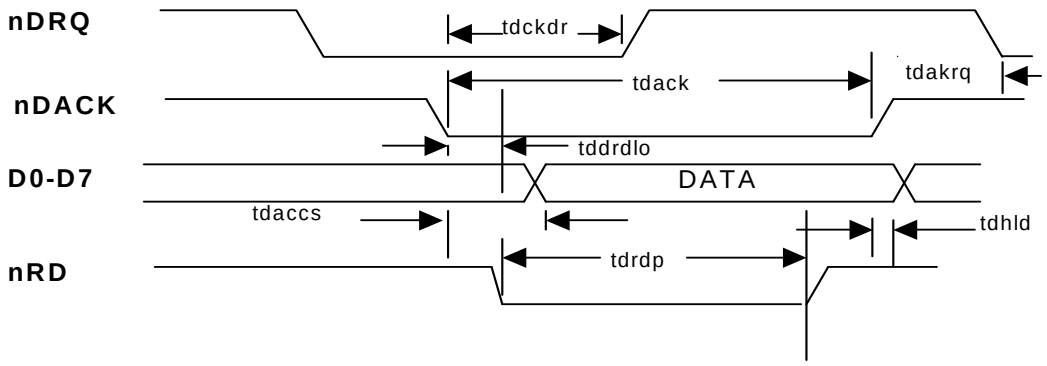


DMA Write Cycle

Parameter	Description	Min	Typ	Max
tdack	nDACK low	80 ns		
tdwrlo	nDACK to nWR low delay	5 ns		
tdakrq	nDACK low to nDRQ high delay	5 ns		
tdwrp	nWR pulse width	65 ns		
tdhld	Data hold after nWR high	5 ns		
tdsu	Data set-up to nWR strobe low	60 ns		
tackrq	NDACK high to nDRQ low	5 ns		
tackwrh	NDACK high to nDRQ low	5 ns		
twrcycle	DMA Write Cycle Time	150 ns		

Note nWR must go low after nDACK goes low in order for nDRQ to clear. If this sequence is not implemented as requested, the next nDRQ is not inserted.

DMA Read Cycle

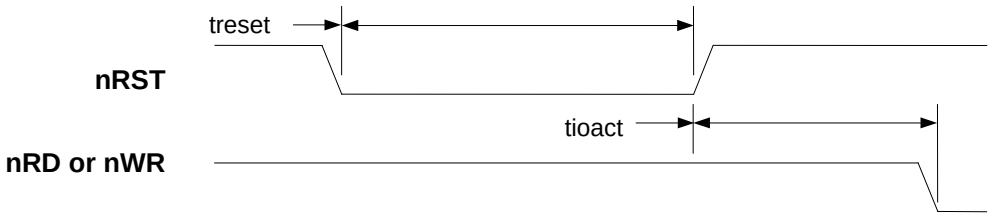


SL811 DMA Read Cycle Timing

Parameter	Description	Min	Typ	Max
tdack	nDACK low	100 ns		
tddrdlo	nDACK to nRD low delay	0 ns		
tdckdr	nDACK low to nDRQ high delay	5 ns		
tdrdp	nRD pulse width	90 ns		
tdhld	Date hold after nDACK high	5 ns		
tddaccs	Data access from nDACK low	85 ns		
tdrdack	nRD high to nDACK high	0 ns		
tdakrq	nDRQ low after nDACK high	5 ns		
trdcycle	DMA Read Cycle Time	150 ns		

Note Data is held until nDACK goes high regardless of state of nREAD.

Reset Timing

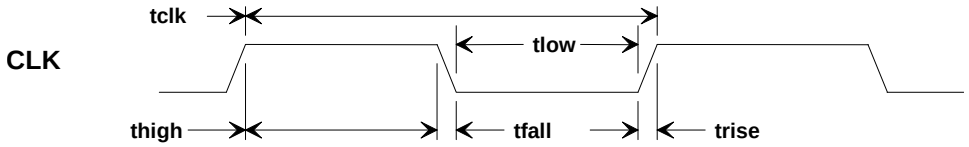


Reset Timing

Parameter	Description	Min	Typ	Max
t_{RESET}	nRst Pulse width	16 clocks		
t_{IOACT}	nRst HIGH to nRD or nWR active	16 clocks		

Note Clock is 48 MHz nominal.

Clock Timing Specifications



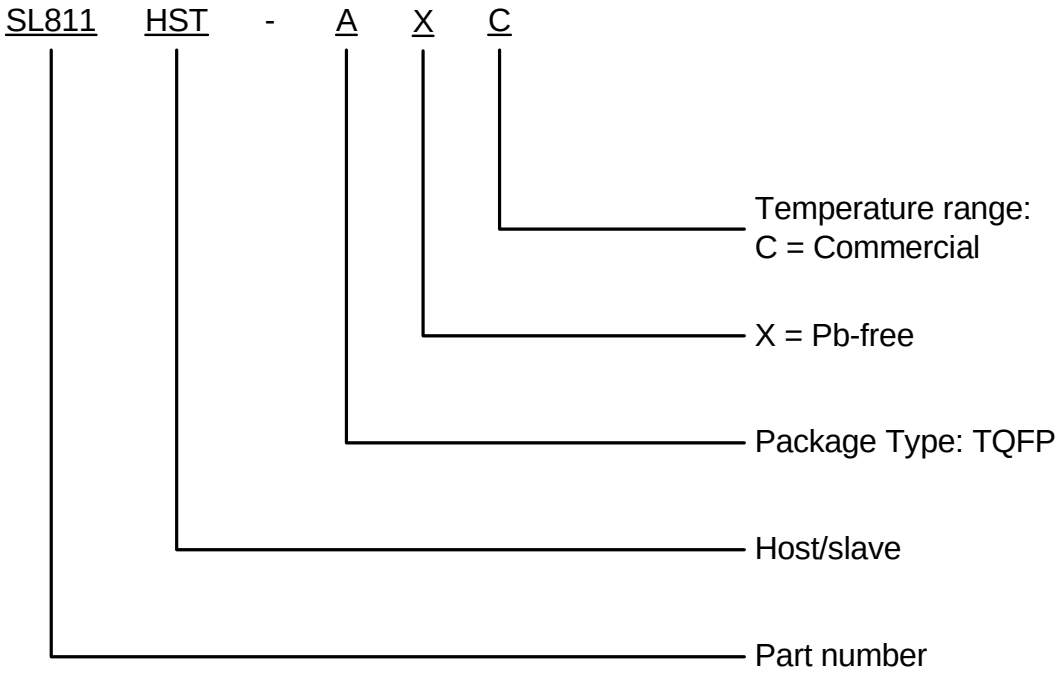
Clock Timing

Parameter	Description	Min	Typ	Max
t_{CLK}	Clock Period (48 MHz)	20.0 ns	20.8 ns	
t_{HIGH}	Clock HIGH Time	9 ns		11 ns
t_{LOW}	Clock LOW Time	9 ns		11 ns
t_{RISE}	Clock Rise Time			5.0 ns
t_{FALL}	Clock Fall Time			5.0 ns
	Clock Duty Cycle	45%		55%

Ordering Information

Part Number	Package Type	
SL811HST-AXC	48-pin Pb-free	–

Ordering Code Definitions



Acronyms

Table 35. Acronyms Used in this Document

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CRC	Cyclical Redundancy Check
DMA	Direct Memory Access
DPLL	Dynamic Phase Locked Loop
I/O	Input Output
PCMCIA	Personal Computer Memory Card International Association
RAM	Random Access Memory
SIE	Serial Interface Engine
SOF	Start of Frame
SRAM	Static Random Access Memory
USB	Universal Serial Bus

Document Conventions

Units of Measure

Table 36. Units of Measure

Symbol	Unit of Measure
mA	milliampere
Mbps	megabits per second
MHz	megahertz
mV	millivolt
mW	milliwatt
ns	nanosecond
ppm	parts per million
pF	picofarad
V	volt
VDC	volts (direct current)

4. Peripheral Mode: Unreliable DMA interface

■ **Problem Definition**

The DMA interface can be unreliable in slave mode.

■ **Parameters Affected**

DMA transfers to or from the SL811HS internal RAM.

■ **Trigger Condition(S)**

Use of the DMA interface to move data to or from SL811HS internal RAM.

■ **Scope of Impact**

When performing DMA writes, data may get corrupted. This problem has only been seen for DMA write operations, but can also occur for read operations as well.

■ **Workaround**

Use the standard Data Port interface instead of the DMA interface for writing to or reading from the SL811HS RAM space. The DMA interface is not a recommended interface for the SL811HS due to this issue.

■ **Fix Status**

Use workaround.

5. Peripheral Mode: SL811HS can miss packets in a noisy environment

■ **Problem Definition**

In a noisy environment, the SL811HS has the potential to occasionally miss a packet. Occasionally missed packets are anticipated and dealt with in USB 2.0 Specification Section 10.2.6, where the following applies "It is recommended that the error count not be incremented when there is an error due to host specific reasons (buffer underrun or overrun), and that whenever a transaction does not encounter a transmission error, the error count be reset to zero." In other words if an individual packet is missed and the next packet is processed properly, the recommendation is that the error counter be reset to ‘0’. When drivers are written with this in mind, they can avoid issues that cause the transfer to be retired due to three errors in a transaction.

■ **Parameters Affected**

Error count.

■ **Trigger Condition(S)**

Electrically noisy environments.

■ **Scope of Impact**

If the SL811HS is used in an electrically noisy environment that may corrupt three requests within that transaction, the transaction will be retired by the host.

■ **Workaround**

1) The workaround for this issue is to write the driver according to the guidelines specified in section 10.2.6 of the USB 2.0 Specification, to prevent the driver from retrying the transfer.

2) Board layout is the major reason for electrical noise that can aggravate this issue. When doing layout for the USB chip, use guidelines provided in a Cypress application note titled, *High-speed USB PCB Layout Recommendations* found on the Cypress web site.

■ **Fix Status**

Use workaround.

6. Host/Peripheral Mode: Auto-increment feature results in corrupt data

■ **Problem Definition**

The SL811HS has a feature called auto-increment used to read or write blocks of the data buffer. This feature is used to speed up the time it takes to write blocks of data because an address location write is not required between data writes or reads. In some cases, the auto-increment feature can intermittently fail, causing the RAM location to be corrupted or the read buffer to provide incorrect data to the system processor. This type of error is very infrequent.

■ **Parameters Affected**

Any RAM location where auto-increment feature is used to access data. This includes both register and buffer space.

■ **Trigger Condition(S)**

Use of the auto-increment feature.

■ **Scope of Impact**

When using the auto-increment feature for writes or reads, it is possible for the data to become corrupt. The following table demonstrates a typical error when it occurs. The error condition is shown in red.

If an error occurs during writes using auto-increment, an address location can be written with the value of the previous address; each subsequent write will also be incorrect until the end of the block write. In the following example, note that the value of 0x01 from address 0x11 is incorrectly written to address 0x12 instead of the expected value of 0x02. After this error, the write to each subsequent address is also incorrectly written with the value that was intended to be in the previous address location.

If an error occurs during a read using auto-increment, a single location can be incorrectly read as the previous addresses value. If the data is read again, it will show that the data in RAM is correct.

Auto-increment error during a write								
Address	**0x10**	**0x11**	**0x12**	**0x13**	**0x14**	**.....**	**0x1E**	**0x1F**
Data intended to be written to RAM	0x00	0x01	0x02	0x03	0x04	.....	0x0E	0x0F
Data actually written to RAM	0x00	0x01	**0x01**	**0x02**	**0x03**	**.....**	**0x0D**	**0x0E**
Auto-increment error during a read								
Address	**0x10**	**0x11**	**0x12**	**0x13**	**0x14**	**.....**	**0x1E**	**0x1F**
Data actually in RAM	0x00	0x01	0x02	0x03	0x04	.....	0x0E	0x0F
Data read back from RAM	0x00	0x01	**0x01**	0x03	0x04	.....	0x0E	0x0F

■ **Workaround**

The easiest way to work around this issue is to not use the auto-increment feature. This affects performance because the address must be written prior to each write or read.

■ **Fix Status**

Use workaround.

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