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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	100K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 36x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/ft1166192f80hlaaxp

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  - One General Purpose Timer Array Module (GPTA) with a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One 16-channel Analog-to-Digital Converter unit (ADC) with selectable 8-bit, 10-bit, or 12-bit, supporting 32 input channels
  - One 2-channel Fast Analog-to-Digital Converter unit (FADC) with concatenated comb filters for hardware data reduction: supporting 10-bit resolution, with minimum conversion time of 262.5ns
- 32 analog input lines for ADC and FADC
- 81 digital general purpose I/O lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 and 2 (CPU, PCP, DMA)
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full Industrial and Multi-Market temperature range: -40° to +85°C
- PG-LQFP-176-2 package

1) Not applicable to TC1165

2.3 Pin Configuration

Figure 2-3 shows the TC1165/TC1166 pin configuration.

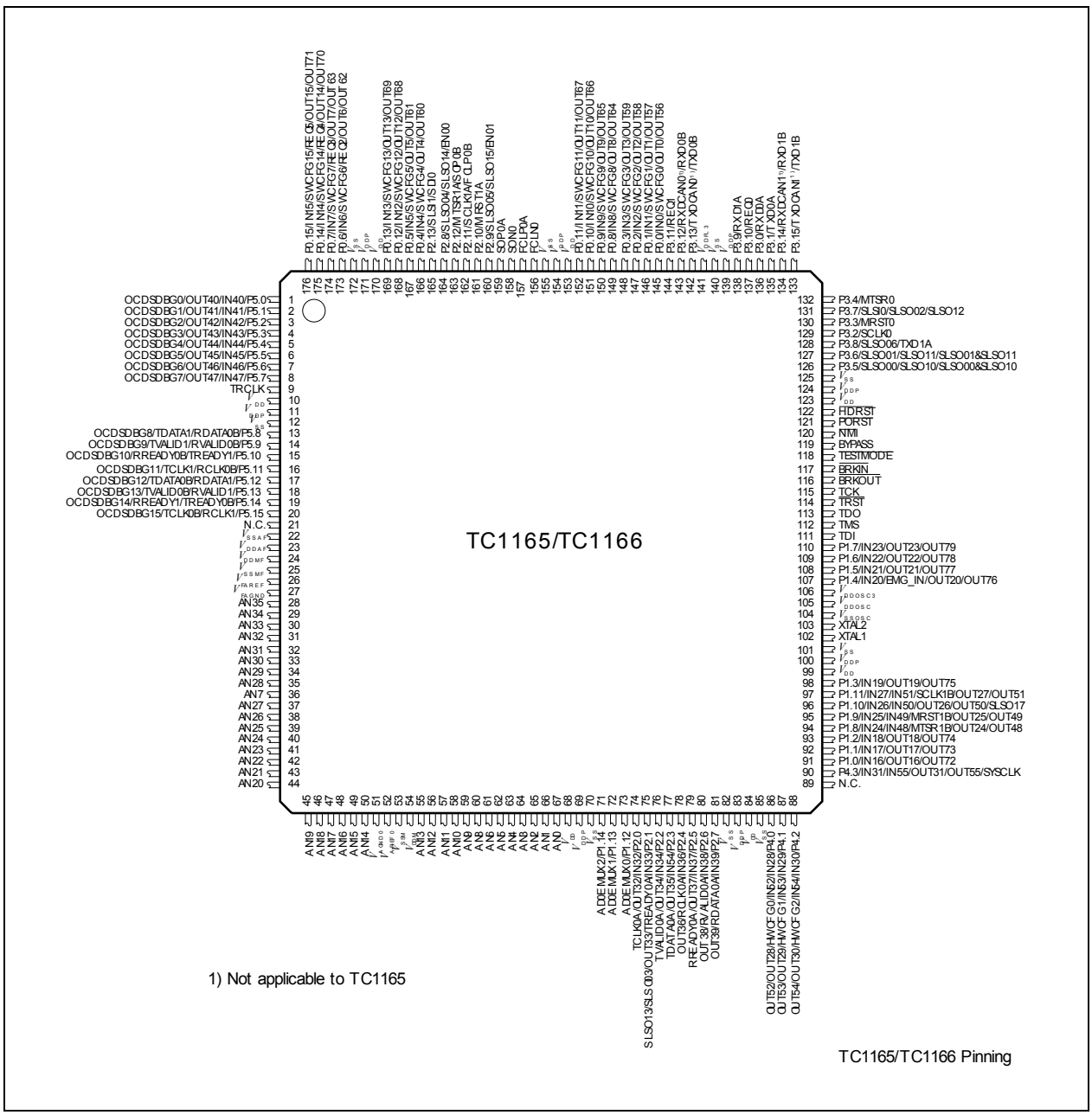

Figure 2-3 TC1165/TC1166 Pinning for PG-LQFP-176-2 Package

2.4 Pad Driver and Input Classes Overview

The TC1165/TC1166 provides different types and classes of input and output lines. For understanding of the abbreviations in **Table 2-1** starting at the next page, **Table 4-1** gives an overview on the pad type and class types.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
N.C.	21, 89	–	–	–	**Not Connected** These pins are reserved for future extension and must not be connected externally.
Power Supplies					
V_{DDM}	54	–	–	–	**ADC Analog Part Power Supply (3.3 V)**
V_{SSM}	53	–	–	–	**ADC Analog Part Ground for V_{DDM}**
V_{DDMF}	24	–	–	–	**FADC Analog Part Power Supply (3.3 V)**
V_{SSMF}	25	–	–	–	**FADC Analog Part Ground for V_{DDMF}**
V_{DDAF}	23	–	–	–	**FADC Analog Part Logic Power Supply (1.5 V)**
V_{SSAF}	22	–	–	–	**FADC Analog Part Logic Ground for V_{DDAF}**
V_{AREF0}	52	–	–	–	**ADC Reference Voltage**
V_{AGND0}	51	–	–	–	**ADC Reference Ground**
V_{FAREF}	26	–	–	–	**FADC Reference Voltage**
V_{FAGND}	27	–	–	–	**FADC Reference Ground**
V_{DDOSC}	105	–	–	–	**Main Oscillator and PLL Power Supply (1.5 V)**
V_{DDOSC3}	106	–	–	–	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC}	104	–	–	–	**Main Oscillator and PLL Ground**
V_{DDFL3}	141	–	–	–	**Power Supply for Flash (3.3 V)**
V_{DD}	10, 68, 84, 99, 123, 153, 170	–	–	–	**Core Power Supply (1.5 V)**

3.3.3 Contents of the Segments

This section summarizes the contents of the segments.

Segments 0-7

These segments are reserved segments in the TC1165/TC1166.

Segment 8

From the SPB point of view (PCP, DMA and Cerberus), this memory segment allows accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

From the CPU point of view (PMI and DMI), this memory segment allows cached accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

Segment 9

This memory segment is reserved in the TC1165/TC1166.

Segment 10

From the SPB point of view (PCP, DMA and Cerberus), this memory segment allows accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

From the CPU point of view (PMI and DMI), this memory segment allows non-cached accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

Segment 11

This memory segment is reserved in the TC1165/TC1166.

Segment 12

From the SPB point of view (PCP, DMA, and Cerberus), this memory segment is reserved in the TC1165/TC1166.

From the CPU point of view (PMI and DMI), this memory segment allows cached accesses to the PMU memory, OVRAM.

Segment 13

From the SPB point of view (PCP, DMA and Cerberus), this memory segment is reserved in the TC1165/TC1166.

From the CPU point of view (PMI and DMI), this memory segment allows non-cached accesses to the PMI scratch-pad RAM, read access to the boot ROM and test ROM (BROM and TROM) and the DMI memories (LDRAM).

Table 3-4 SPB Address Map of Segment 15 (cont'd)

Unit		Address Range	Size	Access Type	
				Read	Write
Program Memory Unit (PMU)		$F800\ 0500_H$ - $F800\ 05FF_H$	256 byte	access	access
Reserved		$F800\ 0600_H$ - $F800\ 0FFF_H$	–	LMBBE & SPBBE	LMBBE
Flash Register		$F800\ 1000_H$ - $F800\ 23FF_H$	5 Kbyte	access	access
Reserved		$F800\ 2400_H$ - $F801\ 00FF_H$	–	LMBBE & SPBBE	LMBBE
Reserved		$F801\ 0100_H$ - $F801\ 01FF_H$	–	LMBBE & SPBBE	LMBBE
Reserved		$F801\ 0200_H$ - $F87F\ F9FF_H$	–	LMBBE & SPBBE	LMBBE
Reserved		$F87F\ FA00_H$ - $F87F\ FAFF_H$	–	LMBBE & SPBBE	LMBBE
Reserved		$F87F\ FB00_H$ - $F87F\ FBFF_H$	–	LMBBE & SPBBE	LMBBE
CPU	DMI Registers	$F87F\ FC00_H$ - $F87F\ FCFF_H$	256 byte	access	access
	PMI Registers	$F87F\ FD00_H$ - $F87F\ FDFF_H$	256 byte	access	access
Local Memory Bus Control Unit (LBCU)		$F87F\ FE00_H$ - $F87F\ FEFF_H$	256 byte	access	access
LFI Bridge		$F87F\ FF00_H$ - $F87F\ FFFF_H$	256 byte	access	access
Reserved		$F880\ 0000_H$ - $FFFF\ FFFF_H$	–	LMBBE & SPBBE	LMBBE

1) For TC1165, read and write accesses to this address range will not generate any traps.

Table 3-5 LMB Address Map (cont'd)

Segment	Address Range	Size	Description	Action	
				Read	Write
10[3]	A000 0000$_H$ - A017 FFFF$_H$	1.5 Mbyte	Program Flash (PFLASH)	access	access[2]
	A017 8000$_H$ - A07F FFFF$_H$	6.5 Mbyte	Reserved	LMBBET	LMBBET
	A080 0000$_H$ - AFDF FFFF$_H$	246 Mbyte	Reserved	LMBBET	LMBBET
	AFE0 0000$_H$ - AFE0 3FFF$_H$	16 Kbyte	Data Flash (DFLASH) Bank 0	access	access[2]
	AFE0 4000$_H$ - AFE0 FFFF$_H$	48 Kbyte	Reserved	LMBBET	LMBBET
	AFE1 0000$_H$ - AFE1 3FFF$_H$	16 Kbyte	Data Flash (DFLASH) Bank 1	access	access[2]
	AFE1 4000$_H$ - AFF1 FFFF$_H$	1 Mbyte	Reserved	LMBBET	LMBBET
	AFF2 0000$_H$ - AFF5 FFFF$_H$	256 Kbyte	Reserved		
	AFF6 0000$_H$ - AFFF BFFF$_H$	624 Kbyte	Reserved		
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	
11[3]	B000 0000$_H$ - BFFF FFFF$_H$	256 Mbyte	Reserved	SPBBET	SPBBE
12[1]	C000 0000$_H$ - C000 1FFF$_H$	8 Kbyte	Overlay memory (OVRAM)	access	access
	C000 2000$_H$ - CFFF FFFF$_H$	256 Mbyte	Reserved	LMBBET	LMBBET

Note: Although the polynomial above is used for generation, the generation algorithm differs from the one that is used by the Ethernet protocol.

3.7 Interrupt System

The TC1165/TC1166 interrupt system provides a flexible and time-efficient means of processing interrupts. An interrupt request can be serviced either by the CPU or by the Peripheral Control Processor (PCP). These units are called “Service Providers”. Interrupt requests are called “Service Requests” rather than “Interrupt Requests” in this document because they can be serviced by either Service Providers.

Each peripheral in the TC1165/TC1166 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two Service Providers.

As shown in **Figure 3-3**, each TC1165/TC1166 unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. Two arbitration buses connect the SRNs with two Interrupt Control Units, which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU Interrupt Arbitration Bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP and administers the PCP Interrupt Arbitration Bus.

The PCP can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

Depending on the selected system clock frequency f_{SYS}, the number of f_{SYS} clock cycles per arbitration cycle must be selected as follows:

- $f_{SYS} < 60$ MHz: ICR.CONECYC = 1 and PCP_ICR.CONECYC = 1
- $f_{SYS} > 60$ MHz: ICR.CONECYC = 0 and PCP_ICR.CONECYC = 0

3.8 Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1)

Figure 3-4 shows a global view of the functional blocks and interfaces of the two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1.

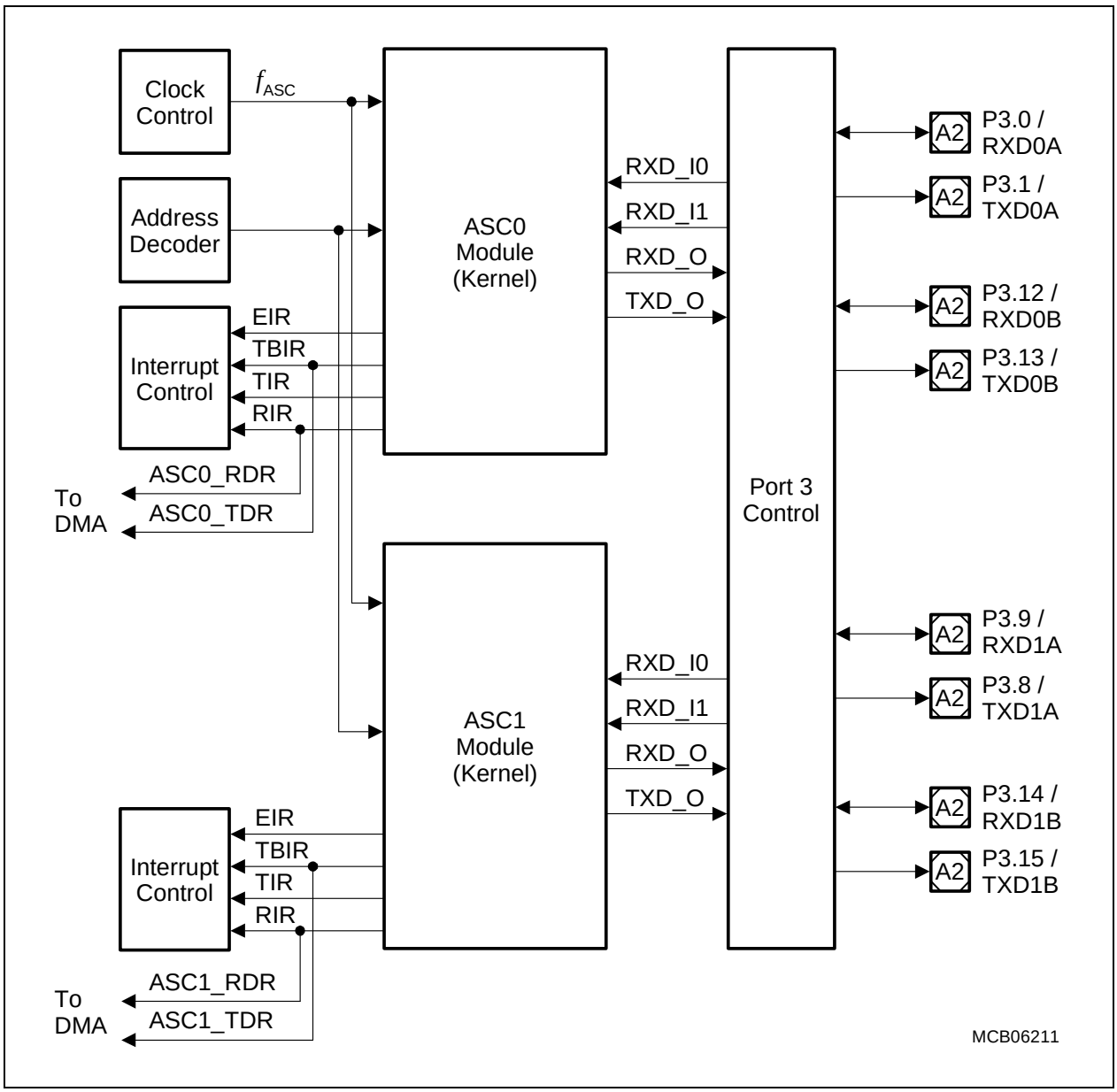

Figure 3-4 Block Diagram of the ASC Interfaces

The ASC provides serial communication between the TC1165/TC1166 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be

selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 5.0 Mbit/s to 1.19 bit/s (@ 80 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 10.0 Mbit/s to 813.8 bit/s (@ 80 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)

3.10 Micro Second Bus Interface (MSC0)

The MSC interface provides a serial communication link typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 3-6** shows a global view of the MSC interface signals.

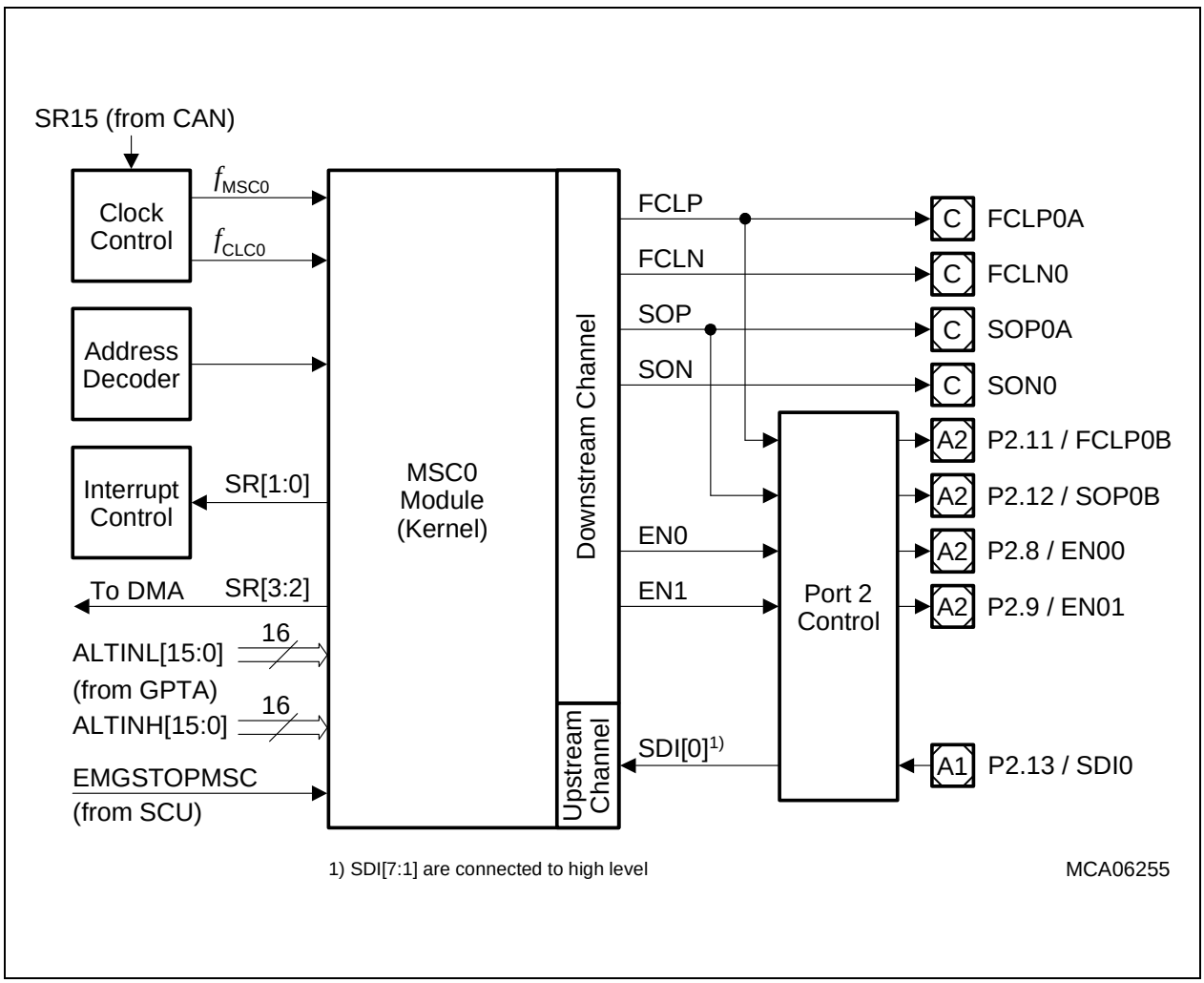

Figure 3-6 Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in emergency cases.

3.12 Micro Link Serial Bus Interface (MLI0, MLI1)

The Micro Link Interface is a fast synchronous serial interface that allows data exchange between microcontrollers of the 32-bit AUDO microcontroller family without intervention of a CPU or other bus masters. **Figure 3-8** shows how two microcontrollers are typically connected together via their MLI interfaces. The MLI operates in both microcontrollers as a bus master on the system bus.

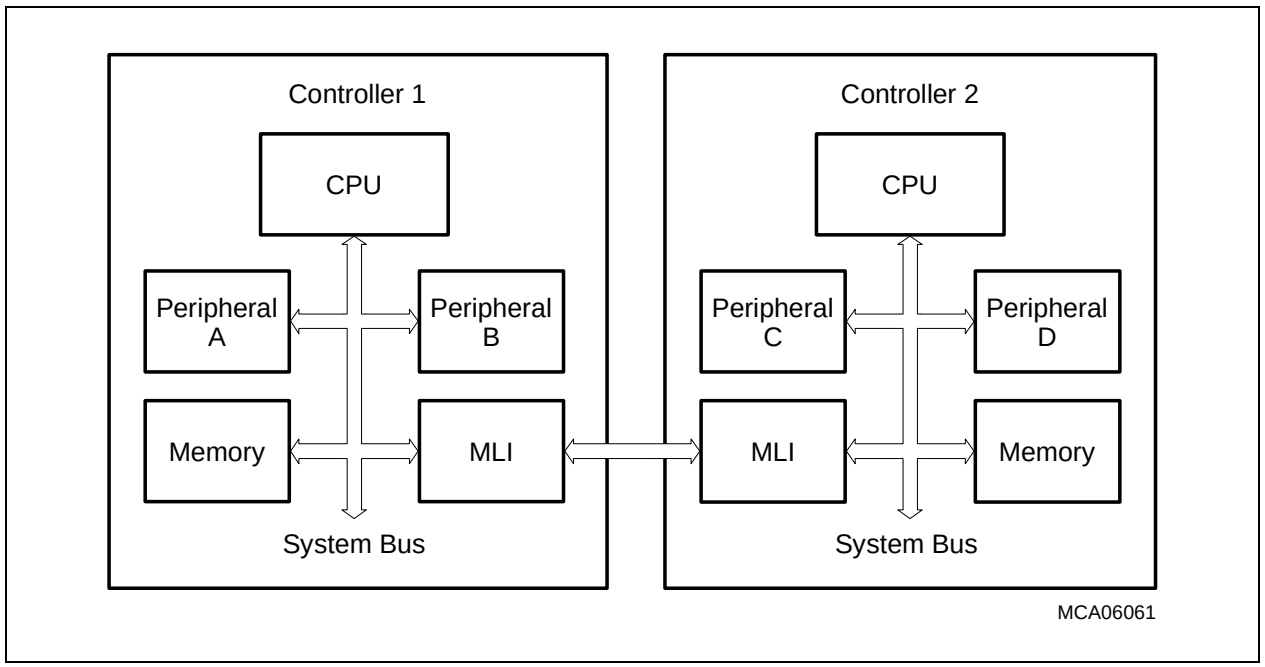

Figure 3-8 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between MLI transmitters and MLI receivers located on the same or on different microcontroller devices
- Automatic data transfer/request transactions between local/remote controller
- Fully transparent read/write access supported (= remote programming)
- Complete address range of remote controller available
- Specific frame protocol to transfer commands, addresses and data
- Error control by parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Programmable baud rate: max. module clock $f_{MLI}/2$
- Multiple remote (slave) controllers are supported

MLI transmitter and MLI receiver communicate with other off-chip MLI receivers and MLI transmitters via a 4-line serial I/O bus each. Several I/O lines of these I/O buses are available outside the MLI module kernel as four-line output or input buses.

Figure 3-9 shows a global view of the functional blocks of the two MLI modules with its interfaces.

3.19 Boot Options

The TC1165/TC1166 booting schemes provide a number of different boot options for the start of code execution. **Table 3-7** shows the boot options available in the TC1165/TC1166.

Table 3-7 TC1165/TC1166 Boot Selections

BRKIN	HWCFG [3:0]	TESTMODE	Type of Boot	BootROM Exit Jump Address
Normal Boot Options				
1	0000_B	1	Enter bootstrap loader mode 1: Serial ASC0 boot via ASC0 pins	$D400\ 0000_H$
	0001_B [1]		Enter bootstrap loader mode 2: Serial CAN boot via P3.12 and P3.13 pins	
	0010_B		Start from internal PFLASH	$A000\ 0000_H$
	0011_B		Alternate boot mode (ABM): Start from internal PFLASH after CRC check is correctly executed; enter a serial bootstrap loader mode[2] if CRC check fails	Defined in ABM header or $D400\ 0000_H$
	1111_B		Enter bootstrap loader mode 3: Serial ASC0 boot via P3.12 and P3.13 pins	$D400\ 0000_H$
	others		Reserved; execute stop loop	–
Debug Boot Options				
0	0000_B	1	Tri-state chip	–
	others	irrel.	Reserved; execute stop loop	–

1) This option is not applicable to TC1165.

2) The type of the alternate bootstrap loader mode is selected by the value of the SCU_SCLIR.SWOPT[2:0] bit field, which contains the levels of the P0.[2:0] latched in with the rising edge of the HDRST.

Table 4-4 Pin Groups for Overload/Short-Circuit Current Sum Parameter

Group	Pins
1	TRCLK, P5.[7:0], P0.[7:6], P0.[15:14]
2	P0.[13:12], P0.[5:4], P2.[13:8], SOP0A, SON0, FCLP0A, FCLN0
3	P0.[11:8], P0.[3:0], P3.[13:11]
4	P3[10:0], P3.[15:14]
5	$\overline{\text{HDRST}}$, $\overline{\text{PORST}}$, $\overline{\text{NMI}}$, $\overline{\text{TESTMODE}}$, $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, BYPASS, TCK, $\overline{\text{TRST}}$, TDO, TMS, TDI, P1.[7:4]
6	P1.[3:0], P1.[11:8], P4.[3:0]
7	P2.[7:0], P1.[14:12]
8	P5.[15:8]

4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

4.2.1 Input/Output Pins

Table 4-5 provides the characteristics of the input/output pins of the TC1165/TC1166.

Table 4-5 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
General Parameters						
Pull-up current[1)]	$\|I_{PUH}\|$	CC	10	100	µA	$V_{IN} < V_{IHAmin}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} < V_{IHAmin}$; class A3/A4 pads.
Pull-down current[1)]	$\|I_{PDL}\|$	CC	10	150	µA	$V_{IN} > V_{ILAmax}$; class A1/A2/Input pads.
			20	200	µA	$V_{IN} > V_{ILAmax}$; class A3/A4 pads.
Pin capacitance[1)] (Digital I/O)	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)						
Input low voltage class A1/A2 pins	V_{ILA}	SR	-0.3	0.34 × V_{DDP}	V	–
Input high voltage class A1/A2 pins	V_{IHA}	SR	0.64 × V_{DDP}	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.53	–	–	–
Input low voltage class A3 pins	V_{ILA3}	SR	–	0.8	V	–
Input high voltage class A3 pins	V_{IHA3}	SR	2.0	–	V	–
Input hysteresis	HYSA	CC	0.1 × V_{DDP}	–	V	[2)5)]
Input leakage current	I_{OZI}	CC	–	±3000 ±6000	nA	$(V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3)]

4.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled, which means that pads are constantly kept at the maximum strength.

4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in **Figure 4-6**, **Figure 4-7** and **Figure 4-8**.

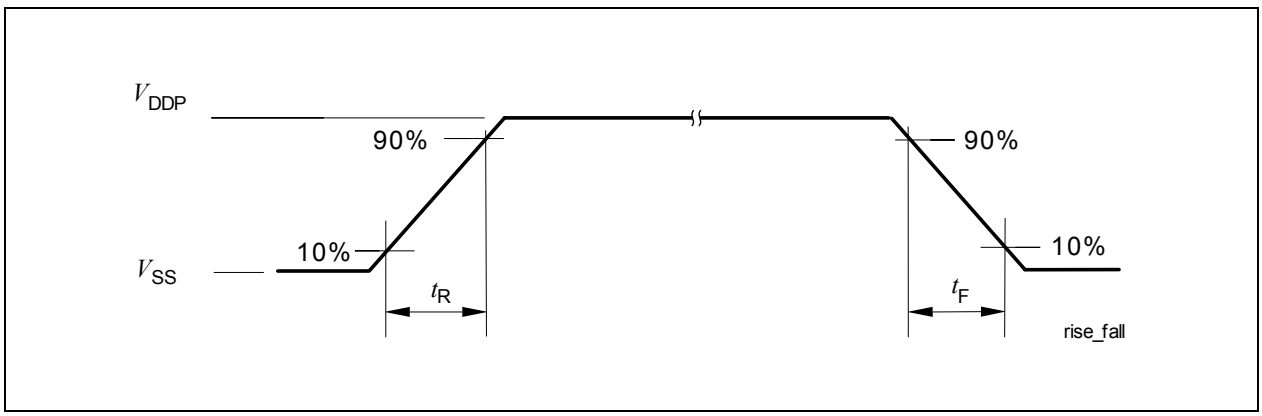

Figure 4-6 Rise/Fall Time Parameters

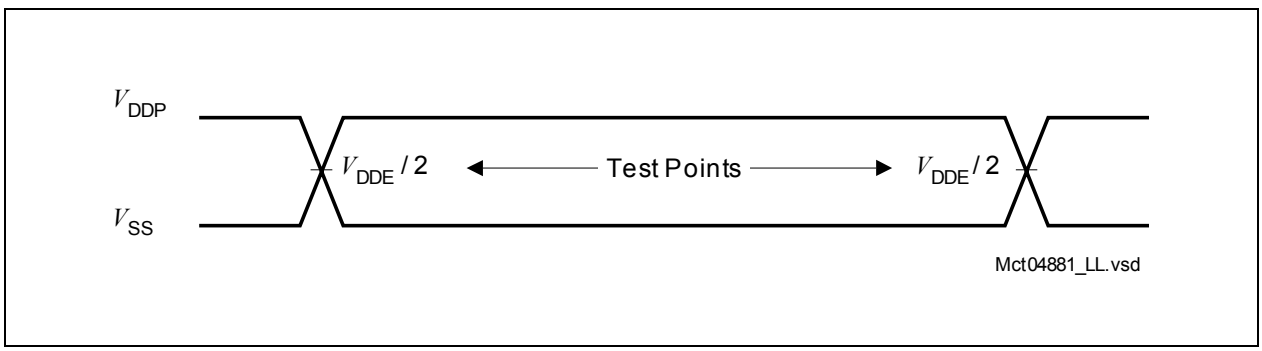

Figure 4-7 Testing Waveform, Output Delay

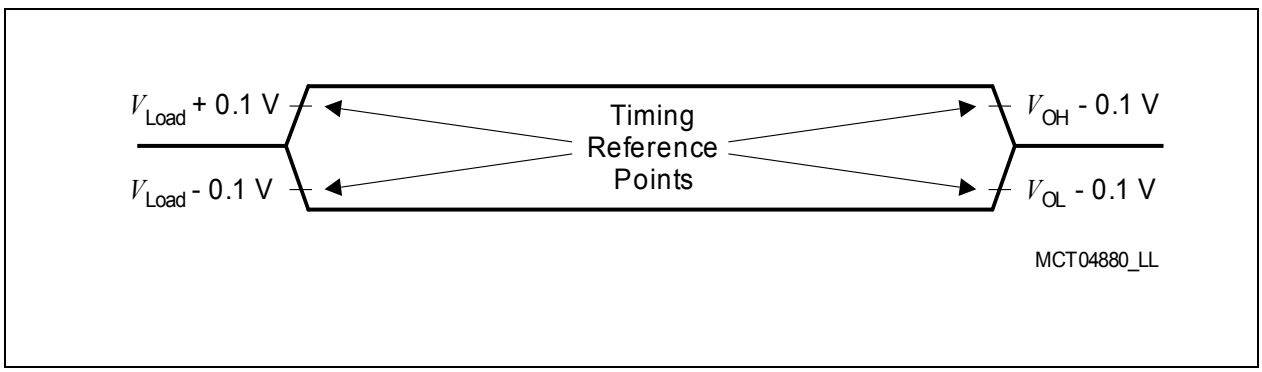

Figure 4-8 Testing Waveform, Output High Impedance

4.3.3 Power Sequencing

There is a restriction for the power sequencing of V_{DD} and V_{DDP} as shown in **Figure 4-9**: V_{DDP} must always be higher than V_{DD} - 0.5 V. The gray area shows the valid range for V_{DDP}.

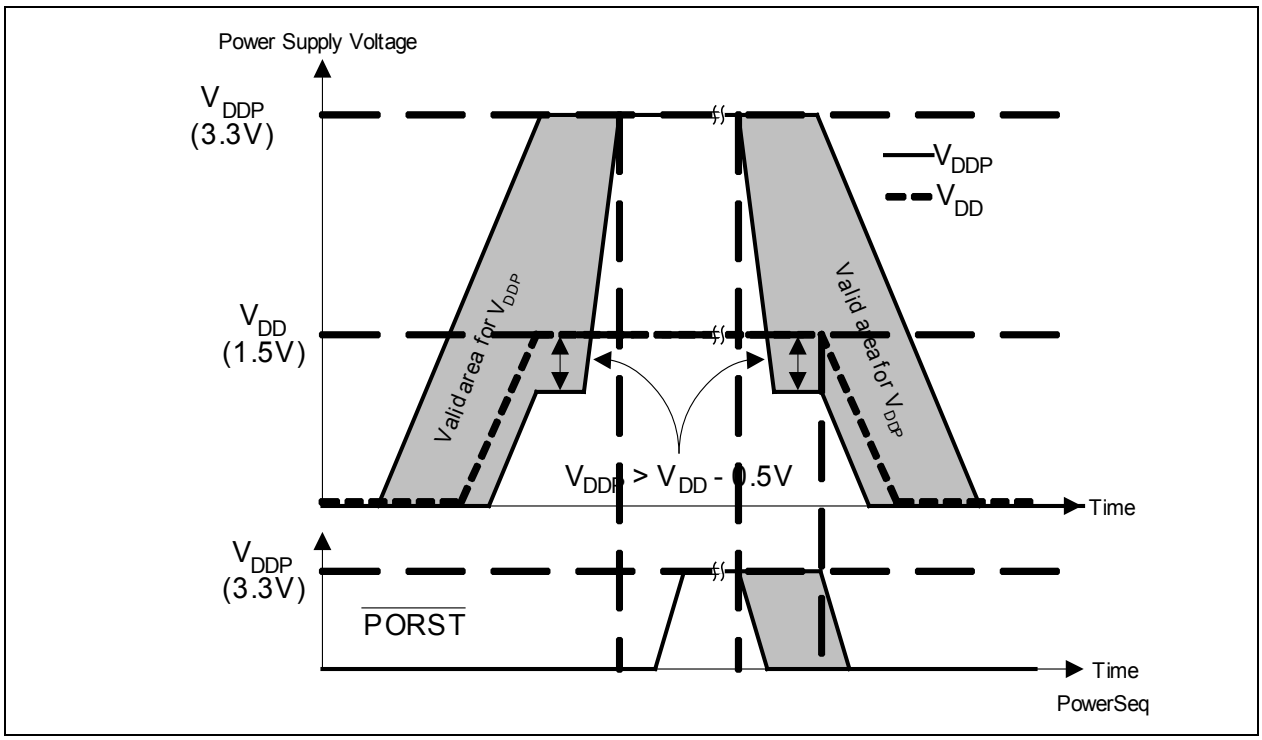

Figure 4-9 V_{DDP} / V_{DD} Power Up Sequence

All ground pins V_{SS} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 200 mV.

The $\overline{\text{PORST}}$ signal must be activated at latest before any power supply voltage falls below the levels shown on the figure below. In this case, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. Additionally, the $\overline{\text{PORST}}$ signal should be activated as soon as possible. The sooner the $\overline{\text{PORST}}$ signal is activated, the less time the system operates outside of the normal operating power supply range.

4) Applicable for input pins $\overline{\text{TESTMODE}}$, $\overline{\text{TRST}}$, $\overline{\text{BRKIN}}$, and TXD1A with noise suppression filter of $\overline{\text{PORST}}$ switched-on (BYPASS = 0).
5) The setup/hold values are applicable for Port 0 and Port 4 input pins with noise suppression filter of $\overline{\text{HDRST}}$ switched-on (BYPASS = 0), independently whether $\overline{\text{HDRST}}$ is used as input or output.
6) Not subject to production test, verified by design / characterization.
7) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
8) Not subject to production test, verified by design / characterization.
9) In case of power loss during internal flash write, prevents Flash write to random address.
10) Booting from Flash, the duration of the boot-time is defined between the rising edge of the $\overline{\text{PORST}}$ and the moment when the first user instruction has entered the CPU and its processing starts.
11) Booting from Flash, the duration of the boot time is defined between the following events:
1. Hardware reset: the falling edge of a short $\overline{\text{HDRST}}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{\text{HDRST}}$ pulse is shorter than 1024 × T_{SYS}.
If the $\overline{\text{HDRST}}$ pulse is longer than 1024 × T_{SYS}, only the time beyond the 1024 × T_{SYS} should be added to the boot time ($\overline{\text{HDRST}}$ falling edge to first user instruction).
2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

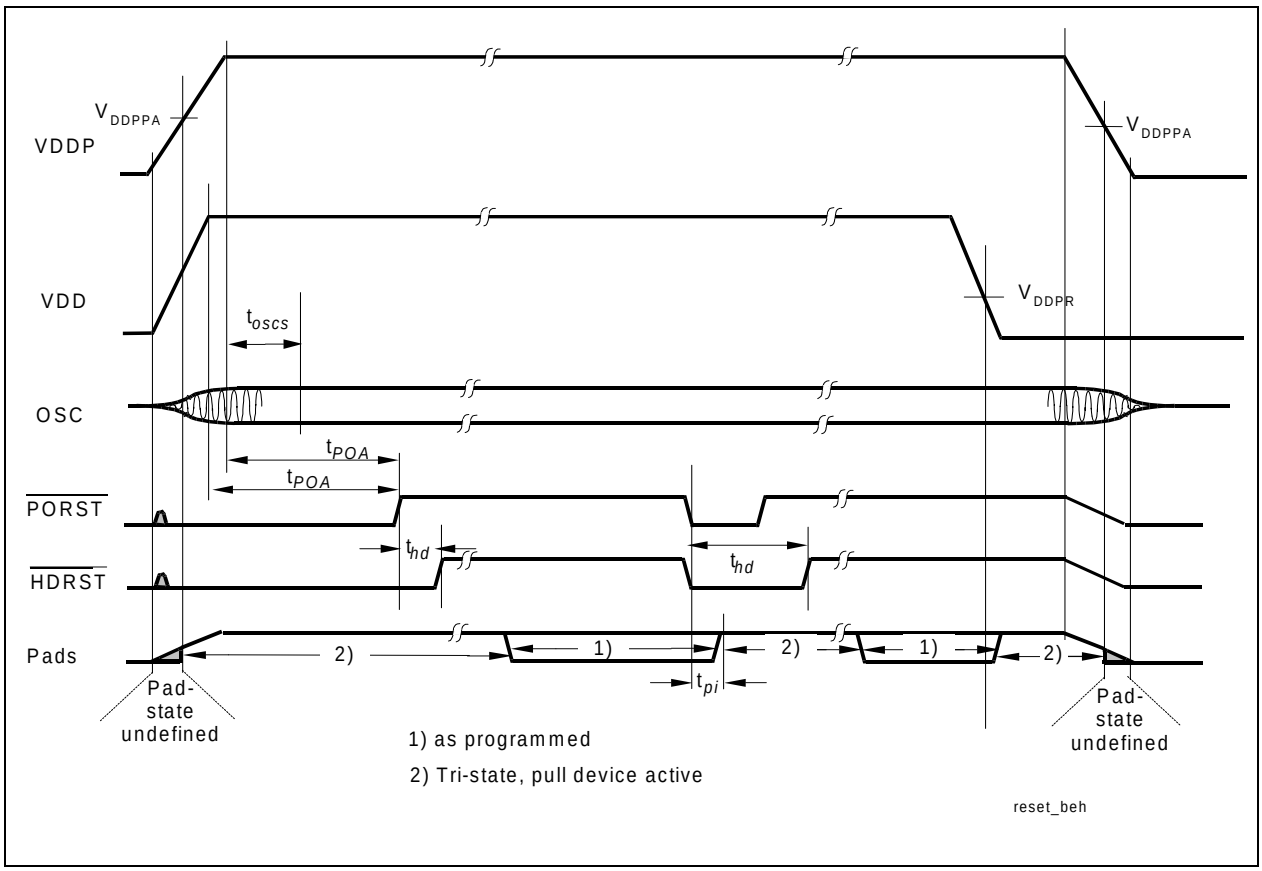

Figure 4-11 Power, Pad and Reset Timing

5 Package and Reliability

Chapter 5 provides the information of the TC1165/TC1166 package and reliability section..

5.1 Package Parameters (PG-LQFP-176-2)

Table 5-1 provides the thermal characteristics of the package.

Table 5-1 Thermal Characteristics of the Package

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Thermal resistance junction case top[1)]	R_{TJCT} CC	–	5.4	K/W	–
Thermal resistance junction case bottom[1)]	R_{TJCB} CC	–	21.5	K/W	–

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J=T_A+R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances, by
a) simply adding only the two bottom thermal resistances (junction case bottom and case ambient bottom), or
b) by taking all four resistances into account,
depending on the precision needed.