Infineon Technologies - SAF-TC1165-192F80HL AA Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, SPI, UART/USART
Peripherals	DMA, POR, WDT
Number of I/O	81
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	100K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 36x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1165-192f80hl-aa

2 General Device Information

Chapter 2 provides the general information for the TC1165/TC1166.

2.1 Block Diagram

Figure 2-1 shows the TC1165/TC1166 block diagram.

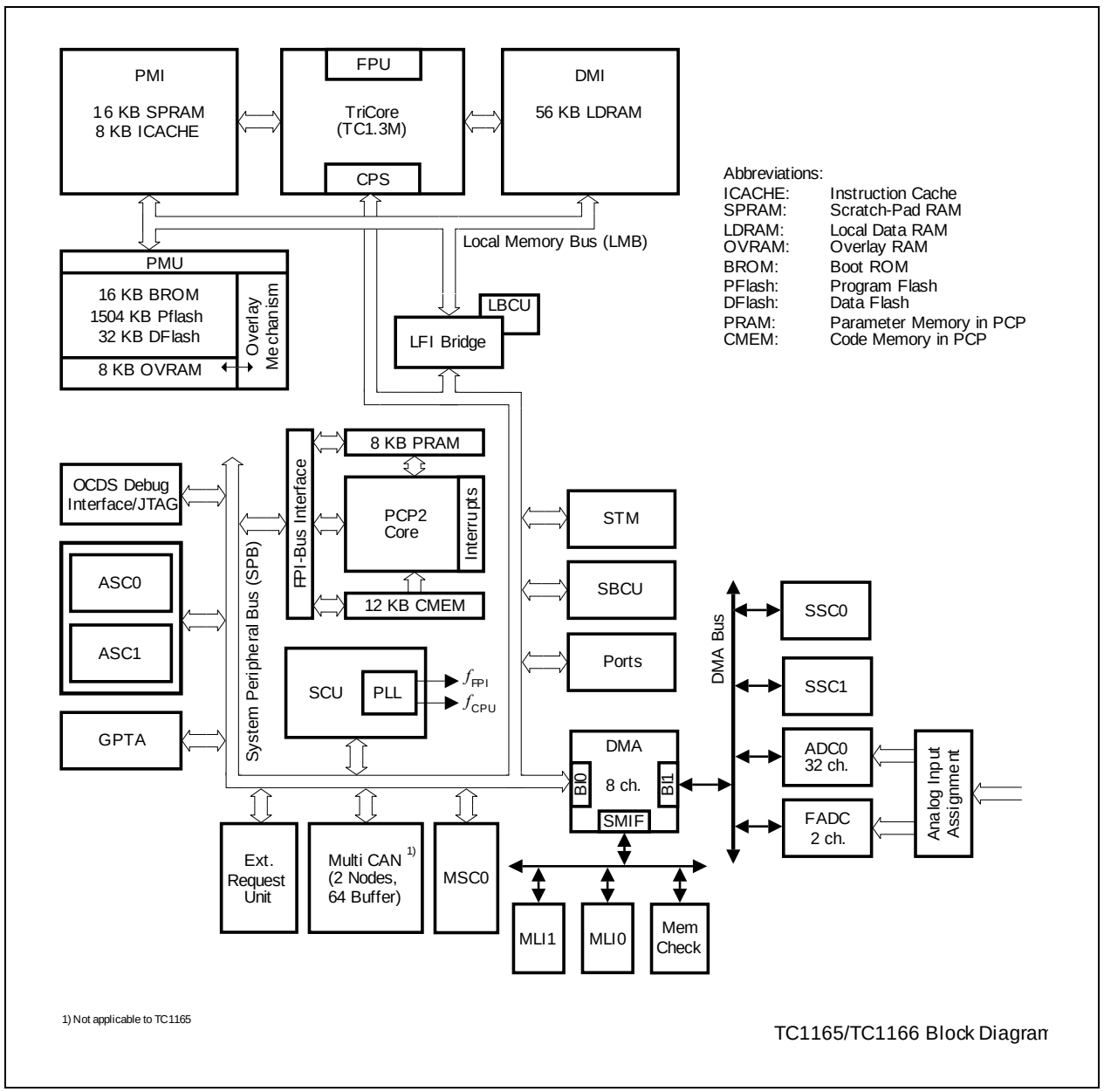

Figure 2-1 TC1165/TC1166 Block Diagram

2.4 Pad Driver and Input Classes Overview

The TC1165/TC1166 provides different types and classes of input and output lines. For understanding of the abbreviations in Table 2-1 starting at the next page, Table 4-1 gives an overview on the pad type and class types.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
AN31 AN32 AN33 AN34 AN35	32 31 30 29 28	I	D	–	Analog input 31 Analog input 32 Analog input 33 Analog input 34 Analog input 35
System I/O					
$\overline{\text{TRST}}$	114	I	A2[3]	V_{DDP}	JTAG Module Reset/Enable Input
TCK	115	I	A2[3]	V_{DDP}	JTAG Module Clock Input
TDI	111	I	A1[3]	V_{DDP}	JTAG Module Serial Data Input
TDO	113	O	A2	V_{DDP}	JTAG Module Serial Data Output
TMS	112	I	A2[3]	V_{DDP}	JTAG Module State Machine Control Input
$\overline{\text{BRKIN}}$	117	I/O	A3	V_{DDP}	OCDS Break Input (Alternate Output) [4][5]
$\overline{\text{BRK OUT}}$	116	I/O	A3	V_{DDP}	OCDS Break Output (Alternate Input) [4][5]
TRCLK	9	O	A4	V_{DDP}	Trace Clock for OCDS_L2 Lines [4]
$\overline{\text{NMI}}$	120	I	A2[6][7]	V_{DDP}	Non-Maskable Interrupt Input
$\overline{\text{HDRST}}$	122	I/O	A2[8]	V_{DDP}	Hardware Reset Input / Reset Indication Output
$\overline{\text{PORST}}$ [9]	121	I	A2[6][7]	V_{DDP}	Power-on Reset Input
BYPASS	119	I	A1[3]	V_{DDP}	PLL Clock Bypass Select Input This input has to be held stable during power-on resets. With $\overline{\text{BYPASS}}$ = 1, the spike filters in the $\overline{\text{HDRST}}$, $\overline{\text{PORST}}$ and $\overline{\text{NMI}}$ inputs are switched off.
$\overline{\text{TEST MODE}}$	118	I	A2[6][10]	V_{DDP}	Test Mode Select Input For normal operation of the TC1165/TC1166, this pin should be connected to high level.
XTAL1 XTAL2	102 103	I O	n.a.	V_{DDOSC}	Oscillator/PLL/Clock Generator Input/Output Pins

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pins	I/O	Pad Driver Class	Power Supply	Functions
V_{DDP}	11, 69, 83, 100, 124, 154, 171, 139	–	–	–	Port Power Supply (3.3 V)
V_{SS}	12, 70, 85, 101, 125, 155, 172, 140, 82	–	–	–	Ground

1) Not applicable to TC1165
2) The logical AND function of the two slave select outputs is available as a third alternate output function.
3) These pads are I/O pads with input only function. Its input characteristics are identical with the input characteristics as defined for class A pads.
4) In case of a power-fail condition (one or more power supply voltages drop below the specified voltage range), an undefined output driving level may occur at these pins.
5) Programmed by software as either break input or break output.
6) These pads are input only pads with input characteristics.
7) Input only pads with input spike filter.
8) Open drain pad with input spike filter.
9) The dual input reset system of TC1165/TC1166 assumes that the $\overline{\text{PORST}}$ reset pin is used for power on reset only.
10) Input only pads without input spike filter.

- On-chip generation of programming voltage
- JEDEC-standard based command sequences for PFLASH control
  – Write state machine controls programming and erase operations
  – Status and error reporting by status flags and interrupt
- Margin check for detection of problematic PFLASH bits

Features of Data Flash

- 32 Kbyte on-chip data Flash memory, organized in two 16 Kbyte banks
- Usable for data storage with EEPROM functionality
- 128 Byte of program interface
  – 128 bytes are programmed into one DFLASH page by one step/command
- 64-bit read interface (no burst transfers)
- Dynamic correction of single-bit errors during read access
- Detection of double-bit errors
- Fixed sector architecture
  – Two 16 Kbyte banks/sectors
  – Each sector separately erasable
- Configurable read protection (combined with write protection) for complete DFLASH together with PFLASH read protection
- Password mechanism for temporary disabling of write and read protection
- Erasing/programming of one bank possible while reading data from the other bank
- Programming of one bank while erasing the other bank possible
- On-chip generation of programming voltage
- JEDEC-standard based command sequences for DFLASH control
  – Write state machine controls programming and erase operations
  – Status and error reporting by status flags and interrupt
- Margin check for detection of problematic DFLASH bits

3.3.3 Contents of the Segments

This section summarizes the contents of the segments.

Segments 0-7

These segments are reserved segments in the TC1165/TC1166.

Segment 8

From the SPB point of view (PCP, DMA and Cerberus), this memory segment allows accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

From the CPU point of view (PMI and DMI), this memory segment allows cached accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

Segment 9

This memory segment is reserved in the TC1165/TC1166.

Segment 10

From the SPB point of view (PCP, DMA and Cerberus), this memory segment allows accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

From the CPU point of view (PMI and DMI), this memory segment allows non-cached accesses to all PMU memories (PFLASH, DFLASH, BROM, and TROM).

Segment 11

This memory segment is reserved in the TC1165/TC1166.

Segment 12

From the SPB point of view (PCP, DMA, and Cerberus), this memory segment is reserved in the TC1165/TC1166.

From the CPU point of view (PMI and DMI), this memory segment allows cached accesses to the PMU memory, OVRAM.

Segment 13

From the SPB point of view (PCP, DMA and Cerberus), this memory segment is reserved in the TC1165/TC1166.

From the CPU point of view (PMI and DMI), this memory segment allows non-cached accesses to the PMI scratch-pad RAM, read access to the boot ROM and test ROM (BROM and TROM) and the DMI memories (LDRAM).

The STM can also be read in sections from seven registers, STM_TIM0 through STM_TIM6, that select increasingly higher-order 32-bit ranges of the STM. These can be viewed as individual 32-bit timers, each with a different resolution and timing range.

The content of the 56-bit System Timer can be compared with the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 80 MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of timing the entire expected product life-time of a system without overflowing continuously.

Figure 3-13 shows an overview on the System Timer with the options for reading parts of the STM contents.

4.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in Section 4.2.1 .

Table 4-1 Pad Driver an d Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage [1]	Termination
A	3.3V	LVTTL I/O, LVTTL outputs	A1 (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
			A3 (e.g. BRKIN, BRKOUT)	80 MHz/	50 pF	6 µA	Series termination recommended (for f > 25 MHz)
			A4 (e.g. Trace Clock)	80 MHz	25 pF	6 µA	Series termination recommended
C	3.3V	LVDS	–	50 MHz		–	Parallel termination[2], 100Ω ± 10%
D	–	Analog inputs, reference voltage inputs					

1) Values are for T_{Jmax} = 125 °C.

2) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100Ω ± 10%.

4.3.8 Peripheral Timings

Section 4.3.8 provides the characteristics of the peripheral timings in the TC1165/TC1166.

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

4.3.8.1 Micro Link Interface (MLI) Timing

Table 4-17 provides the characteristics of the MLI timing in the TC1165/TC1166.

Table 4-17 MLI Timing (Opera ting Conditions apply), C_L = 50 pF

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
TCLK/RCLK clock period[1)2)]	t_{30}	CC/ SR	$2 \times T_{MLI}$[3)]	–	ns
MLI outputs delay from TCLK ↓	t_{35}	CC	0	8	ns
MLI inputs setup to RCLK ↓	t_{36}	SR	4	–	ns
MLI inputs hold to RCLK ↓	t_{37}	SR	4	–	ns
RREADY output delay from RCLK ↓	t_{38}	CC	0	8	ns

1) TCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) TCLK high and low times can be minimum $1 \times T_{MLI}$

3) $T_{MLImin} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80MHz, t_{30} = 25ns