Infineon Technologies - MB96F336USAPMC-GSE2 Datasheet

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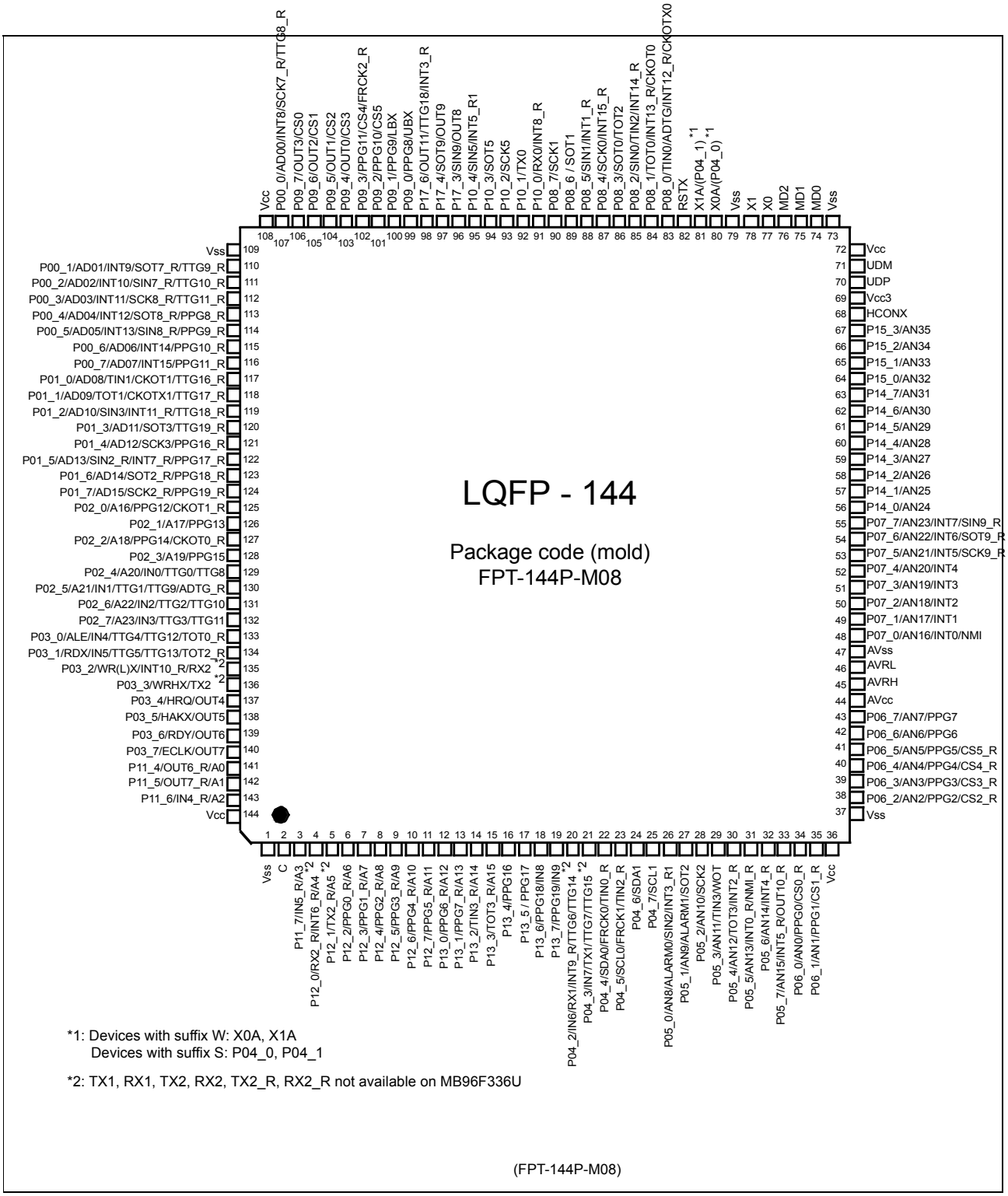
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART, USB
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	120
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f336usapmc-gse2

Pin assignment of MB96F33xU (FPT-144P-M08) USB device

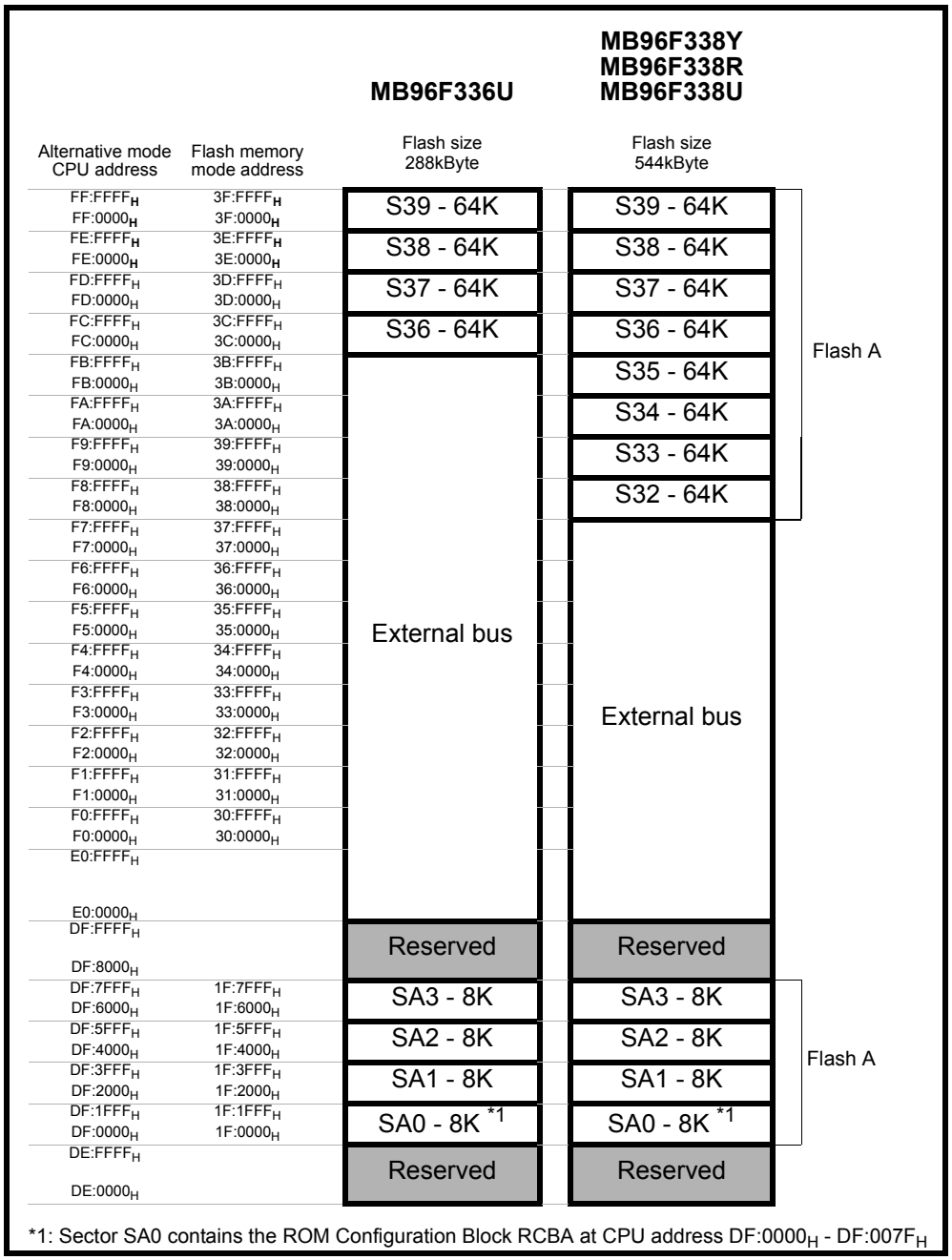


*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

*2: TX1, RX1, TX2, RX2, TX2_R, RX2_R not available on MB96F336U

(FPT-144P-M08)

9. User ROM Memory Map For Flash Devices



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000$_H$ - DF:007F$_H$

I/O map MB96(F)33x (7 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0000AD_H$	I^2C0 - Bus Control Register	IBCR0		R/W
$0000AE_H$	I^2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
$0000AF_H$	I^2C0 - Ten bit Slave address Register High	ITBAH0		R/W
$0000B0_H$	I^2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
$0000B1_H$	I^2C0 - Ten bit Address mask Register High	ITMKH0		R/W
$0000B2_H$	I^2C0 - Seven bit Slave address Register	ISBA0		R/W
$0000B3_H$	I^2C0 - Seven bit Address mask Register	ISMK0		R/W
$0000B4_H$	I^2C0 - Data Register	IDAR0		R/W
$0000B5_H$	I^2C0 - Clock Control Register	ICCR0		R/W
$0000B6_H$	I^2C1 - Bus Status Register	IBSR1		R
$0000B7_H$	I^2C1 - Bus Control Register	IBCR1		R/W
$0000B8_H$	I^2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
$0000B9_H$	I^2C1 - Ten bit Slave address Register High	ITBAH1		R/W
$0000BA_H$	I^2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
$0000BB_H$	I^2C1 - Ten bit Address mask Register High	ITMKH1		R/W
$0000BC_H$	I^2C1 - Seven bit Slave address Register	ISBA1		R/W
$0000BD_H$	I^2C1 - Seven bit Address mask Register	ISMK1		R/W
$0000BE_H$	I^2C1 - Data Register	IDAR1		R/W
$0000BF_H$	I^2C1 - Clock Control Register	ICCR1		R/W
$0000C0_H$	USART0 - Serial Mode Register	SMR0		R/W
$0000C1_H$	USART0 - Serial Control Register	SCR0		R/W
$0000C2_H$	USART0 - TX Register	TDR0		W
$0000C2_H$	USART0 - RX Register	RDR0		R
$0000C3_H$	USART0 - Serial Status	SSR0		R/W
$0000C4_H$	USART0 - Control/Com. Register	ECCR0		R/W
$0000C5_H$	USART0 - Ext. Status Register	ESCR0		R/W
$0000C6_H$	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
$0000C7_H$	USART0 - Baud Rate Generator Register High	BGRH0		R/W
$0000C8_H$	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
$0000C9_H$	Reserved			-

I/O map MB96(F)33x (13 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003B2_H$	Memory patch control/status register ch 2/3		PFCS1	R/W
$0003B3_H$	Memory patch control/status register ch 2/3			R/W
$0003B4_H$	Memory patch control/status register ch 4/5		PFCS2	R/W
$0003B5_H$	Memory patch control/status register ch 4/5			R/W
$0003B6_H$	Memory patch control/status register ch 6/7		PFCS3	R/W
$0003B7_H$	Memory patch control/status register ch 6/7			R/W
$0003B8_H$	Memory Patch function - Patch address 0 low	PFAL0		R/W
$0003B9_H$	Memory Patch function - Patch address 0 middle	PFAM0		R/W
$0003BA_H$	Memory Patch function - Patch address 0 high	PFAH0		R/W
$0003BB_H$	Memory Patch function - Patch address 1 low	PFAL1		R/W
$0003BC_H$	Memory Patch function - Patch address 1 middle	PFAM1		R/W
$0003BD_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
$0003BE_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
$0003BF_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
$0003C0_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
$0003C1_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
$0003C2_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
$0003C3_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
$0003C4_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
$0003C5_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
$0003C6_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
$0003C7_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
$0003C8_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
$0003C9_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
$0003CA_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
$0003CB_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
$0003CC_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
$0003CD_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
$0003CE_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
$0003CF_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W

I/O map MB96(F)33x (15 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000402_H	Clock Stabilization select register	CKSSR		R/W
000403_H	Clock monitor register	CKMR		R
000404_H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405_H	Clock Frequency control register High	CKFCRH		R/W
000406_H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407_H	PLL Control register High	PLLCRH		R/W
000408_H	RC clock timer control register	RCTCR		R/W
000409_H	Main clock timer control register	MCTCR		R/W
$00040A_H$	Sub clock timer control register	SCTCR		R/W
$00040B_H$	Reset cause and clock status register with clear function	RCCSRC		R
$00040C_H$	Reset configuration register	RCR		R/W
$00040D_H$	Reset cause and clock status register	RCCSR		R
$00040E_H$	Watch dog timer configuration register	WDTC		R/W
$00040F_H$	Watch dog timer clear pattern register	WDTCP		W
000410_H-000414_H	Reserved			-
000415_H	Clock output activation register	COAR		R/W
000416_H	Clock output configuration register 0	COCR0		R/W
000417_H	Clock output configuration register 1	COCR1		R/W
000418_H	Clock Modulator control register	CMCR		R/W
000419_H	Reserved			-
$00041A_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
$00041B_H$	Clock Modulator Parameter register High	CMPRH		R/W
$00041C_H$-$00042B_H$	Reserved			-
$00042C_H$	Voltage Regulator Control register	VRCR		R/W
$00042D_H$	Clock Input and LVD Control Register	CILCR		R/W
$00042E_H$-$00042F_H$	Reserved			-
000430_H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431_H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432_H	I/O Port P02 - Data Direction Register	DDR02		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$0004FF_H$	Reserved			-
000500_H	FRT2 - Data register of free-running timer		TCDT2	R/W
000501_H	FRT2 - Data register of free-running timer			R/W
000502_H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503_H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504_H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505_H	FRT3 - Data register of free-running timer			R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000506_H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507_H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508_H	OCU8 - Output Compare Control Status	OCS8		R/W
000509_H	OCU9 - Output Compare Control Status	OCS9		R/W
$00050A_H$	OCU8 - Compare Register		OCCP8	R/W
$00050B_H$	OCU8 - Compare Register			R/W
$00050C_H$	OCU9 - Compare Register		OCCP9	R/W
$00050D_H$	OCU9 - Compare Register			R/W
$00050E_H$	OCU10 - Output Compare Control Status	OCS10		R/W
$00050F_H$	OCU11 - Output Compare Control Status	OCS11		R/W
000510_H	OCU10 - Compare Register		OCCP10	R/W
000511_H	OCU10 - Compare Register			R/W
000512_H	OCU11 - Compare Register		OCCP11	R/W
000513_H	OCU11 - Compare Register			R/W
000514_H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515_H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516_H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517_H	ICU8 - Capture Register High	IPCPH8		R
000518_H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519_H	ICU9 - Capture Register High	IPCPH9		R
$00051A_H$-000529_H	Reserved			-
$00052A_H$	USART5 - Serial Mode Register	SMR5		R/W
$00052B_H$	USART5 - Serial Control Register	SCR5		R/W
$00052C_H$	USART5 - RX Register	TDR5		W
$00052C_H$	USART5 - TX Register	RDR5		R
$00052D_H$	USART5 - Serial Status	SSR5		R/W
$00052E_H$	USART5 - Control/Com. Register	ECCR5		R/W
$00052F_H$	USART5 - Ext. Status Register	ESCR5		R/W
000530_H	USART5 - Baud Rate Generator Register Low	BGRL5	BGR5	R/W
000531_H	USART5 - Baud Rate Generator Register High	BGRH5		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000597_H	PPG11 - Control status register High	PCNH11		R/W
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$	PPG13 - Timer register		PTMR13	R
$0005A5_H$	PPG13 - Timer register			R
$0005A6_H$	PPG13 - Period setting register		PCSR13	W
$0005A7_H$	PPG13 - Period setting register			W
$0005A8_H$	PPG13 - Duty cycle register		PDUT13	W
$0005A9_H$	PPG13 - Duty cycle register			W
$0005AA_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
$0005AB_H$	PPG13 - Control status register High	PCNH13		R/W
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006C8_H$	USB - EP2 Status Register Low	EP2SL0	EP2S0	R/W
$0006C9_H$	USB - EP2 Status Register High	EP2SH0		R/W
$0006CA_H$	USB - EP3 Status Register Low	EP3SL0	EP3S0	R/W
$0006CB_H$	USB - EP3 Status Register High	EP3SH0		R/W
$0006CC_H$	USB - EP4 Status Register Low	EP4SL0	EP4S0	R/W
$0006CD_H$	USB - EP4 Status Register High	EP4SH0		R/W
$0006CE_H$	USB - EP5 Status Register Low	EP5SL0	EP5S0	R/W
$0006CF_H$	USB - EP5 Status Register High	EP5SH0		R/W
$0006D0_H$	USB - EP0 Data register Low	EP0DTL0	EP0DT0	R/W
$0006D1_H$	USB - EP0 Data register High	EP0DTH0		R/W
$0006D2_H$	USB - EP1 Data register Low	EP1DTL0	EP1DT0	R/W
$0006D3_H$	USB - EP1 Data register High	EP1DTH0		R/W
$0006D4_H$	USB - EP2 Data register Low	EP2DTL0	EP2DT0	R/W
$0006D5_H$	USB - EP2 Data register High	EP2DTH0		R/W
$0006D6_H$	USB - EP3 Data register Low	EP3DTL0	EP3DT0	R/W
$0006D7_H$	USB - EP3 Data register High	EP3DTH0		R/W
$0006D8_H$	USB - EP4 Data register Low	EP4DTL0	EP4DT0	R/W
$0006D9_H$	USB - EP4 Data register High	EP4DTH0		R/W
$0006DA_H$	USB - EP5 Data register Low	EP5DTL0	EP5DT0	R/W
$0006DB_H$	USB - EP5 Data register High	EP5DTH0		R/W
$0006DC_H$-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000710_H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711_H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712_H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713_H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714_H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715_H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W
000716_H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717_H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718_H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719_H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
$00071A_H$	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
$00071B_H$	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
$00071C_H$	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
$00071D_H$	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
$00071E_H$	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
$00071F_H$	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720_H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721_H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722_H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723_H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724_H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725_H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726_H-$00073F_H$	Reserved			-
000740_H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741_H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742_H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743_H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744_H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745_H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746_H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W

12. Interrupt Vector Table

Interrupt vector table MB96(F)33x (1 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	
1	$3F8_H$	CALLV1	No	-	
2	$3F4_H$	CALLV2	No	-	
3	$3F0_H$	CALLV3	No	-	
4	$3EC_H$	CALLV4	No	-	
5	$3E8_H$	CALLV5	No	-	
6	$3E4_H$	CALLV6	No	-	
7	$3E0_H$	CALLV7	No	-	
8	$3DC_H$	RESET	No	-	
9	$3D8_H$	INT9	No	-	
10	$3D4_H$	EXCEPTION	No	-	
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	PLL_UNLOCK	No	16	Reserved
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	EXTINT1	Yes	18	External Interrupt 1
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	EXTINT5	Yes	22	External Interrupt 5
23	$3A0_H$	EXTINT6	Yes	23	External Interrupt 6
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9

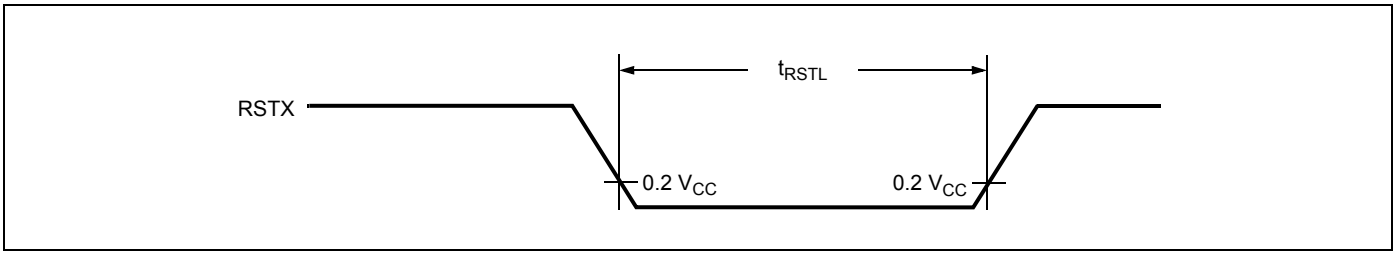
Interrupt vector table MB96(F)33x (4 of 5)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	$2B8_H$	OCU10	Yes	81	Output Compare Unit 10
82	$2B4_H$	OCU11	Yes	82	Output Compare Unit 11
83	$2B0_H$	FRT0	Yes	83	Free Running Timer 0
84	$2AC_H$	FRT1	Yes	84	Free Running Timer 1
85	$2A8_H$	FRT2	Yes	85	Free Running Timer 2
86	$2A4_H$	FRT3	Yes	86	Free Running Timer 3
87	$2A0_H$	RTC0	No	87	Real Timer Clock
88	$29C_H$	CAL0	No	88	Clock Calibration Unit
89	298_H	IIC0	Yes	89	I^2C interface
90	294_H	IIC1	Yes	90	I^2C interface
91	290_H	ADC0	Yes	91	A/D Converter
92	$28C_H$	ALARM0	No	92	Alarm Comparator 0
93	288_H	ALARM1	No	93	Alarm Comparator 1
94	284_H	LINR0	Yes	94	LIN USART 0 RX
95	280_H	LINT0	Yes	95	LIN USART 0 TX
96	$27C_H$	LINR1	Yes	96	LIN USART 1 RX
97	278_H	LINT1	Yes	97	LIN USART 1 TX
98	274_H	LINR2	Yes	98	LIN USART 2 RX
99	270_H	LINT2	Yes	99	LIN USART 2 TX
100	$26C_H$	LINR3	Yes	100	LIN USART 3 RX
101	268_H	LINT3	Yes	101	LIN USART 3 TX
102	264_H	LINR5	Yes	102	LIN USART 5 RX
103	260_H	LINT5	Yes	103	LIN USART 5 TX
104	$25C_H$	LINR7	Yes	104	LIN USART 7 RX
105	258_H	LINT7	Yes	105	LIN USART 7 TX
106	254_H	LINR8	Yes	106	LIN USART 8 RX
107	250_H	LINT8	Yes	107	LIN USART 8 TX

External Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

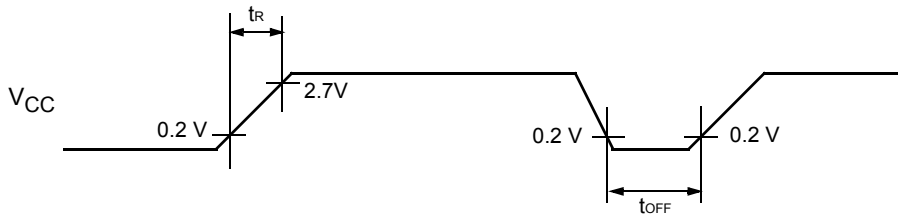
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

(T_A = −40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ Valid data input (multiplexed)	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$3t_{CYC}$ − 60	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$4t_{CYC}$ − 60		
	t_{AD-VDV}	AD[15:0]	EACL:ACE=0 EBM:NMS=0	—	$5t_{CYC}/2$ − 60	ns	w/o cycle extension
			EACL:ACE=1 EBM:NMS=0	—	$7t_{CYC}/2$ − 60		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2$ − 8	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2$ − 55	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2$ − 15	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2$ − 15	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:0], ECLK	—	t_{CYC} − 20	—	ns	
	t_{AD-VCH}	AD[15:0], ECLK		$t_{CYC}/2$ − 20	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2$ − 15	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2$ − 15	—	ns	
			EACL:STS=1	− 15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	t_{CYC} − 55	ns	

USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40°C to 125°C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		N*t_{CLKP1} - 20 *1	—	N*t_{CLKP1} - 30 *1	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series Hardware Manual”
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...

I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V,V_{SS} = AV_{SS} =0V)

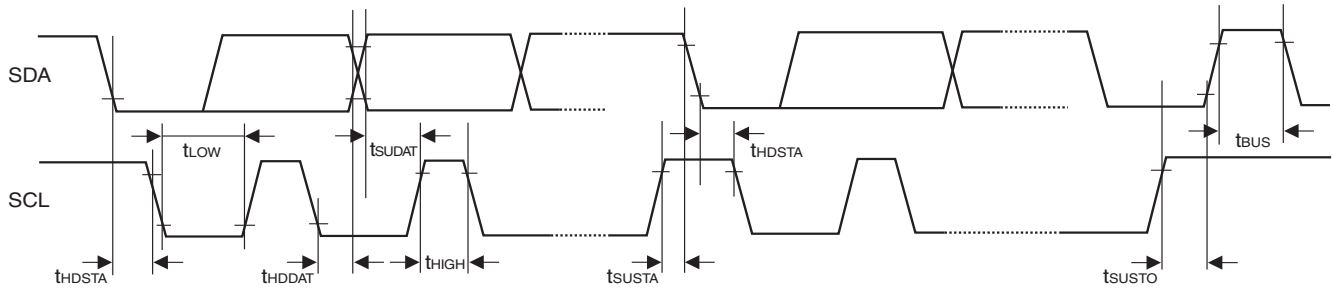
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

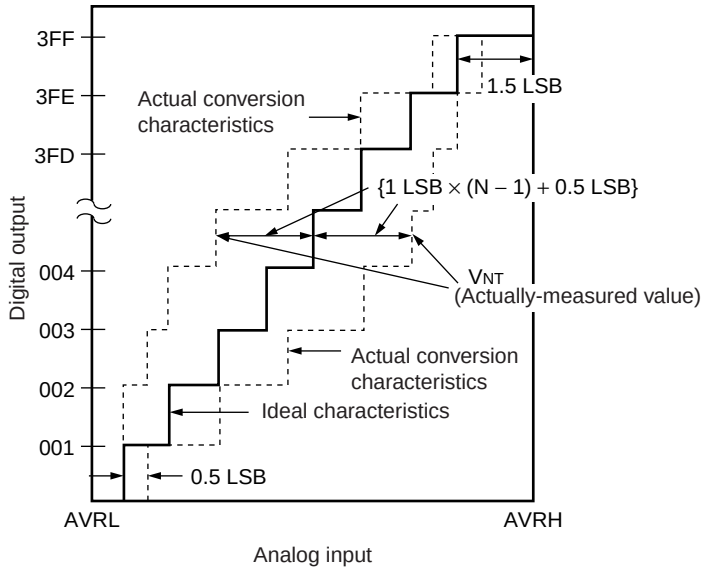
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

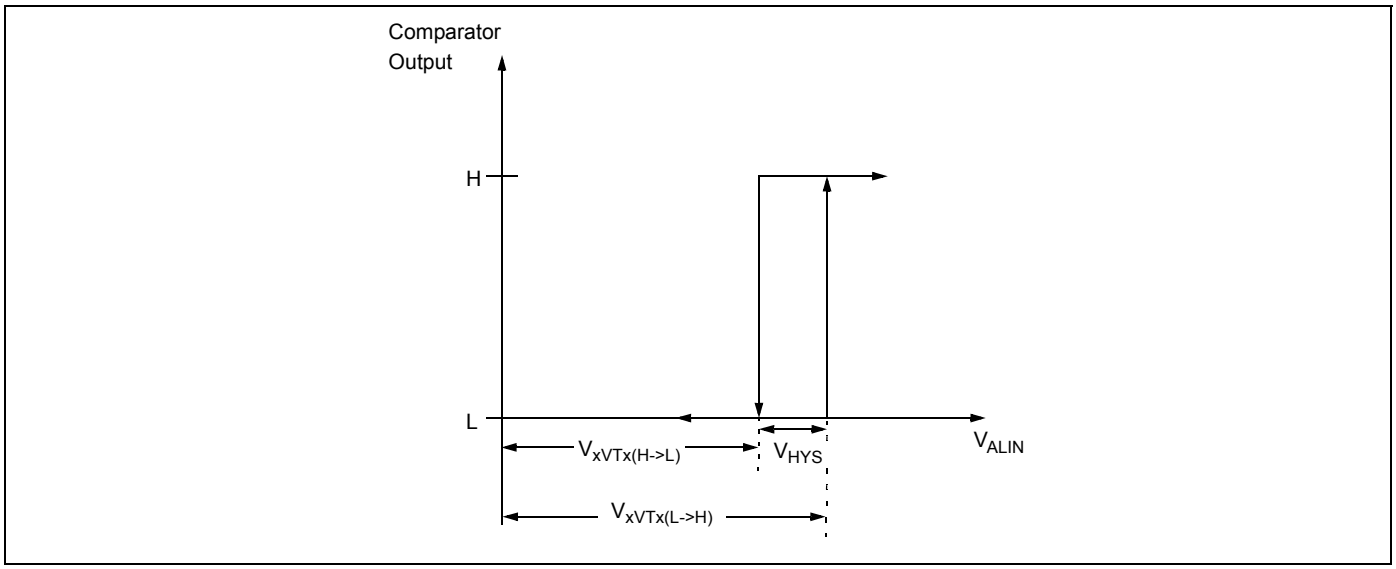
$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\ [V]$$

N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.


Comparator
Output
H
L
$V_{xVTx(H->L)}$
V_{HYS}
$V_{xVTx(L->H)}$
V_{ALIN}

14.8 Low Voltage Detector characteristics

(T_A = -40 °C to +125 °C, V_{cc} = AV_{cc} = 3.0V - 5.5V, V_{ss} = AV_{ss} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Stabilization time	$T_{LVDSTAB}$	60	75	µs	
Level 0	V_{DL0}	2.7	2.9	V	CILCR:LVL[3:0]=”0000”
Level 1	V_{DL1}	2.9	3.1	V	CILCR:LVL[3:0]=”0001”
Level 2	V_{DL2}	3.1	3.3	V	CILCR:LVL[3:0]=”0010”
Level 3	V_{DL3}	3.5	3.75	V	CILCR:LVL[3:0]=”0011”
Level 4	V_{DL4}	3.6	3.85	V	CILCR:LVL[3:0]=”0100”
Level 5	V_{DL5}	3.7	3.95	V	CILCR:LVL[3:0]=”0101”
Level 6	V_{DL6}	3.8	4.05	V	CILCR:LVL[3:0]=”0110”
Level 7	V_{DL7}	3.9	4.15	V	CILCR:LVL[3:0]=”0111”
Level 8	V_{DL8}	4.0	4.25	V	CILCR:LVL[3:0]=”1000”
Level 9	V_{DL9}	4.1	4.35	V	CILCR:LVL[3:0]=”1001”
Level 10	V_{DL10}	not used			
Level 11	V_{DL11}	not used			
Level 12	V_{DL12}	not used			
Level 13	V_{DL13}	not used			
Level 14	V_{DL14}	not used			
Level 15	V_{DL15}	not used			

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004 \frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).