Infineon Technologies - MB96F338RSAPMC-GSK5E2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	124
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 40x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f338rsapmc-gsk5e2

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I^2C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

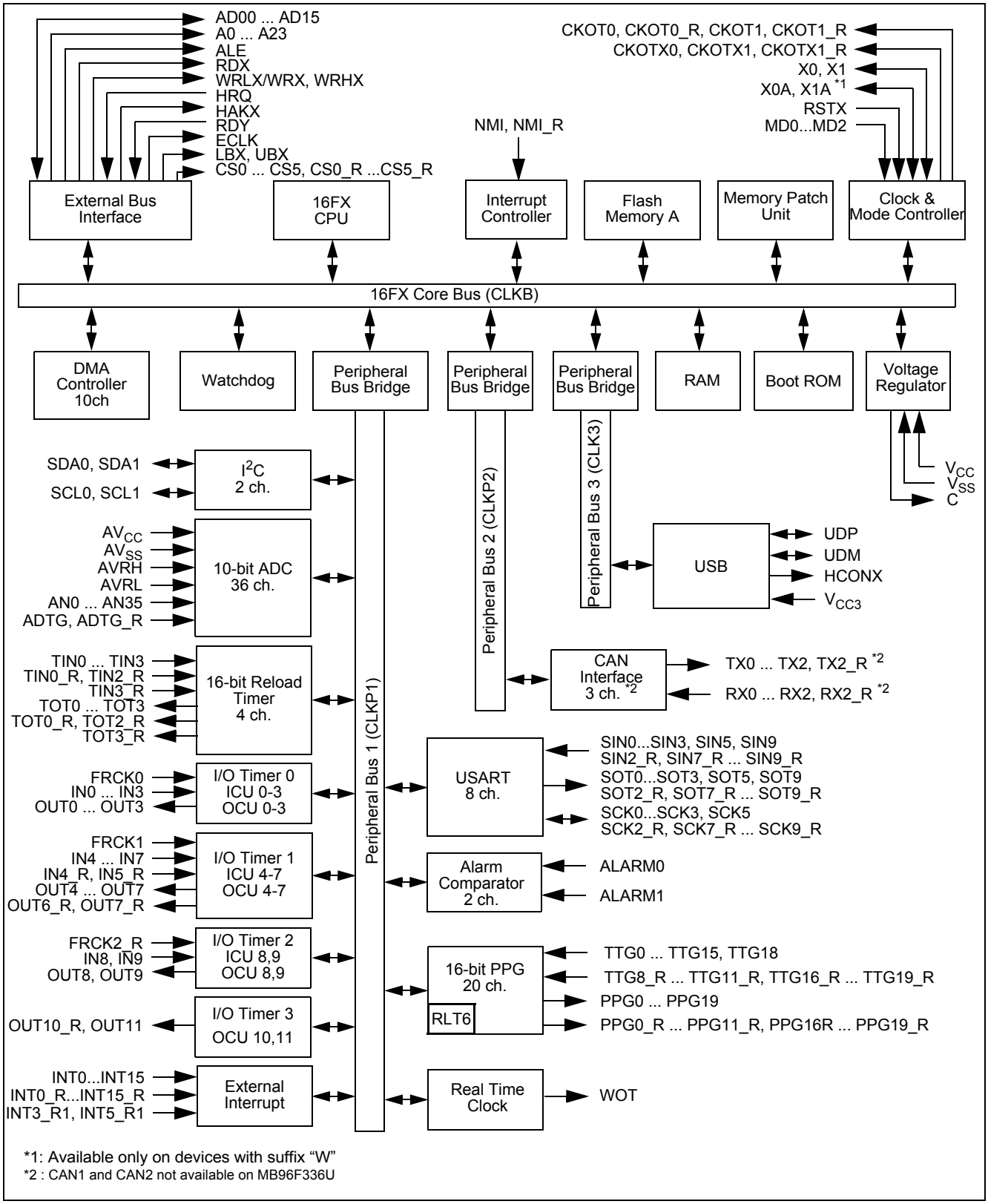
Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

Features	MB96V300	MB96(F)33xY/R	MB96(F)33xU
I/O Ports	136	122 for part number with suffix “W”, 124 for part number with suffix “S”	118 for part number with suffix “W”, 120 for part number with suffix “S”
Alarm comparator	2 channels		
External bus interface	Yes		
Chip select	6 signals		
Clock output function	2 channels		
Low voltage reset	Yes		
On-chip RC-oscillator	Yes		

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

Block diagram of MB96(F)33xU



5. Pin Circuit Type

Pin no.	FPT-144P-M08	
	Circuit type *1	
	MB96(F)33xY/R	MB96(F)33xU (USB device)
1	Supply	
2	F	
3 to 21	H	
22 to 25	N	
26 to 35	I	
36, 37	Supply	
38 to 43	I	
44	Supply	
45	G	
46 to 47	Supply	
48 to 67	I	
68	I	O
69	I	Supply (3.3V)
70, 71	I	P
72, 73	Supply	
74 to 76	C	
77, 78	A	
79	Supply	
80, 81	B *2	
80, 81	H *3	
82	E	
83 to 107	H	
108, 109	Supply	
110 to 143	H	
144	Supply	

*1: Please refer to 6.“I/O Circuit Type” for details on the I/O circuit types

*2: Devices with suffix “W”

*3: Devices without suffix “W”

I/O map MB96(F)33x (5 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000072_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073_H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074_H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075_H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076_H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077_H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078_H	PPG0 - Timer register		PTMR0	R
000079_H	PPG0 - Timer register			R
$00007A_H$	PPG0 - Period setting register		PCSR0	W
$00007B_H$	PPG0 - Period setting register			W
$00007C_H$	PPG0 - Duty cycle register		PDUT0	W
$00007D_H$	PPG0 - Duty cycle register			W
$00007E_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
$00007F_H$	PPG0 - Control status register High	PCNH0		R/W
000080_H	PPG1 - Timer register		PTMR1	R
000081_H	PPG1 - Timer register			R
000082_H	PPG1 - Period setting register		PCSR1	W
000083_H	PPG1 - Period setting register			W
000084_H	PPG1 - Duty cycle register		PDUT1	W
000085_H	PPG1 - Duty cycle register			W
000086_H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087_H	PPG1 - Control status register High	PCNH1		R/W
000088_H	PPG2 - Timer register		PTMR2	R
000089_H	PPG2 - Timer register			R
$00008A_H$	PPG2 - Period setting register		PCSR2	W
$00008B_H$	PPG2 - Period setting register			W
$00008C_H$	PPG2 - Duty cycle register		PDUT2	W
$00008D_H$	PPG2 - Duty cycle register			W
$00008E_H$	PPG2 - Control status register Low	PCNL2	PCN2	R/W

I/O map MB96(F)33x (12 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382_H	DMA2 - Interrupt select	DISEL2		R/W
000383_H	DMA3 - Interrupt select	DISEL3		R/W
000384_H	DMA4 - Interrupt select	DISEL4		R/W
000385_H	DMA5 - Interrupt select	DISEL5		R/W
000386_H	DMA6 - Interrupt select	DISEL6		R/W
000387_H	DMA7 - Interrupt select	DISEL7		R/W
000388_H	DMA8 - Interrupt select	DISEL8		R/W
000389_H	DMA9 - Interrupt select	DISEL9		R/W
$00038A_H$-$00038F_H$	Reserved			-
000390_H	DMA - Status register low byte	DSRL	DSR	R/W
000391_H	DMA - Status register high byte	DSRH		R/W
000392_H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393_H	DMA - Stop status register high byte	DSSRH		R/W
000394_H	DMA - Enable register low byte	DERL	DER	R/W
000395_H	DMA - Enable register high byte	DERH		R/W
000396_H-$00039F_H$	Reserved			-
$0003A0_H$	Interrupt level register	ILR	ICR	R/W
$0003A1_H$	Interrupt index register	IDX		R/W
$0003A2_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
$0003A3_H$	Interrupt vector table base register High	TBRH		R/W
$0003A4_H$	Delayed Interrupt register	DIRR		R/W
$0003A5_H$	Non Maskable Interrupt register	NMI		R/W
$0003A6_H$-$0003AB_H$	Reserved			-
$0003AC_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
$0003AD_H$	EDSU communication interrupt selection High	EDSU2H		R/W
$0003AE_H$	ROM mirror control register	ROMM		R/W
$0003AF_H$	EDSU configuration register	EDSU		R/W
$0003B0_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
$0003B1_H$	Memory patch control/status register ch 0/1			R/W

I/O map MB96(F)33x (16 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000433_H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434_H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435_H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436_H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437_H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438_H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439_H	I/O Port P09 - Data Direction Register	DDR09		R/W
$00043A_H$	I/O Port P10 - Data Direction Register	DDR10		R/W
$00043B_H$	I/O Port P11 - Data Direction Register	DDR11		R/W
$00043C_H$	I/O Port P12 - Data Direction Register	DDR12		R/W
$00043D_H$	I/O Port P13 - Data Direction Register	DDR13		R/W
$00043E_H$	I/O Port P14 - Data Direction Register	DDR14		R/W
$00043F_H$	I/O Port P15 - Data Direction Register	DDR15		R/W
000440_H	Reserved			-
000441_H	I/O Port P17 - Data Direction Register	DDR17		R/W
000442_H-000443_H	Reserved			-
000444_H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445_H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446_H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447_H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448_H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449_H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
$00044A_H$	I/O Port P06 - Port Input Enable Register	PIER06		R/W
$00044B_H$	I/O Port P07 - Port Input Enable Register	PIER07		R/W
$00044C_H$	I/O Port P08 - Port Input Enable Register	PIER08		R/W
$00044D_H$	I/O Port P09 - Port Input Enable Register	PIER09		R/W
$00044E_H$	I/O Port P10 - Port Input Enable Register	PIER10		R/W
$00044F_H$	I/O Port P11 - Port Input Enable Register	PIER11		R/W
000450_H	I/O Port P12 - Port Input Enable Register	PIER12		R/W
000451_H	I/O Port P13 - Port Input Enable Register	PIER13		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000471_H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472_H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473_H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W
000474_H	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475_H	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476_H	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477_H	I/O Port P11 - Extended Port Input Level Register	EPILR11		R/W
000478_H	I/O Port P12 - Extended Port Input Level Register	EPILR12		R/W
000479_H	I/O Port P13 - Extended Port Input Level Register	EPILR13		R/W
$00047A_H$	I/O Port P14 - Extended Port Input Level Register	EPILR14		R/W
$00047B_H$	I/O Port P15 - Extended Port Input Level Register	EPILR15		R/W
$00047C_H$	Reserved			-
$00047D_H$	I/O Port P17 - Extended Port Input Level Register	EPILR17		R/W
$00047E_H$-$00047F_H$	Reserved			-
000480_H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481_H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482_H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483_H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484_H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485_H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486_H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487_H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488_H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489_H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
$00048A_H$	I/O Port P10 - Port Output Drive Register	PODR10		R/W
$00048B_H$	I/O Port P11 - Port Output Drive Register	PODR11		R/W
$00048C_H$	I/O Port P12 - Port Output Drive Register	PODR12		R/W
$00048D_H$	I/O Port P13 - Port Output Drive Register	PODR13		R/W
$00048E_H$	I/O Port P14 - Port Output Drive Register	PODR14		R/W
$00048F_H$	I/O Port P15 - Port Output Drive Register	PODR15		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000597_H	PPG11 - Control status register High	PCNH11		R/W
000598_H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599_H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
$00059A_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
$00059B_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
$00059C_H$	PPG12 - Timer register		PTMR12	R
$00059D_H$	PPG12 - Timer register			R
$00059E_H$	PPG12 - Period setting register		PCSR12	W
$00059F_H$	PPG12 - Period setting register			W
$0005A0_H$	PPG12 - Duty cycle register		PDUT12	W
$0005A1_H$	PPG12 - Duty cycle register			W
$0005A2_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
$0005A3_H$	PPG12 - Control status register High	PCNH12		R/W
$0005A4_H$	PPG13 - Timer register		PTMR13	R
$0005A5_H$	PPG13 - Timer register			R
$0005A6_H$	PPG13 - Period setting register		PCSR13	W
$0005A7_H$	PPG13 - Period setting register			W
$0005A8_H$	PPG13 - Duty cycle register		PDUT13	W
$0005A9_H$	PPG13 - Duty cycle register			W
$0005AA_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
$0005AB_H$	PPG13 - Control status register High	PCNH13		R/W
$0005AC_H$	PPG14 - Timer register		PTMR14	R
$0005AD_H$	PPG14 - Timer register			R
$0005AE_H$	PPG14 - Period setting register		PCSR14	W
$0005AF_H$	PPG14 - Period setting register			W
$0005B0_H$	PPG14 - Duty cycle register		PDUT14	W
$0005B1_H$	PPG14 - Duty cycle register			W
$0005B2_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
$0005B3_H$	PPG14 - Control status register High	PCNH14		R/W
$0005B4_H$	PPG15 - Timer register		PTMR15	R

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0005B5_H$	PPG15 - Timer register			R
$0005B6_H$	PPG15 - Period setting register		PCSR15	W
$0005B7_H$	PPG15 - Period setting register			W
$0005B8_H$	PPG15 - Duty cycle register		PDUT15	W
$0005B9_H$	PPG15 - Duty cycle register			W
$0005BA_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
$0005BB_H$	PPG15 - Control status register High	PCNH15		R/W
$0005BC_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
$0005BD_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
$0005BE_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
$0005BF_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
$0005C0_H$	PPG16 - Timer register		PTMR16	R
$0005C1_H$	PPG16 - Timer register			R
$0005C2_H$	PPG16 - Period setting register		PCSR16	W
$0005C3_H$	PPG16 - Period setting register			W
$0005C4_H$	PPG16 - Duty cycle register		PDUT16	W
$0005C5_H$	PPG16 - Duty cycle register			W
$0005C6_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
$0005C7_H$	PPG16 - Control status register High	PCNH16		R/W
$0005C8_H$	PPG17 - Timer register		PTMR17	R
$0005C9_H$	PPG17 - Timer register			R
$0005CA_H$	PPG17 - Period setting register		PCSR17	W
$0005CB_H$	PPG17 - Period setting register			W
$0005CC_H$	PPG17 - Duty cycle register		PDUT17	W
$0005CD_H$	PPG17 - Duty cycle register			W
$0005CE_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
$0005CF_H$	PPG17 - Control status register High	PCNH17		R/W
$0005D0_H$	PPG18 - Timer register		PTMR18	R
$0005D1_H$	PPG18 - Timer register			R
$0005D2_H$	PPG18 - Period setting register		PCSR18	W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006C8_H$	USB - EP2 Status Register Low	EP2SL0	EP2S0	R/W
$0006C9_H$	USB - EP2 Status Register High	EP2SH0		R/W
$0006CA_H$	USB - EP3 Status Register Low	EP3SL0	EP3S0	R/W
$0006CB_H$	USB - EP3 Status Register High	EP3SH0		R/W
$0006CC_H$	USB - EP4 Status Register Low	EP4SL0	EP4S0	R/W
$0006CD_H$	USB - EP4 Status Register High	EP4SH0		R/W
$0006CE_H$	USB - EP5 Status Register Low	EP5SL0	EP5S0	R/W
$0006CF_H$	USB - EP5 Status Register High	EP5SH0		R/W
$0006D0_H$	USB - EP0 Data register Low	EP0DTL0	EP0DT0	R/W
$0006D1_H$	USB - EP0 Data register High	EP0DTH0		R/W
$0006D2_H$	USB - EP1 Data register Low	EP1DTL0	EP1DT0	R/W
$0006D3_H$	USB - EP1 Data register High	EP1DTH0		R/W
$0006D4_H$	USB - EP2 Data register Low	EP2DTL0	EP2DT0	R/W
$0006D5_H$	USB - EP2 Data register High	EP2DTH0		R/W
$0006D6_H$	USB - EP3 Data register Low	EP3DTL0	EP3DT0	R/W
$0006D7_H$	USB - EP3 Data register High	EP3DTH0		R/W
$0006D8_H$	USB - EP4 Data register Low	EP4DTL0	EP4DT0	R/W
$0006D9_H$	USB - EP4 Data register High	EP4DTH0		R/W
$0006DA_H$	USB - EP5 Data register Low	EP5DTL0	EP5DT0	R/W
$0006DB_H$	USB - EP5 Data register High	EP5DTH0		R/W
$0006DC_H$-$0006DF_H$	Reserved			-
$0006E0_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
$0006E1_H$	External Bus - Area configuration register 0 High	EACH0		R/W
$0006E2_H$	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
$0006E3_H$	External Bus - Area configuration register 1 High	EACH1		R/W
$0006E4_H$	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
$0006E5_H$	External Bus - Area configuration register 2 High	EACH2		R/W
$0006E6_H$	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
$0006E7_H$	External Bus - Area configuration register 3 High	EACH3		R/W
$0006E8_H$	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W

I/O map MB96(F)33x (33 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000747_H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748_H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749_H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
$00074A_H$	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
$00074B_H$	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
$00074C_H$	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
$00074D_H$	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
$00074E_H$	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W
$00074F_H$	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750_H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751_H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752_H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753_H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754_H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755_H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756_H-$00077F_H$	Reserved			-
000780_H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781_H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782_H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783_H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784_H-$00078F_H$	Reserved			-
000790_H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791_H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792_H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793_H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794_H-$00079F_H$	Reserved			-
$0007A0_H$	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
$0007A1_H$	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
$0007A2_H$	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
USB power supply voltage	V_{CC3}	3.0	3.3	3.6	V	USB device only
Smoothing capacitor at C pin	C_S	4.7	-	10	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{CC3} = 3.0V to 3.6V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILUSB}	UDP, UDM	-	V_{SS} - 0.3	-	0.8	V	USB pins
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -2mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -5mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH3}	3mA outputs	$4.5V \leq V_{CC} \leq 5.5V$, I_{OH} = -3mA / $3.0V \leq V_{CC} < 4.5V$, I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	
	V_{OHUSB}	UDP, UDM	$3.0V \leq V_{CC3} < 3.6V$, I_{OH} = -20mA	V_{CC3} - 0.4	-	-	V	USB pins

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz, CLKP3 = 48MHz	+25°C	39	47	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			+125°C	40	50		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	45	57	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 2 Flash/ROM wait states
			+125°C	46	60		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	56	68	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			+125°C	57	71		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 4MHz	+25°C	5	6	mA	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			+125°C	5.6	9		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 2MHz	+25°C	2.9	4	mA	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			+125°C	3.5	6.5		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 0	+25°C	0.4	0.6	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode 1 Flash/ROM wait state
			+125°C	0.9	3.5		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 1	+25°C	0.15	0.25	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.65	3.2		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 32kHz	+25°C	0.1	0.2	mA	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.6	3		

Internal Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	90	0	96	MHz	MB96F33x
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	Others than below
		0	43.5	0	48	MHz	MB96F33x
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	
Internal peripheral clock frequency (Clock CLKP3)	f_{CLKP3}	0	43.5	0	48	MHz	MB96F33x

WARNING: For USB usage, it is important to change the voltage regulator setting to output 1.9V. Please refer to the chapter Standby Mode and Voltage Regulator control circuit of the hardware manual to perform such setting.

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-20	20	ns	
	t_{CLAV}			-20	20		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		

Ready Input Timing

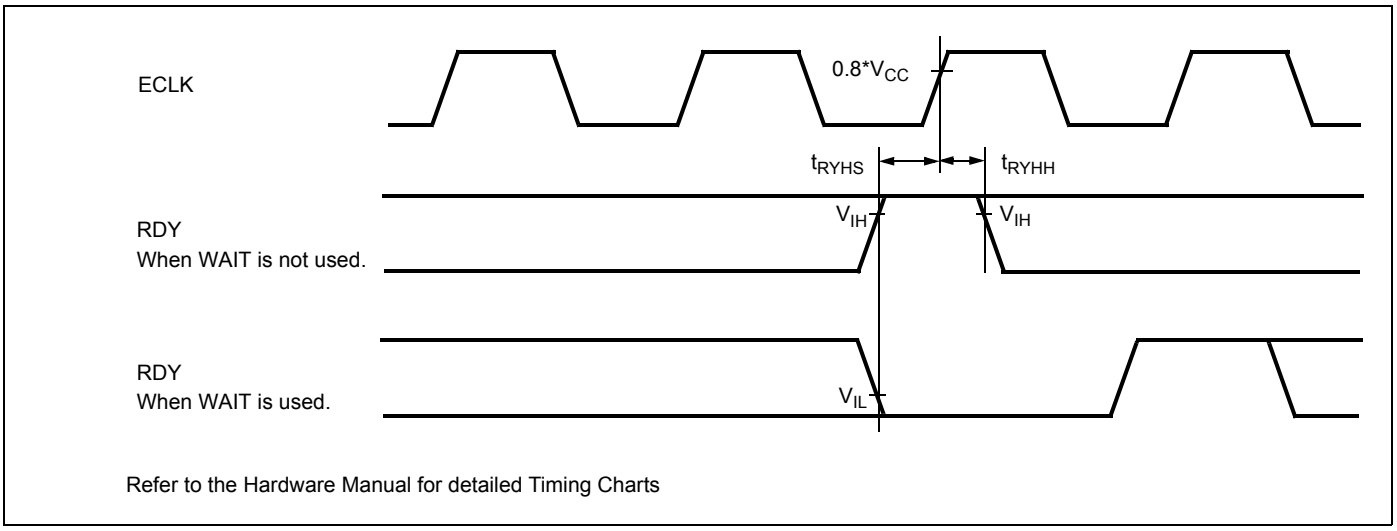
(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

(T_A = –40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



Refer to the Hardware Manual for detailed Timing Charts

14.5 USB Characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC}= 3.0V to 5.5V,V_{SS} = AV_{SS} = 0V, V_{CC3} = 3.0V to 3.6V, USB pins UDP and UDM)

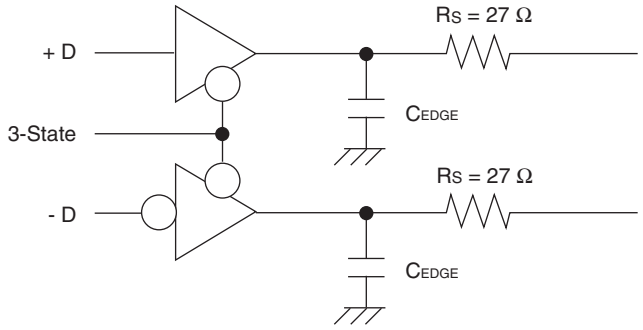
Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Input characteristics	Input High level voltage	V_{IH}	—	2.0	V_{CC} + 0.3	V	*1
	Input Low level voltage	V_{IL}	—	V_{SS} – 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}	—	0.2	—	V	*2
	Differential common mode input voltage	V_{CM}	—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}	External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}	External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}	—	1.3	2.0	V	*4
	Rise time	t_{FR}	—	4	20	nS	*5
	Fall time	t_{FF}	—	4	20	nS	*5
	Rise/fall time matching	t_{RFM}	—	90	111.11	%	*5
	Output impedance	Z_{DRV}	—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C_{EDGE}	—	—	75	pF	*6
Series resistance		R_S	—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 [V], V_{IH} (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

(Continued)

(Continued)

*6 : The place to connect transceiver edge rate control capacitance C_{EDGE}
For this USB I/O, it is recommended to use C_{EDGE} control capacitor.
For USB Max standard as 75 pF, please control the edge characteristic of output waveform by connecting 30 to 50 [pF] (recommended value : 47 [pF] ≒ 50[pF]) to D + and D − lines when implementing on the board.



Driver output impedance 3 Ω to 19 Ω
Rs serial resistance value 25 Ω to 30 Ω
Please apply 27 Ω of serial resistance value as a recommended value.