# Infineon Technologies - MB96F338USAPMC-GS-N2E2 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16FX |
| Core Size | 16-Bit |
| Speed | 48MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART, USB |
| Peripherals | DMA, LVD, LVR, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 544KB (544K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 36x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb96f338usapmc-gs-n2e2 |

**Pin Function description (3 of 3)**

| Pin name | Feature | Description |
|---|---|---|
| UDP | USB | USB plus |
| $V_{CC}$ | Supply | Power supply |
| $V_{CC3}$ | Supply | USB Power supply |
| $V_{SS}$ | Supply | Power supply |
| WOT | RTC | Real Timer clock output |
| WRHX | External bus | External bus High byte write strobe output |
| WRLX/WRX | External bus | External bus Low byte / Word write strobe output |
| X0 | Clock | Oscillator input |
| X0A | Clock | Subclock Oscillator input (only for devices with suffix “W”) |
| X1 | Clock | Oscillator output |
| X1A | Clock | Subclock Oscillator output (only for devices with suffix “W”) |

**I/O map MB96(F)33x (7 of 40)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $0000AD_H$ | $I^2C0$ - Bus Control Register | IBCR0 | | R/W |
| $0000AE_H$ | $I^2C0$ - Ten bit Slave address Register Low | ITBAL0 | ITBA0 | R/W |
| $0000AF_H$ | $I^2C0$ - Ten bit Slave address Register High | ITBAH0 | | R/W |
| $0000B0_H$ | $I^2C0$ - Ten bit Address mask Register Low | ITMKL0 | ITMK0 | R/W |
| $0000B1_H$ | $I^2C0$ - Ten bit Address mask Register High | ITMKH0 | | R/W |
| $0000B2_H$ | $I^2C0$ - Seven bit Slave address Register | ISBA0 | | R/W |
| $0000B3_H$ | $I^2C0$ - Seven bit Address mask Register | ISMK0 | | R/W |
| $0000B4_H$ | $I^2C0$ - Data Register | IDAR0 | | R/W |
| $0000B5_H$ | $I^2C0$ - Clock Control Register | ICCR0 | | R/W |
| $0000B6_H$ | $I^2C1$ - Bus Status Register | IBSR1 | | R |
| $0000B7_H$ | $I^2C1$ - Bus Control Register | IBCR1 | | R/W |
| $0000B8_H$ | $I^2C1$ - Ten bit Slave address Register Low | ITBAL1 | ITBA1 | R/W |
| $0000B9_H$ | $I^2C1$ - Ten bit Slave address Register High | ITBAH1 | | R/W |
| $0000BA_H$ | $I^2C1$ - Ten bit Address mask Register Low | ITMKL1 | ITMK1 | R/W |
| $0000BB_H$ | $I^2C1$ - Ten bit Address mask Register High | ITMKH1 | | R/W |
| $0000BC_H$ | $I^2C1$ - Seven bit Slave address Register | ISBA1 | | R/W |
| $0000BD_H$ | $I^2C1$ - Seven bit Address mask Register | ISMK1 | | R/W |
| $0000BE_H$ | $I^2C1$ - Data Register | IDAR1 | | R/W |
| $0000BF_H$ | $I^2C1$ - Clock Control Register | ICCR1 | | R/W |
| $0000C0_H$ | USART0 - Serial Mode Register | SMR0 | | R/W |
| $0000C1_H$ | USART0 - Serial Control Register | SCR0 | | R/W |
| $0000C2_H$ | USART0 - TX Register | TDR0 | | W |
| $0000C2_H$ | USART0 - RX Register | RDR0 | | R |
| $0000C3_H$ | USART0 - Serial Status | SSR0 | | R/W |
| $0000C4_H$ | USART0 - Control/Com. Register | ECCR0 | | R/W |
| $0000C5_H$ | USART0 - Ext. Status Register | ESCR0 | | R/W |
| $0000C6_H$ | USART0 - Baud Rate Generator Register Low | BGRL0 | BGR0 | R/W |
| $0000C7_H$ | USART0 - Baud Rate Generator Register High | BGRH0 | | R/W |
| $0000C8_H$ | USART0 - Extended Serial Interrupt Register | ESIR0 | | R/W |
| $0000C9_H$ | Reserved | | | - |

**I/O map MB96(F)33x (9 of 40)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $0000E5_H$ | USART3 - Baud Rate Generator Register High | BGRH3 | | R/W |
| $0000E6_H$ | USART3 - Extended Serial Interrupt Register | ESIR3 | | R/W |
| $0000E7_H$-$0000EF_H$ | Reserved | | | - |
| $0000F0_H$-$000 0FF_H$ | External Bus area | EXTBUS0 | | R/W |
| $000100_H$ | DMA0 - Buffer address pointer low byte | BAPL0 | | R/W |
| $000101_H$ | DMA0 - Buffer address pointer middle byte | BAPM0 | | R/W |
| $000102_H$ | DMA0 - Buffer address pointer high byte | BAPH0 | | R/W |
| $000103_H$ | DMA0 - DMA control register | DMACS0 | | R/W |
| $000104_H$ | DMA0 - I/O register address pointer low byte | IOAL0 | IOA0 | R/W |
| $000105_H$ | DMA0 - I/O register address pointer high byte | IOAH0 | | R/W |
| $000106_H$ | DMA0 - Data counter low byte | DCTL0 | DCT0 | R/W |
| $000107_H$ | DMA0 - Data counter high byte | DCTH0 | | R/W |
| $000108_H$ | DMA1 - Buffer address pointer low byte | BAPL1 | | R/W |
| $000109_H$ | DMA1 - Buffer address pointer middle byte | BAPM1 | | R/W |
| $00010A_H$ | DMA1 - Buffer address pointer high byte | BAPH1 | | R/W |
| $00010B_H$ | DMA1 - DMA control register | DMACS1 | | R/W |
| $00010C_H$ | DMA1 - I/O register address pointer low byte | IOAL1 | IOA1 | R/W |
| $00010D_H$ | DMA1 - I/O register address pointer high byte | IOAH1 | | R/W |
| $00010E_H$ | DMA1 - Data counter low byte | DCTL1 | DCT1 | R/W |
| $00010F_H$ | DMA1 - Data counter high byte | DCTH1 | | R/W |
| $000110_H$ | DMA2 - Buffer address pointer low byte | BAPL2 | | R/W |
| $000111_H$ | DMA2 - Buffer address pointer middle byte | BAPM2 | | R/W |
| $000112_H$ | DMA2 - Buffer address pointer high byte | BAPH2 | | R/W |
| $000113_H$ | DMA2 - DMA control register | DMACS2 | | R/W |
| $000114_H$ | DMA2 - I/O register address pointer low byte | IOAL2 | IOA2 | R/W |
| $000115_H$ | DMA2 - I/O register address pointer high byte | IOAH2 | | R/W |
| $000116_H$ | DMA2 - Data counter low byte | DCTL2 | DCT2 | R/W |
| $000117_H$ | DMA2 - Data counter high byte | DCTH2 | | R/W |
| $000118_H$ | DMA3 - Buffer address pointer low byte | BAPL3 | | R/W |

### I/O map MB96(F)33x (15 of 40)

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $000402_H$ | Clock Stabilization select register | CKSSR | | R/W |
| $000403_H$ | Clock monitor register | CKMR | | R |
| $000404_H$ | Clock Frequency control register Low | CKFCRL | CKFCR | R/W |
| $000405_H$ | Clock Frequency control register High | CKFCRH | | R/W |
| $000406_H$ | PLL Control register Low | PLLCRL | PLLCR | R/W |
| $000407_H$ | PLL Control register High | PLLCRH | | R/W |
| $000408_H$ | RC clock timer control register | RCTCR | | R/W |
| $000409_H$ | Main clock timer control register | MCTCR | | R/W |
| $00040A_H$ | Sub clock timer control register | SCTCR | | R/W |
| $00040B_H$ | Reset cause and clock status register with clear function | RCCSRC | | R |
| $00040C_H$ | Reset configuration register | RCR | | R/W |
| $00040D_H$ | Reset cause and clock status register | RCCSR | | R |
| $00040E_H$ | Watch dog timer configuration register | WDTC | | R/W |
| $00040F_H$ | Watch dog timer clear pattern register | WDTCP | | W |
| $000410_H$-$000414_H$ | Reserved | | | - |
| $000415_H$ | Clock output activation register | COAR | | R/W |
| $000416_H$ | Clock output configuration register 0 | COCR0 | | R/W |
| $000417_H$ | Clock output configuration register 1 | COCR1 | | R/W |
| $000418_H$ | Clock Modulator control register | CMCR | | R/W |
| $000419_H$ | Reserved | | | - |
| $00041A_H$ | Clock Modulator Parameter register Low | CMPRL | CMPR | R/W |
| $00041B_H$ | Clock Modulator Parameter register High | CMPRH | | R/W |
| $00041C_H$-$00042B_H$ | Reserved | | | - |
| $00042C_H$ | Voltage Regulator Control register | VRCR | | R/W |
| $00042D_H$ | Clock Input and LVD Control Register | CILCR | | R/W |
| $00042E_H$-$00042F_H$ | Reserved | | | - |
| $000430_H$ | I/O Port P00 - Data Direction Register | DDR00 | | R/W |
| $000431_H$ | I/O Port P01 - Data Direction Register | DDR01 | | R/W |
| $000432_H$ | I/O Port P02 - Data Direction Register | DDR02 | | R/W |

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| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $000452_H$ | I/O Port P14 - Port Input Enable Register | PIER14 | | R/W |
| $000453_H$ | I/O Port P15 - Port Input Enable Register | PIER15 | | R/W |
| $000454_H$ | Reserved | | | - |
| $000455_H$ | I/O Port P17 - Port Input Enable Register | PIER17 | | R/W |
| $000456_H$-$000457_H$ | Reserved | | | - |
| $000458_H$ | I/O Port P00 - Port Input Level Register | PILR00 | | R/W |
| $000459_H$ | I/O Port P01 - Port Input Level Register | PILR01 | | R/W |
| $00045A_H$ | I/O Port P02 - Port Input Level Register | PILR02 | | R/W |
| $00045B_H$ | I/O Port P03 - Port Input Level Register | PILR03 | | R/W |
| $00045C_H$ | I/O Port P04 - Port Input Level Register | PILR04 | | R/W |
| $00045D_H$ | I/O Port P05 - Port Input Level Register | PILR05 | | R/W |
| $00045E_H$ | I/O Port P06 - Port Input Level Register | PILR06 | | R/W |
| $00045F_H$ | I/O Port P07 - Port Input Level Register | PILR07 | | R/W |
| $000460_H$ | I/O Port P08 - Port Input Level Register | PILR08 | | R/W |
| $000461_H$ | I/O Port P09 - Port Input Level Register | PILR09 | | R/W |
| $000462_H$ | I/O Port P10 - Port Input Level Register | PILR10 | | R/W |
| $000463_H$ | I/O Port P11 - Port Input Level Register | PILR11 | | R/W |
| $000464_H$ | I/O Port P12 - Port Input Level Register | PILR12 | | R/W |
| $000465_H$ | I/O Port P13 - Port Input Level Register | PILR13 | | R/W |
| $000466_H$ | I/O Port P14 - Port Input Level Register | PILR14 | | R/W |
| $000467_H$ | I/O Port P15 - Port Input Level Register | PILR15 | | R/W |
| $000468_H$ | Reserved | | | - |
| $000469_H$ | I/O Port P17 - Port Input Level Register | PILR17 | | R/W |
| $00046A_H$-$00046B_H$ | Reserved | | | - |
| $00046C_H$ | I/O Port P00 - Extended Port Input Level Register | EPILR00 | | R/W |
| $00046D_H$ | I/O Port P01 - Extended Port Input Level Register | EPILR01 | | R/W |
| $00046E_H$ | I/O Port P02 - Extended Port Input Level Register | EPILR02 | | R/W |
| $00046F_H$ | I/O Port P03 - Extended Port Input Level Register | EPILR03 | | R/W |
| $000470_H$ | I/O Port P04 - Extended Port Input Level Register | EPILR04 | | R/W |

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| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $0007A3_H$ | CAN0 - Interrupt Pending 2 Register High | INTPND2H0 | | R |
| $0007A4_H$-$0007AF_H$ | Reserved | | | - |
| $0007B0_H$ | CAN0 - Message Valid 1 Register Low | MSGVAL1L0 | MSGVAL10 | R |
| $0007B1_H$ | CAN0 - Message Valid 1 Register High | MSGVAL1H0 | | R |
| $0007B2_H$ | CAN0 - Message Valid 2 Register Low | MSGVAL2L0 | MSGVAL20 | R |
| $0007B3_H$ | CAN0 - Message Valid 2 Register High | MSGVAL2H0 | | R |
| $0007B4_H$-$0007CD_H$ | Reserved | | | - |
| $0007CE_H$ | CAN0 - Output enable register | COER0 | | R/W |
| $0007CF_H$-$0007FF_H$ | Reserved | | | - |
| $000800_H$ | CAN1 - Control register Low | CTRLRL1 | CTRLR1 | R/W |
| $000801_H$ | CAN1 - Control register High (reserved) | CTRLRH1 | | R |
| $000802_H$ | CAN1 - Status register Low | STATRL1 | STATR1 | R/W |
| $000803_H$ | CAN1 - Status register High (reserved) | STATRH1 | | R |
| $000804_H$ | CAN1 - Error Counter Low (Transmit) | ERRCNTL1 | ERRCNT1 | R |
| $000805_H$ | CAN1 - Error Counter High (Receive) | ERRCNTH1 | | R |
| $000806_H$ | CAN1 - Bit Timing Register Low | BTRL1 | BTR1 | R/W |
| $000807_H$ | CAN1 - Bit Timing Register High | BTRH1 | | R/W |
| $000808_H$ | CAN1 - Interrupt Register Low | INTRL1 | INTR1 | R |
| $000809_H$ | CAN1 - Interrupt Register High | INTRH1 | | R |
| $00080A_H$ | CAN1 - Test Register Low | TESTRL1 | TESTR1 | R/W |
| $00080B_H$ | CAN1 - Test Register High (reserved) | TESTRH1 | | R |
| $00080C_H$ | CAN1 - BRP Extension register Low | BRPERL1 | BRPER1 | R/W |
| $00080D_H$ | CAN1 - BRP Extension register High (reserved) | BRPERH1 | | R |
| $00080E_H$-$00080F_H$ | Reserved | | | - |
| $000810_H$ | CAN1 - IF1 Command request register Low | IF1CREQL1 | IF1CREQ1 | R/W |
| $000811_H$ | CAN1 - IF1 Command request register High | IF1CREQH1 | | R/W |
| $000812_H$ | CAN1 - IF1 Command Mask register Low | IF1CMSKL1 | IF1CMSK1 | R/W |
| $000813_H$ | CAN1 - IF1 Command Mask register High (reserved) | IF1CMSKH1 | | R |

**I/O map MB96(F)33x (37 of 40)**

| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $0008B1_H$ | CAN1 - Message Valid 1 Register High | MSGVAL1H1 | | R |
| $0008B2_H$ | CAN1 - Message Valid 2 Register Low | MSGVAL2L1 | MSGVAL21 | R |
| $0008B3_H$ | CAN1 - Message Valid 2 Register High | MSGVAL2H1 | | R |
| $0008B4_H$-$0008CD_H$ | Reserved | | | - |
| $0008CE_H$ | CAN1 - Output enable register | COER1 | | R/W |
| $0008CF_H$-$0008FF_H$ | Reserved | | | - |
| $000900_H$ | CAN2 - Control register Low | CTRLRL2 | CTRLR2 | R/W |
| $000901_H$ | CAN2 - Control register High (reserved) | CTRLRH2 | | R |
| $000902_H$ | CAN2 - Status register Low | STATRL2 | STATR2 | R/W |
| $000903_H$ | CAN2 - Status register High (reserved) | STATRH2 | | R |
| $000904_H$ | CAN2 - Error Counter Low (Transmit) | ERRCNTL2 | ERRCNT2 | R |
| $000905_H$ | CAN2 - Error Counter High (Receive) | ERRCNTH2 | | R |
| $000906_H$ | CAN2 - Bit Timing Register Low | BTRL2 | BTR2 | R/W |
| $000907_H$ | CAN2 - Bit Timing Register High | BTRH2 | | R/W |
| $000908_H$ | CAN2 - Interrupt Register Low | INTRL2 | INTR2 | R |
| $000909_H$ | CAN2 - Interrupt Register High | INTRH2 | | R |
| $00090A_H$ | CAN2 - Test Register Low | TESTRL2 | TESTR2 | R/W |
| $00090B_H$ | CAN2 - Test Register High (reserved) | TESTRH2 | | R |
| $00090C_H$ | CAN2 - BRP Extension register Low | BRPERL2 | BRPER2 | R/W |
| $00090D_H$ | CAN2 - BRP Extension register High (reserved) | BRPERH2 | | R |
| $00090E_H$-$00090F_H$ | Reserved | | | - |
| $000910_H$ | CAN2 - IF1 Command request register Low | IF1CREQL2 | IF1CREQ2 | R/W |
| $000911_H$ | CAN2 - IF1 Command request register High | IF1CREQH2 | | R/W |
| $000912_H$ | CAN2 - IF1 Command Mask register Low | IF1CMSKL2 | IF1CMSK2 | R/W |
| $000913_H$ | CAN2 - IF1 Command Mask register High (reserved) | IF1CMSKH2 | | R |
| $000914_H$ | CAN2 - IF1 Mask 1 Register Low | IF1MSK1L2 | IF1MSK12 | R/W |
| $000915_H$ | CAN2 - IF1 Mask 1 Register High | IF1MSK1H2 | | R/W |
| $000916_H$ | CAN2 - IF1 Mask 2 Register Low | IF1MSK2L2 | IF1MSK22 | R/W |
| $000917_H$ | CAN2 - IF1 Mask 2 Register High | IF1MSK2H2 | | R/W |

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| Address | Register | Abbreviation 8-bit access | Abbreviation 16-bit access | Access |
|---|---|---|---|---|
| $000918_H$ | CAN2 - IF1 Arbitration 1 Register Low | IF1ARB1L2 | IF1ARB12 | R/W |
| $000919_H$ | CAN2 - IF1 Arbitration 1 Register High | IF1ARB1H2 | | R/W |
| $00091A_H$ | CAN2 - IF1 Arbitration 2 Register Low | IF1ARB2L2 | IF1ARB22 | R/W |
| $00091B_H$ | CAN2 - IF1 Arbitration 2 Register High | IF1ARB2H2 | | R/W |
| $00091C_H$ | CAN2 - IF1 Message Control Register Low | IF1MCTRL2 | IF1MCTR2 | R/W |
| $00091D_H$ | CAN2 - IF1 Message Control Register High | IF1MCTRH2 | | R/W |
| $00091E_H$ | CAN2 - IF1 Data A1 Low | IF1DTA1L2 | IF1DTA12 | R/W |
| $00091F_H$ | CAN2 - IF1 Data A1 High | IF1DTA1H2 | | R/W |
| $000920_H$ | CAN2 - IF1 Data A2 Low | IF1DTA2L2 | IF1DTA22 | R/W |
| $000921_H$ | CAN2 - IF1 Data A2 High | IF1DTA2H2 | | R/W |
| $000922_H$ | CAN2 - IF1 Data B1 Low | IF1DTB1L2 | IF1DTB12 | R/W |
| $000923_H$ | CAN2 - IF1 Data B1 High | IF1DTB1H2 | | R/W |
| $000924_H$ | CAN2 - IF1 Data B2 Low | IF1DTB2L2 | IF1DTB22 | R/W |
| $000925_H$ | CAN2 - IF1 Data B2 High | IF1DTB2H2 | | R/W |
| $000926_H$-$00093F_H$ | Reserved | | | - |
| $000940_H$ | CAN2 - IF2 Command request register Low | IF2CREQL2 | IF2CREQ2 | R/W |
| $000941_H$ | CAN2 - IF2 Command request register High | IF2CREQH2 | | R/W |
| $000942_H$ | CAN2 - IF2 Command Mask register Low | IF2CMSKL2 | IF2CMSK2 | R/W |
| $000943_H$ | CAN2 - IF2 Command Mask register High (reserved) | IF2CMSKH2 | | R |
| $000944_H$ | CAN2 - IF2 Mask 1 Register Low | IF2MSK1L2 | IF2MSK12 | R/W |
| $000945_H$ | CAN2 - IF2 Mask 1 Register High | IF2MSK1H2 | | R/W |
| $000946_H$ | CAN2 - IF2 Mask 2 Register Low | IF2MSK2L2 | IF2MSK22 | R/W |
| $000947_H$ | CAN2 - IF2 Mask 2 Register High | IF2MSK2H2 | | R/W |
| $000948_H$ | CAN2 - IF2 Arbitration 1 Register Low | IF2ARB1L2 | IF2ARB12 | R/W |
| $000949_H$ | CAN2 - IF2 Arbitration 1 Register High | IF2ARB1H2 | | R/W |
| $00094A_H$ | CAN2 - IF2 Arbitration 2 Register Low | IF2ARB2L2 | IF2ARB22 | R/W |
| $00094B_H$ | CAN2 - IF2 Arbitration 2 Register High | IF2ARB2H2 | | R/W |
| $00094C_H$ | CAN2 - IF2 Message Control Register Low | IF2MCTRL2 | IF2MCTR2 | R/W |
| $00094D_H$ | CAN2 - IF2 Message Control Register High | IF2MCTRH2 | | R/W |
| $00094E_H$ | CAN2 - IF2 Data A1 Low | IF2DTA1L2 | IF2DTA12 | R/W |

**Interrupt vector table MB96(F)33x (5 of 5)**

| Vector number | Offset in vector table | Vector name | Cleared by DMA | Index in ICR to program | Description |
|---|---|---|---|---|---|
| 108 | $24C_H$ | LINR9 | Yes | 108 | LIN USART 9 RX |
| 109 | $248_H$ | LINT9 | Yes | 109 | LIN USART 9 TX |
| 110 | $244_H$ | FLASH_A | No | 110 | Main Flash memory interrupt (only Flash devices) |
| 111 | $240_H$ | reserved | - | - | reserved |
| 112 | $23C_H$ | USB_EP0IN0 | Yes | 112 | USB End point 0 IN |
| 113 | $238_H$ | USB_EP0OUT0 | Yes | 113 | USB End point 0 OUT |
| 114 | $234_H$ | USB_EP10 | Yes | 114 | USB End point 1 |
| 115 | $230_H$ | USB_EP20 | Yes | 115 | USB End point 2 |
| 116 | $22C_H$ | USB_EP30 | Yes | 116 | USB End point 3 |
| 117 | $228_H$ | USB_EP40 | Yes | 117 | USB End point 4 |
| 118 | $224_H$ | USB_EP50 | Yes | 118 | USB End point 5 |
| 119 | $220_H$ | USB_F10 | No | 119 | USB function Flags 1 (SUSP SOF BRST WKUP CONF) |
| 120 | $21C_H$ | USB_F20 | No | 120 | USB function Flags 2 (SPK) |
| 121 | $218_H$ | USB_H10 | No | 121 | USB MiniHost 1 (DIRQ CNNIRQ URIRQ RWKIRQ) |
| 122 | $214_H$ | USB_H20 | No | 122 | USB MiniHost 2 (SOFIRQ CMPIRQ) |

# 13. Handling Devices

**Special care is required for the following when handling the device:**

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins ($V_{CC}$/$V_{SS}$)
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage

## 13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between $V_{CC}$ pins and $V_{SS}$ pins.
- The $AV_{CC}$ power supply is applied before the $V_{CC}$ voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ($AV_{CC}$, AVRH) exceed the digital power-supply voltage.

## 13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

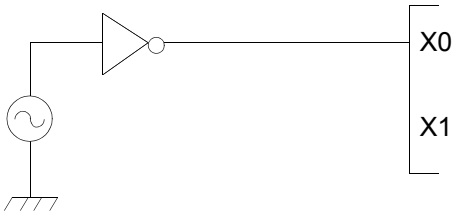
Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

## 13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

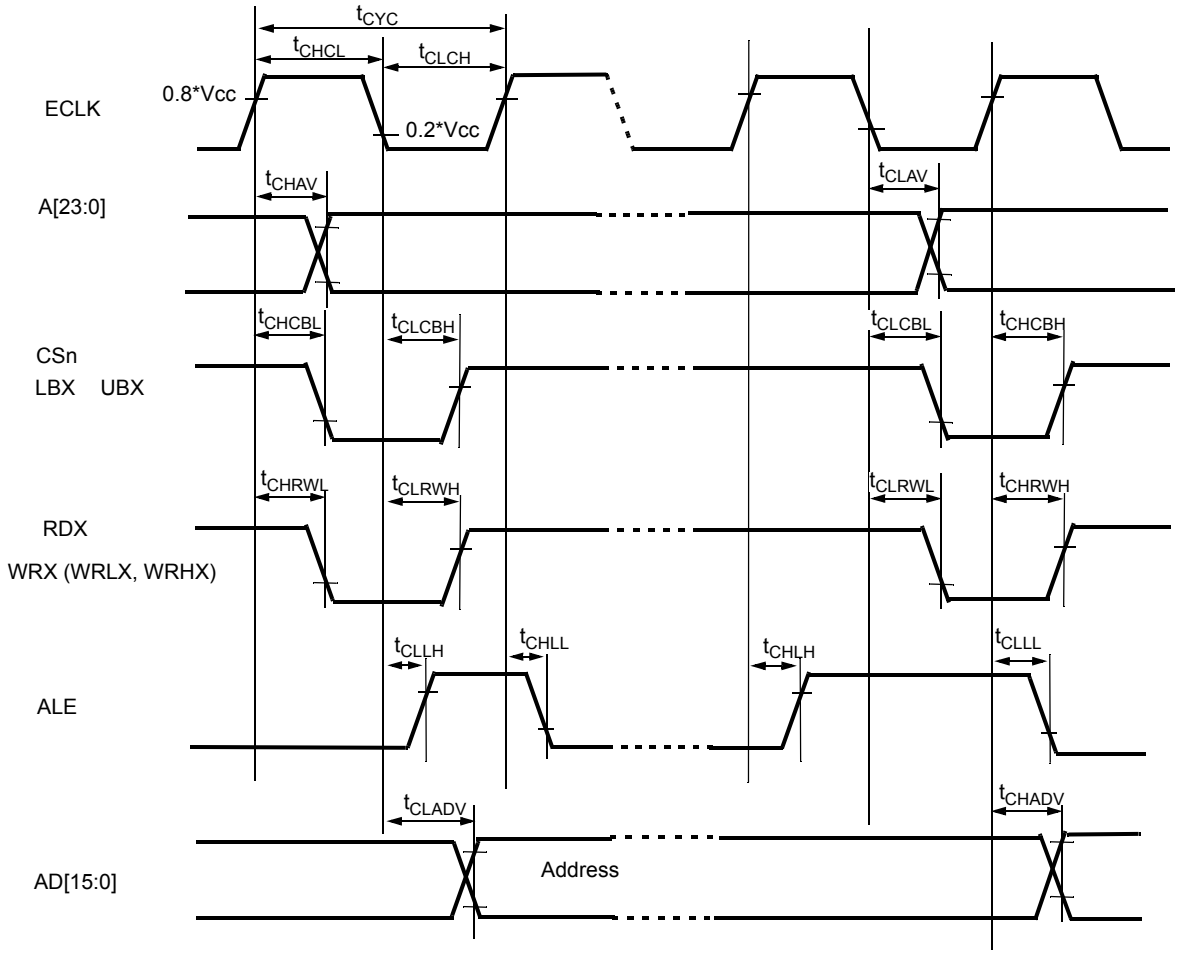
1. Single phase external clock
   - When using a single phase external clock, X0 pin must be driven and X1 pin left open.



($T_A$ = -40°C to 125°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Symbol | Condition (at $T_A$) | | Value | | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Max | Unit | |
| Stop Mode | $I_{CCH}$ | VRCR:LPMB[2:0] = $110_B$ | +25°C | 0.02 | 0.08 | mA | Core voltage at 1.8V |
| | | | +125°C | 0.52 | 2.8 | | |
| | | VRCR:LPMB[2:0] = $000_B$ | +25°C | 0.015 | 0.06 | mA | Core voltage at 1.2V |
| | | | +125°C | 0.4 | 2.3 | | |
| Power supply current for active Low Voltage detector | $I_{CCLVD}$ | Low voltage detector enabled (RCR:LVDE = 1) | +25°C | 90 | 140 | µA | This current must be added to all Power supply currents above |
| | | | +125°C | 100 | 150 | | |
| Clock modulator current | $I_{CCCLOMO}$ | Clock modulator enabled (CMCR:PDX = 1) | - | 3 | 4.5 | mA | Must be added to all current above |
| Flash Write/Erase current | $I_{CCFLASH}$ | Current for one Flash module | - | 15 | 40 | mA | Must be added to all current above |
| Input capacitance | $C_{IN}$ | - | - | 5 | 15 | pF | Other than C, $AV_{CC}$, $AV_{SS}$, AVRH, AVRL, $V_{CC}$, $V_{SS}$ |

*: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.




Refer to the Hardware Manual for detailed Timing Charts

($T_A$ = –40°C to +125°C, $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0.0 V, $IO_{drive}$ = 5mA, $C_L$ = 50pF)

| Parameter | Sym-bol | Pin | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Valid address ⇒ Valid data input (multiplexed) | $t_{AVDV}$ | A[23:16], AD[15:0] | EACL:ACE=0 EBM:NMS=0 | — | $3t_{CYC}$ – 55 | ns | w/o cycle extension |
| | | | EACL:ACE=1 EBM:NMS=0 | — | $4t_{CYC}$ – 55 | | |
| | $t_{AD-VDV}$ | AD[15:0] | EACL:ACE=0 EBM:NMS=0 | — | $5t_{CYC}/2$ – 55 | ns | w/o cycle extension |
| | | | EACL:ACE=1 EBM:NMS=0 | — | $7t_{CYC}/2$ – 55 | | |
| RDX pulse width | $t_{RLRH}$ | RDX | — | 3 $t_{CYC}/2$ – 5 | — | ns | w/o cycle extension |
| RDX ↓ ⇒ Valid data input | $t_{RLDV}$ | RDX, AD[15:0] | — | — | 3 $t_{CYC}/2$ – 50 | ns | w/o cycle extension |
| RDX ↑ ⇒ Data hold time | $t_{RHDX}$ | RDX, AD[15:0] | — | 0 | — | ns | |
| Address valid ⇒ Data hold time | $t_{AXDX}$ | A[23:0], AD[15:0] | — | 0 | — | ns | |
| RDX ↑ ⇒ ALE ↑ time | $t_{RHLH}$ | RDX, ALE | EACL:STS=1 and EACL:ACE=1 | $3t_{CYC}/2$ – 10 | — | ns | |
| | | | other ECL:STS, EACL:ACE setting | $t_{CYC}/2$ – 10 | — | | |
| Valid address ⇒ ECLK ↑ time | $t_{AVCH}$ | A[23:0], ECLK | — | $t_{CYC}$ – 15 | — | ns | |
| | $t_{AD-VCH}$ | AD[15:0], ECLK | | $t_{CYC}/2$ – 15 | — | | |
| RDX ↓ ⇒ ECLK ↑ time | $t_{RLCH}$ | RDX, ECLK | — | $t_{CYC}/2$ – 10 | — | ns | |
| ALE ↓ ⇒ RDX ↓ time | $t_{LLRL}$ | ALE, RDX | EACL:STS=0 | $t_{CYC}/2$ – 10 | — | ns | |
| | | | EACL:STS=1 | – 10 | — | | |
| ECLK↑ ⇒ Valid data input | $t_{CHDV}$ | AD[15:0], ECLK | — | — | $t_{CYC}$ – 50 | ns | |

## 14.5 USB Characteristics

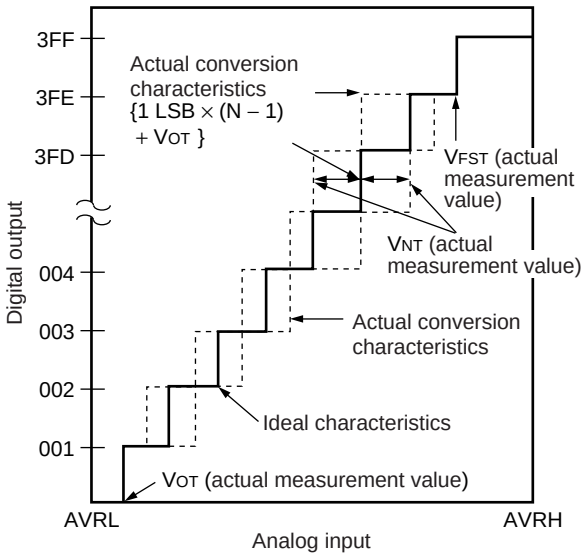
($T_A$ = -40°C to 105°C, $V_{CC}$ = $AV_{CC}$= 3.0V to 5.5V,$V_{SS}$ = $AV_{SS}$ = 0V, $V_{CC3}$ = 3.0V to 3.6V, USB pins UDP and UDM)

| Parameter | | Symbol | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input characteristics | Input High level voltage | $V_{IH}$ | — | 2.0 | $V_{CC}$ + 0.3 | V | *1 |
| | Input Low level voltage | $V_{IL}$ | — | $V_{SS}$ – 0.3 | 0.8 | V | *1 |
| | Differential input sensitivity | $V_{DI}$ | — | 0.2 | — | V | *2 |
| | Differential common mode input voltage | $V_{CM}$ | — | 0.8 | 2.5 | V | *2 |
| Output characteristics | Output High level voltage | $V_{OH}$ | External pull-down resistance = 15 kΩ | 2.8 | 3.6 | V | *3 |
| | Output Low level voltage | $V_{OL}$ | External pull-up resistance = 1.5 kΩ | 0.0 | 0.3 | V | *3 |
| | Crossover voltage | $V_{CRS}$ | — | 1.3 | 2.0 | V | *4 |
| | Rise time | $t_{FR}$ | — | 4 | 20 | nS | *5 |
| | Fall time | $t_{FF}$ | — | 4 | 20 | nS | *5 |
| | Rise/fall time matching | $t_{RFM}$ | — | 90 | 111.11 | % | *5 |
| | Output impedance | $Z_{DRV}$ | — | 28 | 44 | Ω | Including Rs = 27 Ω |
| Input capacitance | Transceiver edge rate control capacitance | $C_{EDGE}$ | — | — | 75 | pF | *6 |
| Series resistance | | $R_S$ | — | 25 | 30 | Ω | Recommended value:27 Ω |

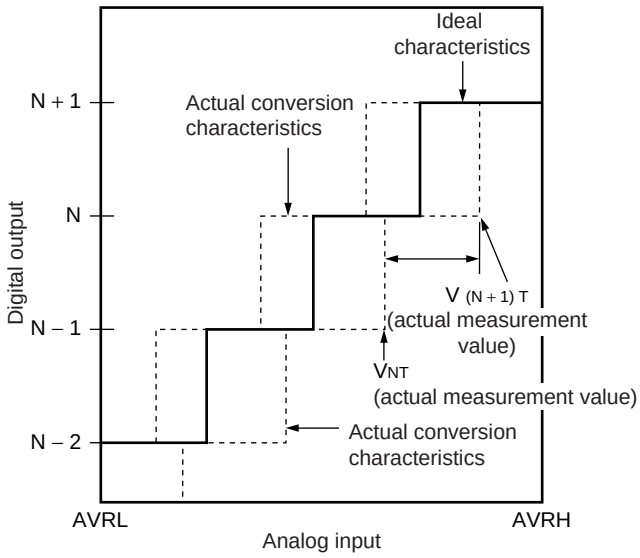
*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within $V_{IL}$ (Max) = 0.8 [V], $V_{IH}$ (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

*(Continued)*

Nonlinearity error




Differential nonlinearity error




$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

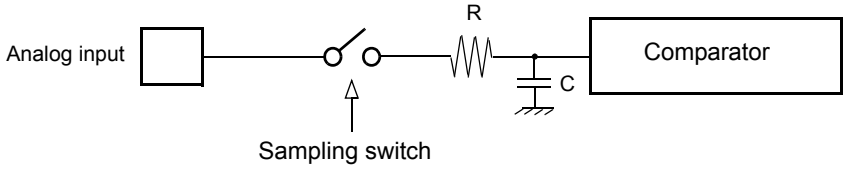
N : A/D converter digital output value
$V_{OT}$ : Voltage at which digital output transits from "$000_H$" to "$001_H$."
$V_{FST}$ : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

## Notes on A/D Converter Section

- About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

### analog input circuit model:

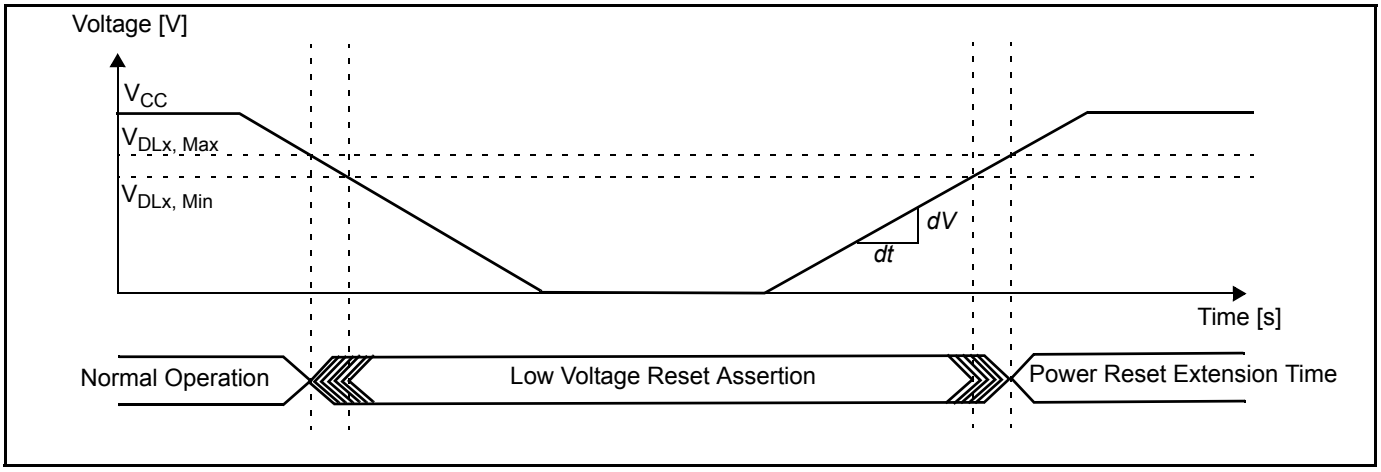



**Reference value:**

- C = 8.5 pF (Max)

### Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



## 14.9 FLASH memory program/erase characteristics

($T_A$ = -40°C to 105°C, $V_{CC}$ = $AV_{CC}$ = 3.0V to 5.5V, $V_{SS}$ = $AV_{SS}$ = 0V)

| Parameter | Value | | | Unit | Remarks |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 0.9 | 3.6 | s | Without erasure pre-programming time |
| Chip erase time | - | n*0.9 | n*3.6 | s | Without erasure pre-programming time (n is the number of Flash sector of the device) |
| Word (16-bit width) programming time | - | 23 | 370 | us | Without overhead time for submitting write command |
| Program/Erase cycle | 10 000 | - | - | cycle | |
| Flash data retention time | 20 | - | - | year | *1 |

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85$^{o}$C)

## 15. Example Characteristics

To be prepared

## 18. Revision History

| Revision | Date | Modification |
|---|---|---|
| Prelim 0.1 | 2007-05-23 | Creation |
| Prelim 0.2 | 2007-08-14 | - information about MB96F338U (with USB function) is added<br>- DMA 8ch --> 16ch<br>- ADC reference switch is removed |
| Prelim 0.3 | 2007-09-11 | - Circuit Type of Device with “U“ suffix is added<br>- Circuit Type diagram: TTL input cell type was changed from NOR to NAND<br>- IO Map, IRQ table are updated<br>- Parallel Programing Flash Memory Control Signals is updated<br>- DC/AC spec of USB I/O is added |
| Prelim 0.4 | 2007-09-24 | - Block diagram for MB96F338U was corrected: USB PB1 -> PB3<br>- IRQ table was modified: Vector number 111 was inserted (reserved)<br>- Pin assignment was corrected: not used resource name was removed |
| Prelim 0.5 | 2007-11-02 | - Internal Max Freq 56MHz --> 48MHz<br>- DMA 12ch --> 10ch<br>- FPT-144P-M12 package was removed |
| Prelim 1 | 2007-12-20 | Update of the block diagram to include USB block.<br>Update DC characteristics to include all USB pins characteristics.<br>IOMAP regenerated.<br>Memory maps and Flash configuration reworked.<br>Typos corrected across the document.<br>Renaming of the Flash banks. |
| Prelim 2 | 2008-02-07 | • Features:<br>- Removed ADC reference switch<br>- changed USB description<br>• Lineup:<br>- option description added<br>- Part number names corrected<br>- Flash B removed<br>- RLT6 added<br>• Block diagrams:<br>- Flash B removed<br>- OUT5_R -> OUT6_R<br>- TX2_R, RX2_R added<br>- SIN2_R, SOT2_R, SCK2_R and SOT9 added<br>- not existing TTGx, TTGx_R and PPGx_R pins deleted<br>- RLT6 added<br>• Pin function description: relocated clock output and CAN pins added<br>• I/O circuit types updated<br>• Memory maps replaced by new standard maps<br>• Parallel Flash programming pinning removed<br>• IOMAP regenerated (naming style changed, all reserved registers added)<br>• DC current limits updated with new setting and corrected frequencies<br>• External bus timings: missing conditions added and readability improved<br>• Alarm comparator spec updated (transition voltages defined)<br>• Ordering information updated<br>• Typos and formatting corrected |

## Document History

| Document Title: MB96330 Series F$^2$MC-16FX 16-bit Proprietary Microcontroller<br>Document Number: 002-04586 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | — | AKIH | 05/23/2007 | Migrated to Cypress and assigned document number 002-04586.<br>No change to document contents or format. |
| *A | 5245336 | AKIH | 05/13/2016 | Updated to Cypress template |