Infineon Technologies - MB96F338USAPMC-GS-N2K5E2 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, UART/USART, USB
Peripherals	DMA, LVD, LVR, POR, PWM, WDT
Number of I/O	120
Program Memory Size	544KB (544K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f338usapmc-gs-n2k5e2

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I^2C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset
- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

4. Pin Function Description

Pin Function description (1 of 3)

Pin name	Feature	Description
ADn	External bus	External bus interface (non multiplexed mode) data input/output. External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus non-multiplexed address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
CKOTXn_R	Clock output function	Relocated Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
FRCKn_R	Free Running Timer	Relocated Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HCONX	USB	USB connection to host or hub
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INn_R	ICU	Relocated Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output

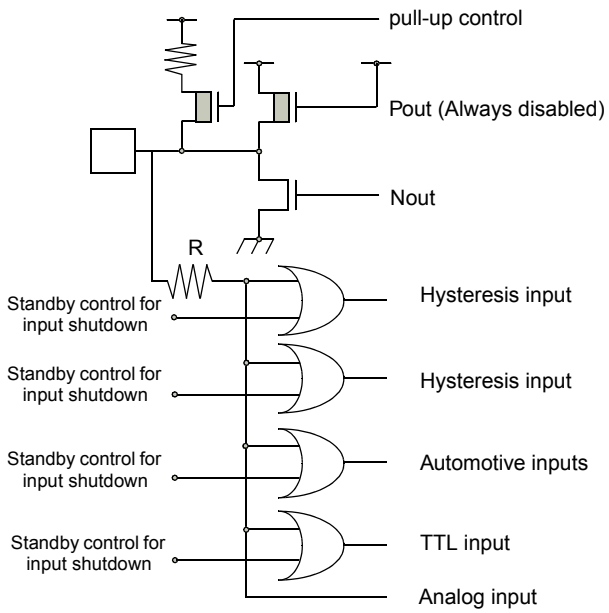
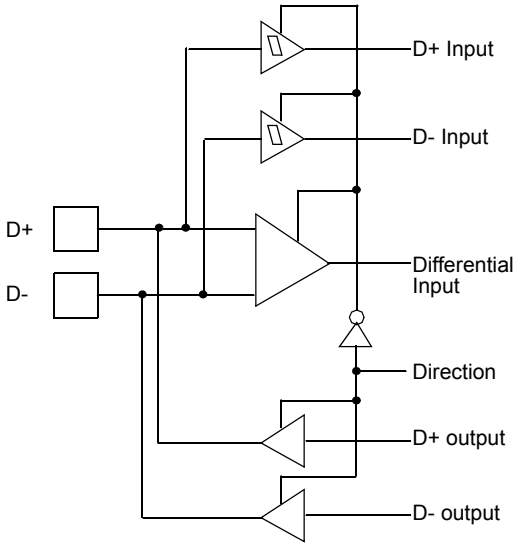
5. Pin Circuit Type

Pin no.	FPT-144P-M08	
	Circuit type *1	
	MB96(F)33xY/R	MB96(F)33xU (USB device)
1	Supply	
2	F	
3 to 21	H	
22 to 25	N	
26 to 35	I	
36, 37	Supply	
38 to 43	I	
44	Supply	
45	G	
46 to 47	Supply	
48 to 67	I	
68	I	O
69	I	Supply (3.3V)
70, 71	I	P
72, 73	Supply	
74 to 76	C	
77, 78	A	
79	Supply	
80, 81	B *2	
80, 81	H *3	
82	E	
83 to 107	H	
108, 109	Supply	
110 to 143	H	
144	Supply	

*1: Please refer to 6.“I/O Circuit Type” for details on the I/O circuit types

*2: Devices with suffix “W”

*3: Devices without suffix “W”

Type	Circuit	Remarks
O		HCONX • Available only for device with suffix “U”
P		USB IO cell: UDP and UDM • Available only for device with suffix “U”

8. RAMSTART/END and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96F336	24KByte	-	$00:11FF_H$	$00:2240_H$	-	-
MB96F338, MB96338	28KByte	4kB	$00:11FF_H$	$00:1240_H$	$01:8000_H$	$01:8FFF_H$

I/O map MB96(F)33x (12 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000382_H	DMA2 - Interrupt select	DISEL2		R/W
000383_H	DMA3 - Interrupt select	DISEL3		R/W
000384_H	DMA4 - Interrupt select	DISEL4		R/W
000385_H	DMA5 - Interrupt select	DISEL5		R/W
000386_H	DMA6 - Interrupt select	DISEL6		R/W
000387_H	DMA7 - Interrupt select	DISEL7		R/W
000388_H	DMA8 - Interrupt select	DISEL8		R/W
000389_H	DMA9 - Interrupt select	DISEL9		R/W
$00038A_H$-$00038F_H$	Reserved			-
000390_H	DMA - Status register low byte	DSRL	DSR	R/W
000391_H	DMA - Status register high byte	DSRH		R/W
000392_H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393_H	DMA - Stop status register high byte	DSSRH		R/W
000394_H	DMA - Enable register low byte	DERL	DER	R/W
000395_H	DMA - Enable register high byte	DERH		R/W
000396_H-$00039F_H$	Reserved			-
$0003A0_H$	Interrupt level register	ILR	ICR	R/W
$0003A1_H$	Interrupt index register	IDX		R/W
$0003A2_H$	Interrupt vector table base register Low	TBRL	TBR	R/W
$0003A3_H$	Interrupt vector table base register High	TBRH		R/W
$0003A4_H$	Delayed Interrupt register	DIRR		R/W
$0003A5_H$	Non Maskable Interrupt register	NMI		R/W
$0003A6_H$-$0003AB_H$	Reserved			-
$0003AC_H$	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
$0003AD_H$	EDSU communication interrupt selection High	EDSU2H		R/W
$0003AE_H$	ROM mirror control register	ROMM		R/W
$0003AF_H$	EDSU configuration register	EDSU		R/W
$0003B0_H$	Memory patch control/status register ch 0/1		PFCS0	R/W
$0003B1_H$	Memory patch control/status register ch 0/1			R/W

I/O map MB96(F)33x (14 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0003D0_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
$0003D1_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
$0003D2_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
$0003D3_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
$0003D4_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
$0003D5_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
$0003D6_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
$0003D7_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
$0003D8_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
$0003D9_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
$0003DA_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
$0003DB_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
$0003DC_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
$0003DD_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
$0003DE_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
$0003DF_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
$0003E0_H$-$0003F0_H$	Reserved			-
$0003F1_H$	Memory Control Status Register A	MCSRA		R/W
$0003F2_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
$0003F3_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
$0003F4_H$-$0003F8_H$	Reserved			-
$0003F9_H$	Flash Memory Write Control register 1	FMWC1		R/W
$0003FA_H$	Flash Memory Write Control register 2	FMWC2		R/W
$0003FB_H$	Flash Memory Write Control register 3	FMWC3		R/W
$0003FC_H$	Flash Memory Write Control register 4	FMWC4		R/W
$0003FD_H$	Flash Memory Write Control register 5	FMWC5		R/W
$0003FE_H$-$0003FF_H$	Reserved			-
000400_H	Standby Mode control register	SMCR		R/W
000401_H	Clock select register	CKSR		R/W

I/O map MB96(F)33x (19 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000490_H	Reserved			-
000491_H	I/O Port P17 - Port Output Drive Register	PODR17		R/W
000492_H-$00049B_H$	Reserved			-
$00049C_H$	I/O Port P08 - Port High Drive Register	PHDR08		R/W
$00049D_H$	I/O Port P09 - Port High Drive Register	PHDR09		R/W
$00049E_H$	I/O Port P10 - Port High Drive Register	PHDR10		R/W
$00049F_H$-$0004A7_H$	Reserved			-
$0004A8_H$	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
$0004A9_H$	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
$0004AA_H$	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
$0004AB_H$	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
$0004AC_H$	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
$0004AD_H$	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
$0004AE_H$	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
$0004AF_H$	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
$0004B0_H$	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
$0004B1_H$	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
$0004B2_H$	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
$0004B3_H$	I/O Port P11 - Pull-Up resistor Control Register	PUCR11		R/W
$0004B4_H$	I/O Port P12 - Pull-Up resistor Control Register	PUCR12		R/W
$0004B5_H$	I/O Port P13 - Pull-Up resistor Control Register	PUCR13		R/W
$0004B6_H$	I/O Port P14 - Pull-Up resistor Control Register	PUCR14		R/W
$0004B7_H$	I/O Port P15 - Pull-Up resistor Control Register	PUCR15		R/W
$0004B8_H$	Reserved			-
$0004B9_H$	I/O Port P17 - Pull-Up resistor Control Register	PUCR17		R/W
$0004BA_H$-$0004BB_H$	Reserved			-
$0004BC_H$	I/O Port P00 - External Pin State Register	EPSR00		R
$0004BD_H$	I/O Port P01 - External Pin State Register	EPSR01		R
$0004BE_H$	I/O Port P02 - External Pin State Register	EPSR02		R

I/O map MB96(F)33x (21 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0004DE_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
$0004DF_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
$0004E0_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
$0004E1_H$	RTC - Sub Second Register M	WTBRH0		R/W
$0004E2_H$	RTC - Sub-Second Register H	WTBR1		R/W
$0004E3_H$	RTC - Second Register	WTSR		R/W
$0004E4_H$	RTC - Minutes	WTMR		R/W
$0004E5_H$	RTC - Hour	WTHR		R/W
$0004E6_H$	RTC - Timer Control Extended Register	WTCER		R/W
$0004E7_H$	RTC - Clock select register	WTCKSR		R/W
$0004E8_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
$0004E9_H$	RTC - Timer Control Register High	WTCRH		R/W
$0004EA_H$	CAL - Calibration unit Control register	CUCR		R/W
$0004EB_H$	Reserved			-
$0004EC_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
$0004ED_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
$0004EE_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
$0004EF_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
$0004F0_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
$0004F1_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
$0004F2_H$-$0004F9_H$	Reserved			-
$0004FA_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
$0004FB_H$-$0004FF_H$	Reserved			-
000500_H	FRT2 - Data register of free-running timer		TCDT2	R/W
000501_H	FRT2 - Data register of free-running timer			R/W
000502_H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503_H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504_H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505_H	FRT3 - Data register of free-running timer			R/W

I/O map MB96(F)33x (29 of 40)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
$0006AA_H$	USB - Host EOF Setting Register Low	HEOFL0	HEOF0	R/W
$0006AB_H$	USB - Host EOF Setting Register High	HEOFH0		R/W
$0006AC_H$	USB - Host Frame Register Low	HFRAMEL0	HFRAME0	R/W
$0006AD_H$	USB - Host Frame Register High	HFRAMEH0		R/W
$0006AE_H$	USB - Host Token End Point Register	HTOKEN0		R/W
$0006AF_H$	Reserved			-
$0006B0_H$	USB - UDC Control Register	UDCC0		R/W
$0006B1_H$	Reserved			-
$0006B2_H$	USB - EP0 Control Register Low	EP0CL0	EP0C0	R/W
$0006B3_H$	USB - EP0 Control Register High	EP0CH0		R/W
$0006B4_H$	USB - EP1 Control Register Low	EP1CL0	EP1C0	R/W
$0006B5_H$	USB - EP1 Control Register High - non public	EP1CH0		R/W
$0006B6_H$	USB - EP2 Control Register Low	EP2CL0	EP2C0	R/W
$0006B7_H$	USB - EP2 Control Register High	EP2CH0		R/W
$0006B8_H$	USB - EP3 Control Register Low	EP3CL0	EP3C0	R/W
$0006B9_H$	USB - EP3 Control Register High	EP3CH0		R/W
$0006BA_H$	USB - EP4 Control Register Low	EP4CL0	EP4C0	R/W
$0006BB_H$	USB - EP4 Control Register High	EP4CH0		R/W
$0006BC_H$	USB - EP5 Control Register Low	EP5CL0	EP5C0	R/W
$0006BD_H$	USB - EP5 Control Register High	EP5CH0		R/W
$0006BE_H$	USB - Timer Stamp Register Low	TMSPL0	TMSP0	R/W
$0006BF_H$	USB - Timer Stamp Register High	TMSPH0		R/W
$0006C0_H$	USB - UDC Status Register	UDCS0		R/W
$0006C1_H$	USB - UDC Interrupt Enable Register	UDCIE0		R/W
$0006C2_H$	USB - EP0I Status Register Low	EP0ISL0	EP0IS0	W
$0006C3_H$	USB - EP0I Status Register High	EP0ISH0		R/W
$0006C4_H$	USB - EP0O Status Register Low	EP0OSL0	EP0OS0	R/W
$0006C5_H$	USB - EP0O Status Register High	EP0OSH0		R/W
$0006C6_H$	USB - EP1 Status Register Low	EP1SL0	EP1S0	R/W
$0006C7_H$	USB - EP1 Status Register High	EP1SH0		R/W

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
USB power supply voltage	V_{CC3}	3.0	3.3	3.6	V	USB device only
Smoothing capacitor at C pin	C_S	4.7	-	10	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz, CLKP3 = 48MHz	+25°C	39	47	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 0 Flash/ROM wait states
			+125°C	40	50		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	45	57	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 2 Flash/ROM wait states
			+125°C	46	60		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1/3 = 48MHz, CLKP2 = 24MHz	+25°C	56	68	mA	CLKRC and CLKSC stopped. Core voltage at 1.9V 1 Flash/ROM wait state
			+125°C	57	71		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 4MHz	+25°C	5	6	mA	CLKPLL, CLKSC and CLKRC stopped 1 Flash/ROM wait state
			+125°C	5.6	9		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 2MHz	+25°C	2.9	4	mA	CLKMC, CLKPLL and CLKSC stopped 1 Flash/ROM wait state
			+125°C	3.5	6.5		
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 0	+25°C	0.4	0.6	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode 1 Flash/ROM wait state
			+125°C	0.9	3.5		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 100kHz, SMCR:LPMS = 1	+25°C	0.15	0.25	mA	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.65	3.2		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2/3 = 32kHz	+25°C	0.1	0.2	mA	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed. 1 Flash/ROM wait state
			+125°C	0.6	3		

External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

Basic Timing

(T_A = –40°C to +125°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time (non-multiplexed)	t_{CHAV}	A[23:0], ECLK	EBM:NMS=1	-15	15	ns	
	t_{CLAV}			-15	15		
ECLK → address valid time (multiplexed)	t_{CHAV}	A[23:16], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	EBM:NMS=0	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = −40°C to +125°C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width (multiplexed)	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	EBM:NMS = 0
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address ⇒ ALE ↓ time (multiplexed)	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE ↓ ⇒ Address valid time (multiplexed)	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		
Valid address ⇒ RDX ↓ time (non-multiplexed)	t_{AVRL}	RDX, A[23:0]	EBM:NMS= 1	$t_{CYC}/2 - 20$	—	ns	
Valid address ⇒ RDX ↓ time (multiplexed)	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0 EBM:NMS=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0 EBM:NMS=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1 EBM:NMS=0	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input (non-multiplexed)	t_{AVDV}	A[23:0], AD[15:0]	EBM:NMS= 1	—	$2t_{CYC} - 60$	ns	w/o cycle extension

14.5 USB Characteristics

(T_A = -40°C to 105°C, V_{CC} = AV_{CC}= 3.0V to 5.5V,V_{SS} = AV_{SS} = 0V, V_{CC3} = 3.0V to 3.6V, USB pins UDP and UDM)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Input characteristics	Input High level voltage	V_{IH}	—	2.0	V_{CC} + 0.3	V	*1
	Input Low level voltage	V_{IL}	—	V_{SS} – 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}	—	0.2	—	V	*2
	Differential common mode input voltage	V_{CM}	—	0.8	2.5	V	*2
Output characteristics	Output High level voltage	V_{OH}	External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output Low level voltage	V_{OL}	External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}	—	1.3	2.0	V	*4
	Rise time	t_{FR}	—	4	20	nS	*5
	Fall time	t_{FF}	—	4	20	nS	*5
	Rise/fall time matching	t_{RFM}	—	90	111.11	%	*5
	Output impedance	Z_{DRV}	—	28	44	Ω	Including Rs = 27 Ω
Input capacitance	Transceiver edge rate control capacitance	C_{EDGE}	—	—	75	pF	*6
Series resistance		R_S	—	25	30	Ω	Recommended value:27 Ω

*1 : The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 [V], V_{IH} (Min) = 2.0 [V] (TTL input standard).
There are some hystereses to lower noise sensitivity.

(Continued)

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

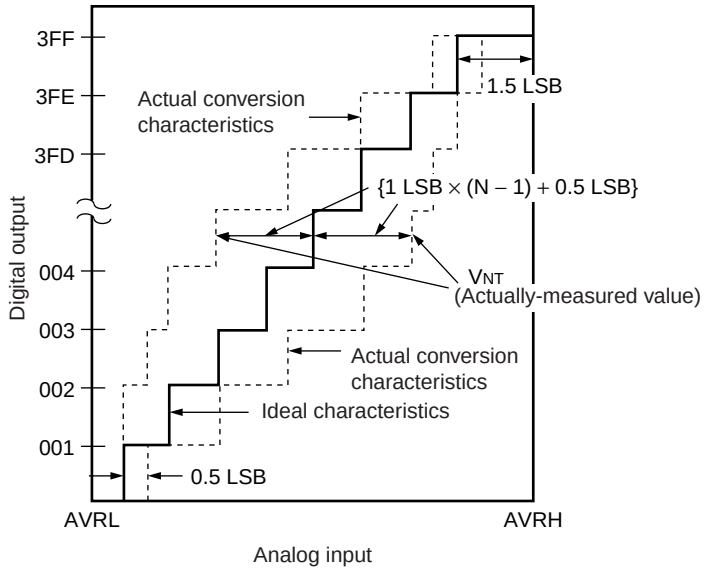
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\ [V]$$

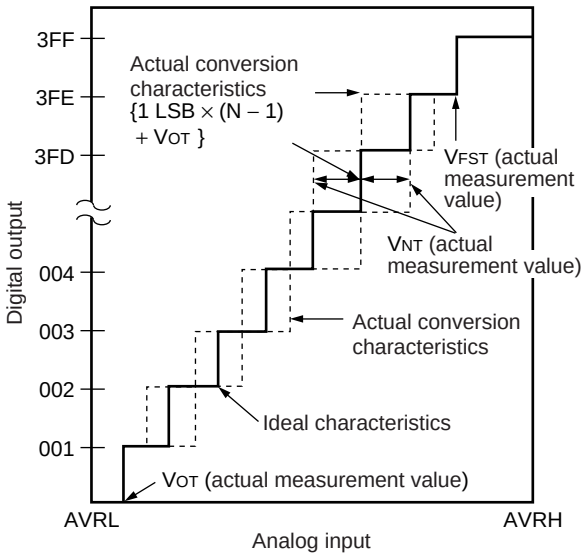
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

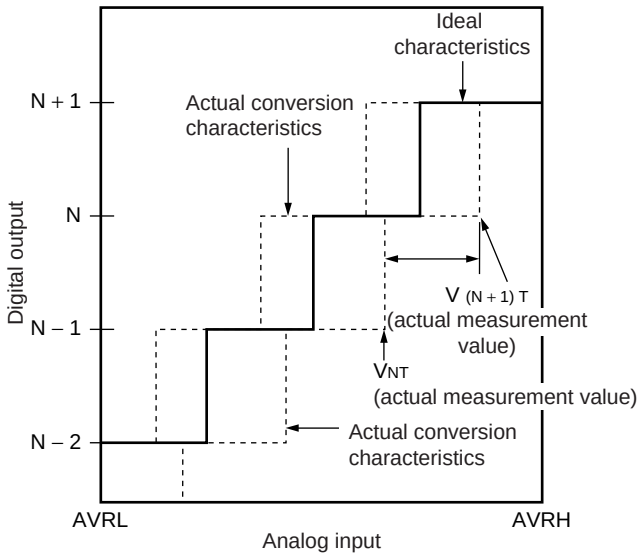
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

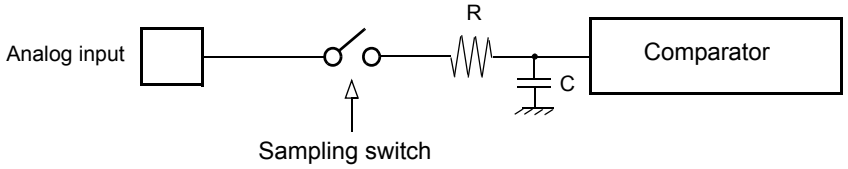
N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

Notes on A/D Converter Section

- About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

analog input circuit model:



Reference value:

- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = $7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \leq AV_{cc} \leq 5.5$

T_{samp} [min] = $7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \leq AV_{cc} \leq 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

15. Example Characteristics

To be prepared

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*A	5245336	AKIH	05/13/2016	Updated to Cypress template