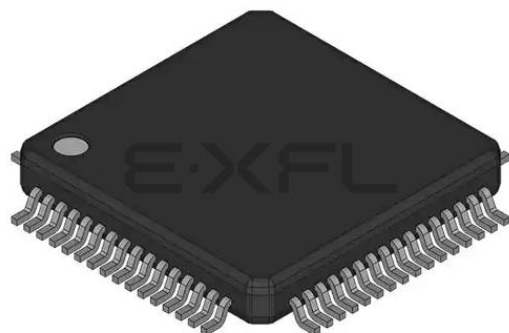


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Details

Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 2x12b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08lc36lh

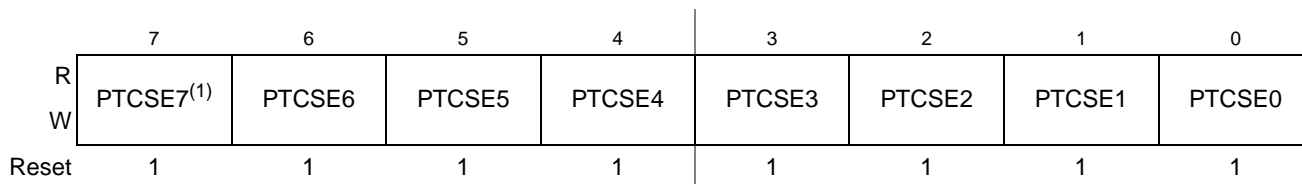


Figure 6-24. Slew Rate Control Enable for Port C (PTCSE)

1. PTCSE7 has no effect on the input-only PTC7 pin.

3 Information removed from Figure 6-25, Output Drive Strength Select (PTCDS)

Please remove the footnote 2 under Figure 6-25, Output Slew Rate Control Enable (PTCSE).

The note says, “PTCDD6 has no effect on the output-only PTC6 pin.”

The figure will now look like this:

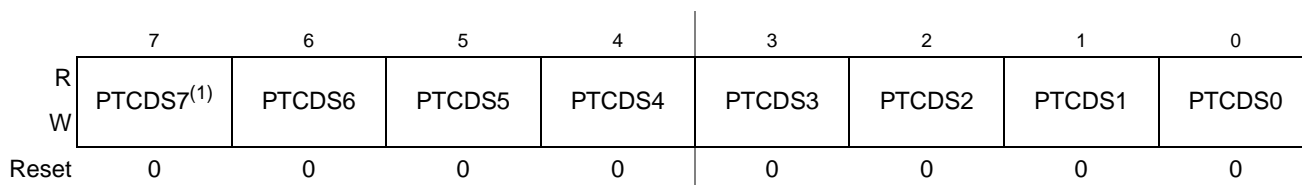


Figure 6-25. Drive Strength Selection for Port C (PTCDS)

1. PTCDS7 has no effect on the input-only PTC7 pin.

4 New information added to Table A-5

Please replace the I_{OZ} row of Table A-5 with this row of the table below.

Table A-5 DC Characteristics
(Temperature Range = -40 to 85°C Ambient)

Parameter	Symbol	Min	Typ ⁽¹⁾	Max	Unit
High impedance (off-state) leakage current (per pin) V _{in} = V _{DD} or V _{SS} , all input/output (all except PTC7) V _{in} = V _{DD} or V _{SS} , (PTC7 only)	I _{OZ}	—	0.025 0.025	1 3	μA

1. Typicals are measured at 25°C.

Section Number	Title	Page
13.5	Functional Description	244
13.5.1	SPI Clock Formats	244
13.5.2	SPI Interrupts	247
13.5.3	Mode Fault Detection	247

Chapter 14 Inter-Integrated Circuit (S08IICV1)

14.1	Introduction	249
14.1.1	Features	251
14.1.2	Modes of Operation	251
14.1.3	Block Diagram	252
14.2	External Signal Description	252
14.2.1	SCL — Serial Clock Line	252
14.2.2	SDA — Serial Data Line	252
14.3	Register Definition	252
14.3.1	IIC Address Register (IICA)	253
14.3.2	IIC Frequency Divider Register (IICF)	253
14.3.3	IIC Control Register (IICC)	256
14.3.4	IIC Status Register (IICS)	257
14.3.5	IIC Data I/O Register (IICD)	258
14.4	Functional Description	259
14.4.1	IIC Protocol	259
14.4.1.1	START Signal	260
14.4.1.2	Slave Address Transmission	260
14.4.1.3	Data Transfer	260
14.4.1.4	STOP Signal	261
14.4.1.5	Repeated START Signal	261
14.4.1.6	Arbitration Procedure	261
14.4.1.7	Clock Synchronization	261
14.4.1.8	Handshaking	262
14.4.1.9	Clock Stretching	262
14.5	Resets	262
14.6	Interrupts	262
14.6.1	Byte Transfer Interrupt	263
14.6.2	Address Detect Interrupt	263
14.6.3	Arbitration Lost Interrupt	263
14.7	Initialization/Application Information	264

Chapter 15 Analog-to-Digital Converter (S08ADC12V1)

15.1	Introduction	267
15.1.1	ADC Configuration Information	267
15.1.1.1	Channel Assignments	267
15.1.1.2	Alternate Clock	268

before writing to the PPDACK bit. If the port registers are not restored from RAM before writing to PPDACK, then the pins will switch to their reset states when PPDACK is written.

For pins that were configured as peripheral I/O, the user must reconfigure the peripheral module that interfaces to the pin before writing to the PPDACK bit. If the peripheral module is not enabled before writing to PPDACK, the pins will be controlled by their associated port control registers when the I/O latches are opened.

3.6.3 Stop1 Mode

Stop1 mode is entered by executing a STOP instruction under the conditions as shown in Table 3-1. Most of the internal circuitry of the MCU is powered off in stop1, providing the lowest possible standby current. Upon entering stop1, all I/O pins automatically transition to their default reset states.

Exit from stop1 is performed by asserting the wake-up pins or $\overline{\text{RESET}}$ or IRQ.

NOTE

IRQ always functions as an active-low wakeup input when the MCU is in stop1, regardless of how the pin is configured before entering stop1.

In addition, the real-time interrupt (RTI) can wake the MCU from stop1 if enabled.

Upon wake-up from stop1 mode, the MCU starts up as from a power-on reset (POR):

- All module control and status registers are reset
- The LVD reset function is enabled and the MCU remains in the reset state if V_{DD} is below the LVD trip point (low trip point selected due to POR)
- The CPU takes the reset vector

In addition to the above, upon waking up from stop1, the PDF bit in SPMSC2 is set. This flag is used to direct user code to go to a stop1 recovery routine. PDF remains set until a 1 is written to PPDACK in SPMSC2.

3.6.4 On-Chip Peripheral Modules in Stop Modes

When the MCU enters any stop mode, system clocks to the internal peripheral modules are stopped. Even in the exception case (ENBDM = 1), where clocks to the background debug logic continue to operate, clocks to the peripheral systems are halted to reduce power consumption. Refer to Section 3.6.3, “Stop1 Mode,” Section 3.6.2, “Stop2 Mode,” and Section 3.6.1, “Stop3 Mode,” for specific information on system behavior in stop modes.

6.2.2 Port A Control Registers

Associated with the parallel I/O ports is a set of registers located in the high page register space that operate independently of the parallel I/O registers. These registers are used to control pullups, slew rate, and drive strength for the associated pins and may be used in conjunction with the peripheral functions on these pins for most modules.

The pins associated with port A are controlled by the registers in this section. These registers control the pin pullup, slew rate and drive strength of the port A pins independent of the parallel I/O registers.

6.2.2.1 Internal Pullup Enable (PTAPE)

An internal pullup device can be enabled for each port pin by setting the corresponding bit in the pullup enable register (PTAPEn). The pullup device is disabled if the pin is configured as an output by the parallel I/O control logic or any shared peripheral function regardless of the state of the corresponding pullup enable register bit. The pullup device is also disabled if the pin is controlled by an analog function.

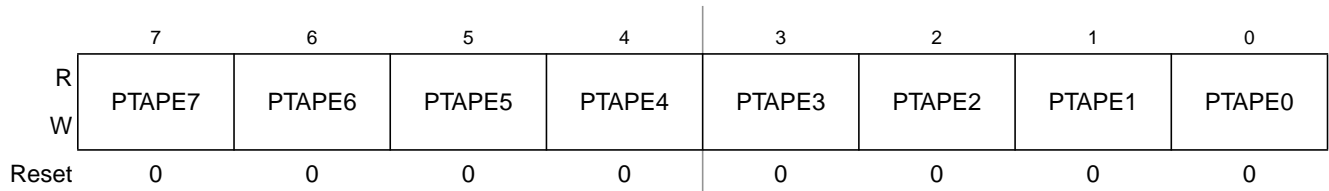


Figure 6-7. Pullup Enable for Port A (PTAPE)

Table 6-3. PTAPE Field Descriptions

Field	Description
7:0 PTAPE[7:0]	<p>Pullup Enable for Port A Bits — For port A pins that are inputs, these read/write control bits determine whether internal pullup devices are enabled provided the corresponding PTADDn is 0. For port A pins that are configured as outputs, these bits are ignored and the internal pullup devices are disabled. When any of bits 7 through 0 of port A are enabled as KBI inputs and are configured to detect rising edges/high levels, the pullup enable bits enable pulldown rather than pullup devices.</p> <p>0 Internal pullup device disabled. 1 Internal pullup device enabled.</p>

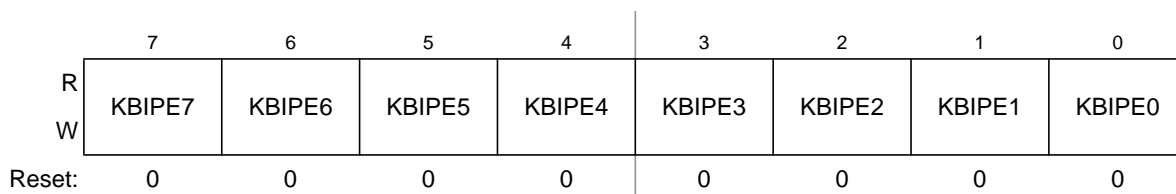


Figure 7-4. KBIx Pin Enable Register

Table 7-3. KBIxPE Register Field Descriptions

Field	Description
7:0 KBIPE _n	Keyboard Pin Enables — Each of the KBIPE _n bits enable the corresponding keyboard interrupt pin. 0 Pin not enabled as keyboard interrupt. 1 Pin enabled as keyboard interrupt.

7.3.3 KBIx Edge Select Register (KBIxES)

KBIxES contains the edge select control bits.

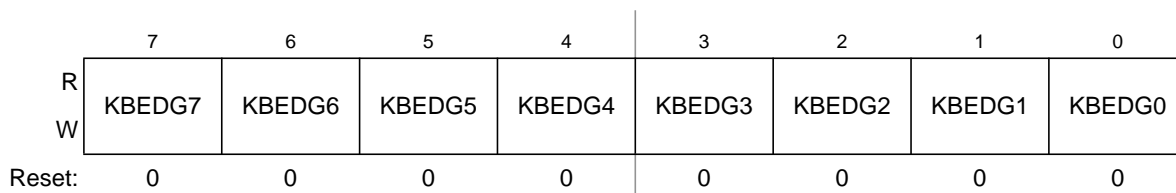


Figure 7-5. KBIx Edge Select Register

Table 7-4. KBIxES Register Field Descriptions

Field	Description
7:0 KBEDG _n	Keyboard Edge Selects — Each of the KBEDG _n bits selects the falling edge/low level or rising edge/high level function of the corresponding pin). 0 Falling edge/low level. 1 Rising edge/high level.

7.4 Functional Description

This on-chip peripheral module is called a keyboard interrupt (KBI) module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking the MCU from stop or wait low-power modes.

The KBI module allows up to eight pins to act as additional interrupt sources. Writing to the KBIPE_n bits in the keyboard interrupt pin enable register (KBIxPE) independently enables or disables each KBI pin. Each KBI pin can be configured as edge sensitive or edge and level sensitive based on the KBMOD bit in the keyboard interrupt status and control register (KBIxSC). Edge sensitive can be software programmed to be either falling or rising; the level can be either low or high. The polarity of the edge or edge and level sensitivity is selected using the KBEDG_n bits in the keyboard interrupt edge select register (KBIxES).

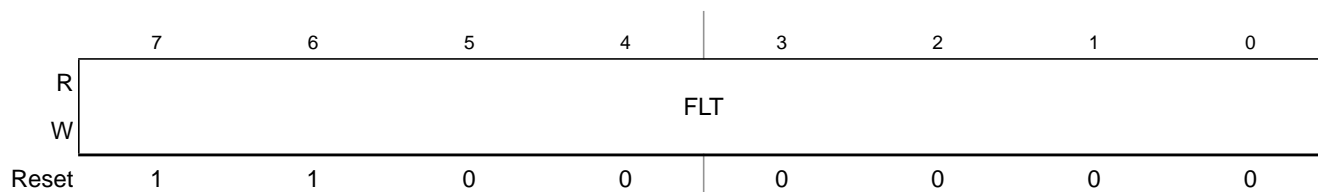
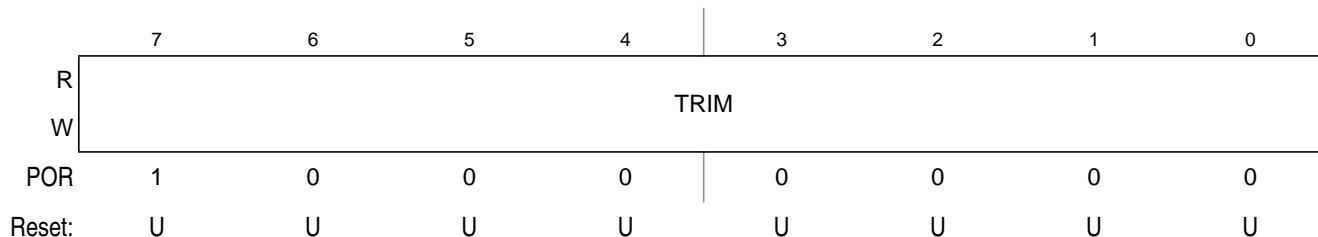


Figure 10-11. ICG Lower Filter Register (ICGFLTL)

Table 10-6. ICGFLTL Register Field Descriptions

Field	Description
7:0 FLT	Filter Value — The FLT bits indicate the current filter value, which controls the DCO frequency. The FLT bits are read only except when the CLKS bits are programmed to self-clocked mode (CLKS = 00). In self-clocked mode, any write to ICGFLTU updates the current 12-bit filter value. Writes to the ICGFLTU register will not affect FLT if a previous latch sequence is not complete. The filter registers show the filter value (FLT).

10.4.6 ICG Trim Register (ICGTRM)



U = Unaffected by MCU reset

Figure 10-12. ICG Trim Register (ICGTRM)

Table 10-7. ICGTRM Register Field Descriptions

Field	Description
7 TRIM	ICG Trim Setting — The TRIM bits control the internal reference generator frequency. They allow a $\pm 25\%$ adjustment of the nominal (POR) period. The bit's effect on period is binary weighted (i.e., bit 1 will adjust twice as much as changing bit 0). Increasing the binary value in TRIM will increase the period and decreasing the value will decrease the period.

10.5 Functional Description

This section provides a functional description of each of the five operating modes of the ICG. Also discussed are the loss of clock and loss of lock errors and requirements for entry into each mode. The ICG is very flexible, and in some configurations, it is possible to exceed certain clock specifications. When using the FLL, configure the ICG so that the frequency of ICGDCLK does not exceed its maximum value to ensure proper MCU operation.

10.5.1 Off Mode (Off)

Normally when the CPU enters stop mode, the ICG will cease all clock activity and is in the off state. However there are two cases to consider when clock activity continues while the CPU is in stop mode,

10.5.1.1 BDM Active

When the BDM is enabled, the ICG continues activity as originally programmed. This allows access to memory and control registers via the BDC controller.

10.5.1.2 OSCSTEN Bit Set

When the oscillator is enabled in stop mode ($OSCSTEN = 1$), the individual clock generators are enabled but the clock feed to the rest of the MCU is turned off. This option is provided to avoid long oscillator startup times if necessary, or to run the RTI from the oscillator during stop3.

10.5.1.3 Stop/Off Mode Recovery

Upon the CPU exiting stop mode due to an interrupt, the previously set control bits are valid and the system clock feed resumes. If FEE is selected, the ICG will source the internal reference until the external clock is stable. If FBE is selected, the ICG will wait for the external clock to stabilize before enabling ICGOUT.

Upon the CPU exiting stop mode due to a reset, the previously set ICG control bits are ignored and the default reset values applied. Therefore the ICG will exit stop in SCM mode configured for an approximately 8 MHz DCO output (4 MHz bus clock) with trim value maintained. If using a crystal, 4096 clocks are detected prior to engaging ICGERCLK. This is incorporated in crystal start-up time.

10.5.2 Self-Clocked Mode (SCM)

Self-clocked mode (SCM) is the default mode of operation and is entered when any of the following conditions occur:

- After any reset.
- Exiting from off mode when $CLKS$ does not equal 10. If $CLKS = X1$, the ICG enters this state temporarily until the DCO is stable ($DCOS = 1$).
- $CLKS$ bits are written from X1 to 00.
- $CLKS = 1X$ and ICGERCLK is not detected (both $ERCS = 0$ and $LOCS = 1$).

In this state, the FLL loop is open. The DCO is on, and the output clock signal ICGOUT frequency is given by $f_{ICGDCLK} / R$. The ICGDCLK frequency can be varied from 8 MHz to 40 MHz by writing a new value into the filter registers (ICGFLTH and ICGFLTL). This is the only mode in which the filter registers can be written.

If this mode is entered due to a reset, $f_{ICGDCLK}$ will default to f_{Self_reset} which is nominally 8 MHz. If this mode is entered from FLL engaged internal, $f_{ICGDCLK}$ will maintain the previous frequency. If this mode is entered from FLL engaged external (either by programming $CLKS$ or due to a loss of external reference clock), $f_{ICGDCLK}$ will maintain the previous frequency, but ICGOUT will double if the FLL was unlocked. If this mode is entered from off mode, $f_{ICGDCLK}$ will be equal to the frequency of ICGDCLK before

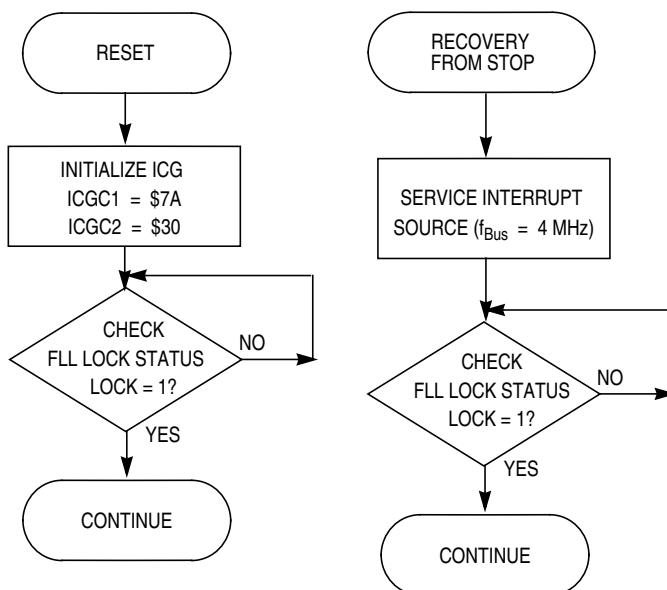


Figure 10-15. ICG Initialization and Stop Recovery for Example #2

Chapter 11

Timer Pulse-Width Modulator (S08TPMV2)

11.1 Introduction

The TPM uses one input/output (I/O) pin per channel, TPMxCHn where x is the TPM number (for example, 1 or 2) and n is the channel number (for example, 0–4). The TPM shares its I/O pins with general-purpose I/O port pins (refer to the Pins and Connections chapter for more information).

The MC9S08LC60 Series has two TPM modules

Figure 11-1 shows the MC9S08LC60 Series block diagram with the TPMs highlighted.

Table 11-2. TPM Clock Source Selection

CLKSB:CLKSA	TPM Clock Source to Prescaler Input
0:0	No clock selected (TPMx disabled)
0:1	Bus rate clock (BUSCLK)
1:0	Fixed system clock (XCLK)
1:1	External source (TPMxCLK) ^{1,2}

- ¹ The maximum frequency that is allowed as an external clock is one-fourth of the bus frequency.
- ² If the external clock input is shared with channel n and is selected as the TPM clock source, the corresponding ELSnB:ELSnA control bits should be set to 0:0 so channel n does not try to use the same pin for a conflicting function.

Table 11-3. Prescale Divisor Selection

PS2:PS1:PS0	TPM Clock Source Divided-By
0:0:0	1
0:0:1	2
0:1:0	4
0:1:1	8
1:0:0	16
1:0:1	32
1:1:0	64
1:1:1	128

11.3.2 Timer x Counter Registers (TPMxCNTH:TPMxCNTL)

The two read-only TPM counter registers contain the high and low bytes of the value in the TPM counter. Reading either byte (TPMxCNTH or TPMxCNTL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This allows coherent 16-bit reads in either order. The coherency mechanism is automatically restarted by an MCU reset, a write of any value to TPMxCNTH or TPMxCNTL, or any write to the timer status/control register (TPMxSC).

Reset clears the TPM counter registers.

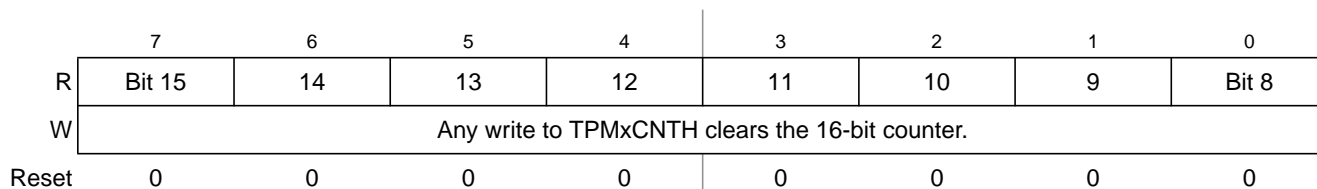


Figure 11-4. Timer x Counter Register High (TPMxCNTH)

Table 11-5. Mode, Edge, and Level Selection

CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration
X	XX	00		Pin not used for TPM channel; use as an external clock for the TPM or revert to general-purpose I/O
0	00	01	Input capture	Capture on rising edge only
		10		Capture on falling edge only
		11		Capture on rising or falling edge
	01	00	Output compare	Software compare only
		01		Toggle output on compare
		10		Clear output on compare
1X	10	Edge-aligned PWM	High-true pulses (clear output on compare)	
	X1		Low-true pulses (set output on compare)	
1	XX	10	Center-aligned PWM	High-true pulses (clear output on compare-up)
		X1		Low-true pulses (set output on compare-up)

If the associated port pin is not stable for at least two bus clock cycles before changing to input capture mode, it is possible to get an unexpected indication of an edge trigger. Typically, a program would clear status flags after changing channel configuration bits and before enabling channel interrupts or using the status flags to avoid any unexpected behavior.

11.3.5 Timer x Channel Value Registers (TPMxCnVH:TPMxCnVL)

These read/write registers contain the captured TPM counter value of the input capture function or the output compare value for the output compare or PWM functions. The channel value registers are cleared by reset.

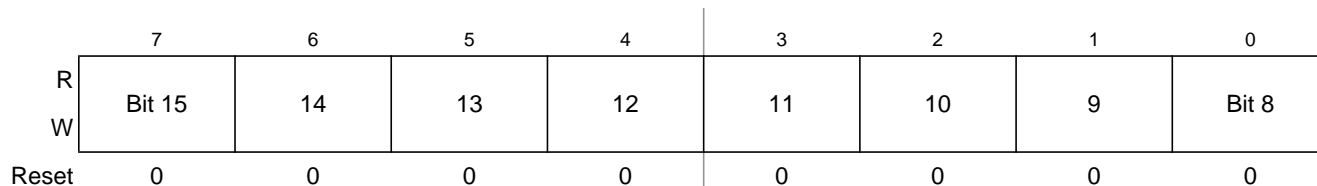


Figure 11-9. Timer x Channel Value Register High (TPMxCnVH)

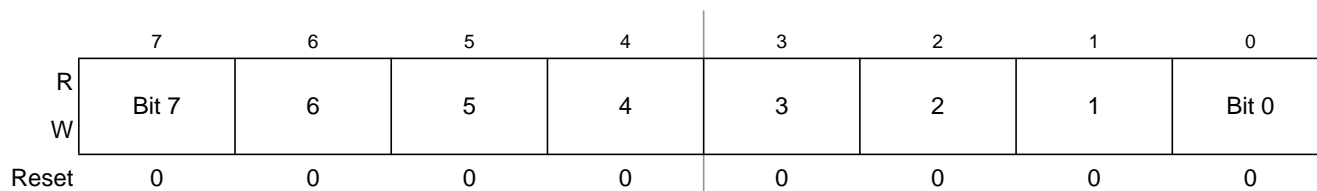


Figure 11-10. Timer Channel Value Register Low (TPMxCnVL)

In input capture mode, reading either byte (TPMxCnVH or TPMxCnVL) latches the contents of both bytes into a buffer where they remain latched until the other byte is read. This latching mechanism also resets (becomes unlatched) when the TPMxCnSC register is written.

masked by local interrupt enable masks. The flags can still be polled by software when the local masks are cleared to disable generation of hardware interrupt requests.

The SCI transmitter has two status flags that optionally can generate hardware interrupt requests. Transmit data register empty (TDRE) indicates when there is room in the transmit data buffer to write another transmit character to SCID. If the transmit interrupt enable (TIE) bit is set, a hardware interrupt will be requested whenever $TDRE = 1$. Transmit complete (TC) indicates that the transmitter is finished transmitting all data, preamble, and break characters and is idle with TxD1 high. This flag is often used in systems with modems to determine when it is safe to turn off the modem. If the transmit complete interrupt enable (TCIE) bit is set, a hardware interrupt will be requested whenever $TC = 1$. Instead of hardware interrupts, software polling may be used to monitor the TDRE and TC status flags if the corresponding TIE or TCIE local interrupt masks are 0s.

When a program detects that the receive data register is full ($RDRF = 1$), it gets the data from the receive data register by reading SCID. The RDRF flag is cleared by reading SCIS1 while $RDRF = 1$ and then reading SCID.

When polling is used, this sequence is naturally satisfied in the normal course of the user program. If hardware interrupts are used, SCIS1 must be read in the interrupt service routine (ISR). Normally, this is done in the ISR anyway to check for receive errors, so the sequence is automatically satisfied.

The IDLE status flag includes logic that prevents it from getting set repeatedly when the RxD1 line remains idle for an extended period of time. IDLE is cleared by reading SCIS1 while $IDLE = 1$ and then reading SCID. After IDLE has been cleared, it cannot become set again until the receiver has received at least one new character and has set RDRF.

If the associated error was detected in the received character that caused RDRF to be set, the error flags — noise flag (NF), framing error (FE), and parity error flag (PF) — get set at the same time as RDRF. These flags are not set in overrun cases.

If RDRF was already set when a new character is ready to be transferred from the receive shifter to the receive data buffer, the overrun (OR) flag gets set instead and the data and any associated NF, FE, or PF condition is lost.

12.4 Additional SCI Functions

The following sections describe additional SCI functions.

12.4.1 8- and 9-Bit Data Modes

The SCI system (transmitter and receiver) can be configured to operate in 9-bit data mode by setting the M control bit in SCIC1. In 9-bit mode, there is a ninth data bit to the left of the MSB of the SCI data register. For the transmit data buffer, this bit is stored in T8 in SCIC3. For the receiver, the ninth bit is held in R8 in SCIC3.

For coherent writes to the transmit data buffer, write to the T8 bit before writing to SCID.

13.1.1 Features

Features of the SPI module include:

- Master or slave mode operation
- Full-duplex or single-wire bidirectional option
- Programmable transmit bit rate
- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting

13.1.2 Block Diagrams

This section includes block diagrams showing SPI system connections, the internal organization of the SPI module, and the SPI clock dividers that control the master mode bit rate.

13.1.2.1 SPI System Block Diagram

Figure 13-2 shows the SPI modules of two MCUs connected in a master-slave arrangement. The master device initiates all SPI data transfers. During a transfer, the master shifts data out (on the MOSI pin) to the slave while simultaneously shifting data in (on the MISO pin) from the slave. The transfer effectively exchanges the data that was in the SPI shift registers of the two SPI systems. The SPSCCK signal is a clock output from the master and an input to the slave. The slave device must be selected by a low level on the slave select input (\overline{SS} pin). In this system, the master device has configured its \overline{SS} pin as an optional slave select output.

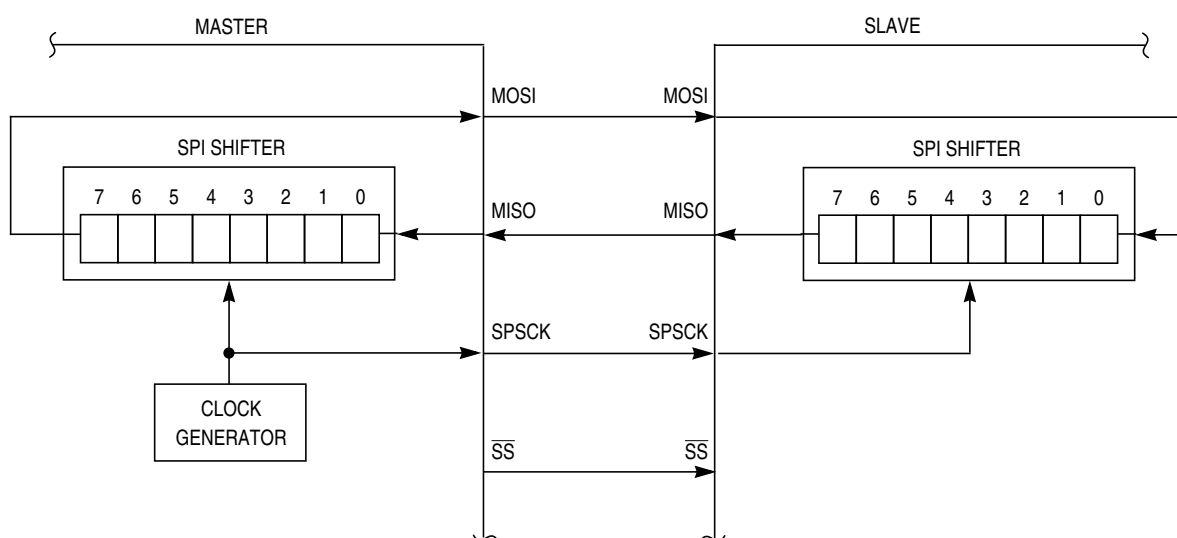


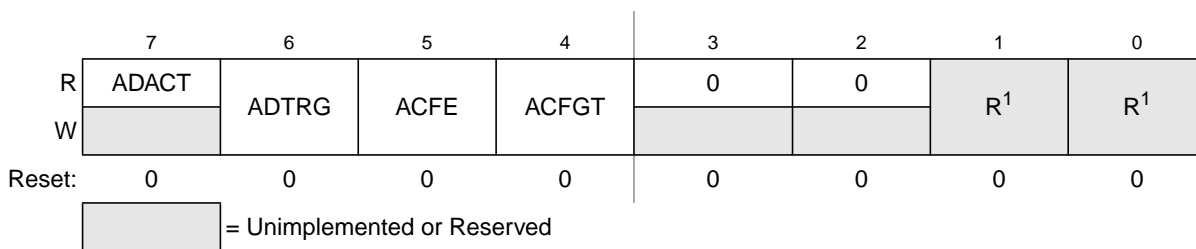
Figure 13-2. SPI System Connections

Figure 15-4. Input Channel Select (continued)

ADCH	Input Select	ADCH	Input Select
01000	AD8	11000	AD24
01001	AD9	11001	AD25
01010	AD10	11010	AD26
01011	AD11	11011	AD27
01100	AD12	11100	Reserved
01101	AD13	11101	V _{REFH}
01110	AD14	11110	V _{REFL}
01111	AD15	11111	Module disabled

15.3.2 Status and Control Register 2 (ADCSC2)

The ADCSC2 register is used to control the compare function, conversion trigger and conversion active of the ADC module.



¹ Bits 1 and 0 are reserved bits that must always be written to 0.

Figure 15-5. Status and Control Register 2 (ADCSC2)

Table 15-4. ADCSC2 Register Field Descriptions

Field	Description
7 ADACT	Conversion Active — ADACT indicates that a conversion is in progress. ADACT is set when a conversion is initiated and cleared when a conversion is completed or aborted. 0 Conversion not in progress 1 Conversion in progress
6 ADTRG	Conversion Trigger Select — ADTRG is used to select the type of trigger to be used for initiating a conversion. Two types of trigger are selectable: software trigger and hardware trigger. When software trigger is selected, a conversion is initiated following a write to ADCSC1. When hardware trigger is selected, a conversion is initiated following the assertion of the ADHWT input. 0 Software trigger selected 1 Hardware trigger selected

Chapter 16

Analog Comparator (S08ACMPV2)

16.1 Introduction

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages or for comparing one analog input voltage to an internal reference voltage. The comparator circuit is designed to operate across the full range of the supply voltage (rail to rail operation).

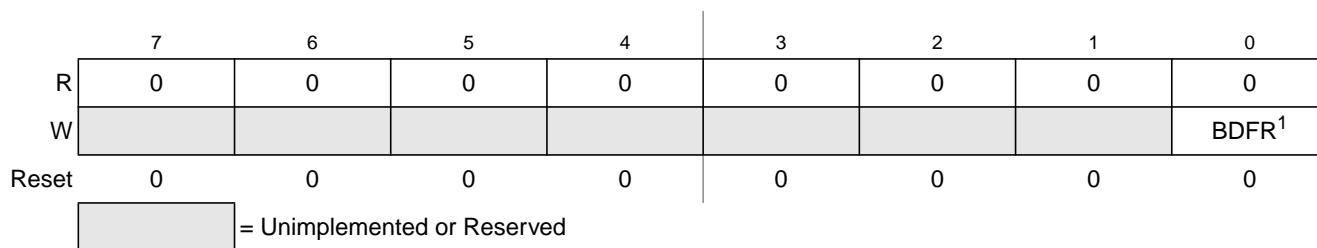
16.1.1 ACMP/TPM1 Configuration Information

The ACMP module can be configured to connect the output of the analog comparator to TPM1 input capture channel 0 by setting ACIC in SOPT2. With ACIC set, the TPM1CH0 pin is not available externally regardless of the configuration of the TPM1 module

Figure 16-1 shows the MC9S08LC60 Series block diagram with the ACMP highlighted.

16.1.2 AMCPO Availability

For the MC9S08LC60 Series, the AMCPO pin is not available, so the ACOPE bit in the ACMPSC register is reserved and does not have any effect.



¹ BDFR is writable only through serial background mode debug commands, not from user programs.

Figure 17-6. System Background Debug Force Reset Register (SBDFR)

Table 17-3. SBDFR Register Field Description

Field	Description
0 BDFR	Background Debug Force Reset — A serial active background mode command such as WRITE_BYTE allows an external debug host to force a target system reset. Writing 1 to this bit forces an MCU reset. This bit cannot be written from a user program.

17.4.3 DBG Registers and Control Bits

The debug module includes nine bytes of register space for three 16-bit registers and three 8-bit control and status registers. These registers are located in the high register space of the normal memory map so they are accessible to normal application programs. These registers are rarely if ever accessed by normal user application programs with the possible exception of a ROM patching mechanism that uses the breakpoint logic.

17.4.3.1 Debug Comparator A High Register (DBGCAH)

This register contains compare value bits for the high-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.2 Debug Comparator A Low Register (DBGCAL)

This register contains compare value bits for the low-order eight bits of comparator A. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.3 Debug Comparator B High Register (DBGCBH)

This register contains compare value bits for the high-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

17.4.3.4 Debug Comparator B Low Register (DBGCBL)

This register contains compare value bits for the low-order eight bits of comparator B. This register is forced to 0x00 at reset and can be read at any time or written at any time unless ARM = 1.

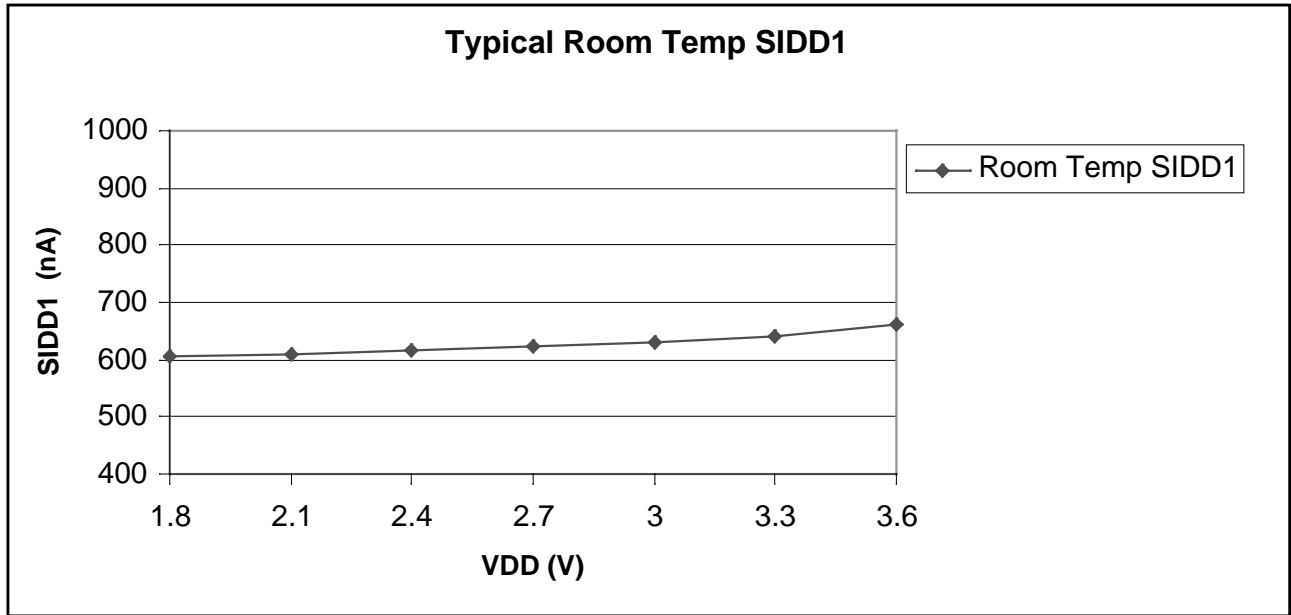


Figure A-7. Typical Stop1 I_{DD}

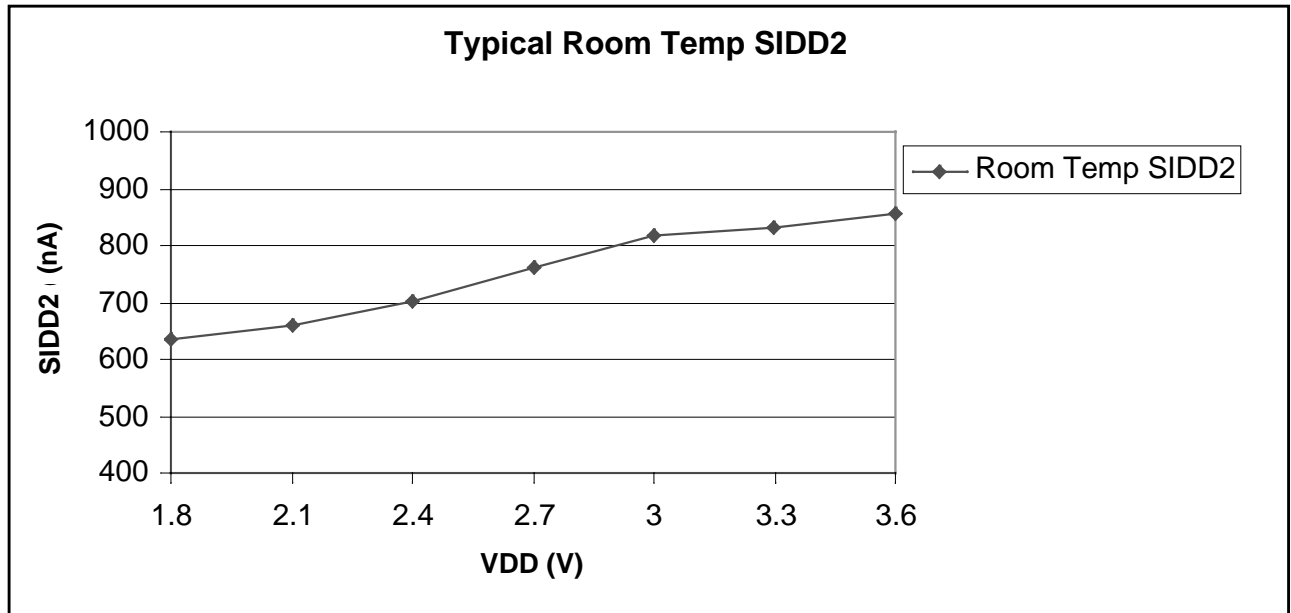


Figure A-8. Typical Stop 2 I_{DD}

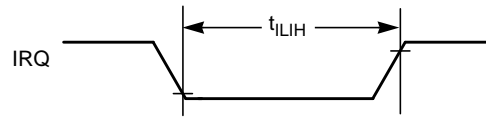


Figure A-14. IRQ Timing

A.10.2 Timer/PWM (TPM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table A-14. TPM Input Timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
External clock period	t_{TPMext}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

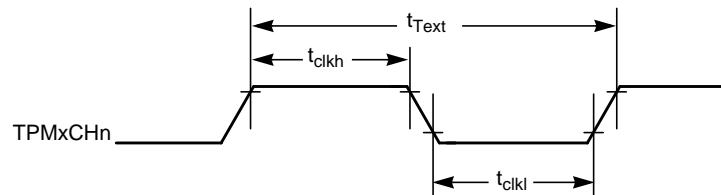


Figure A-15. Timer External Clock

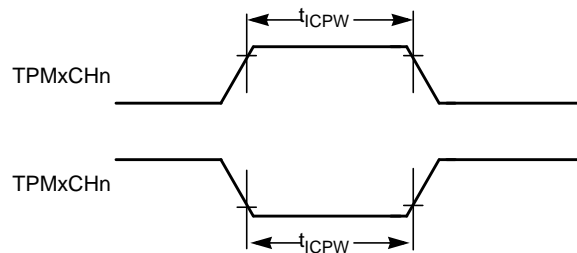


Figure A-16. Timer Input Capture Pulse

