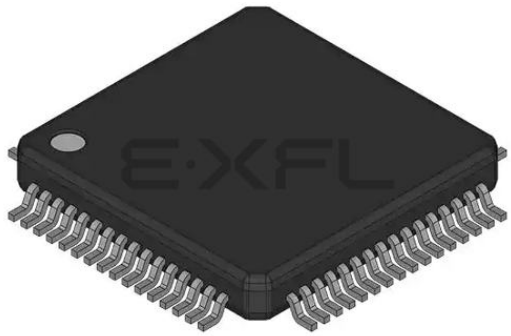

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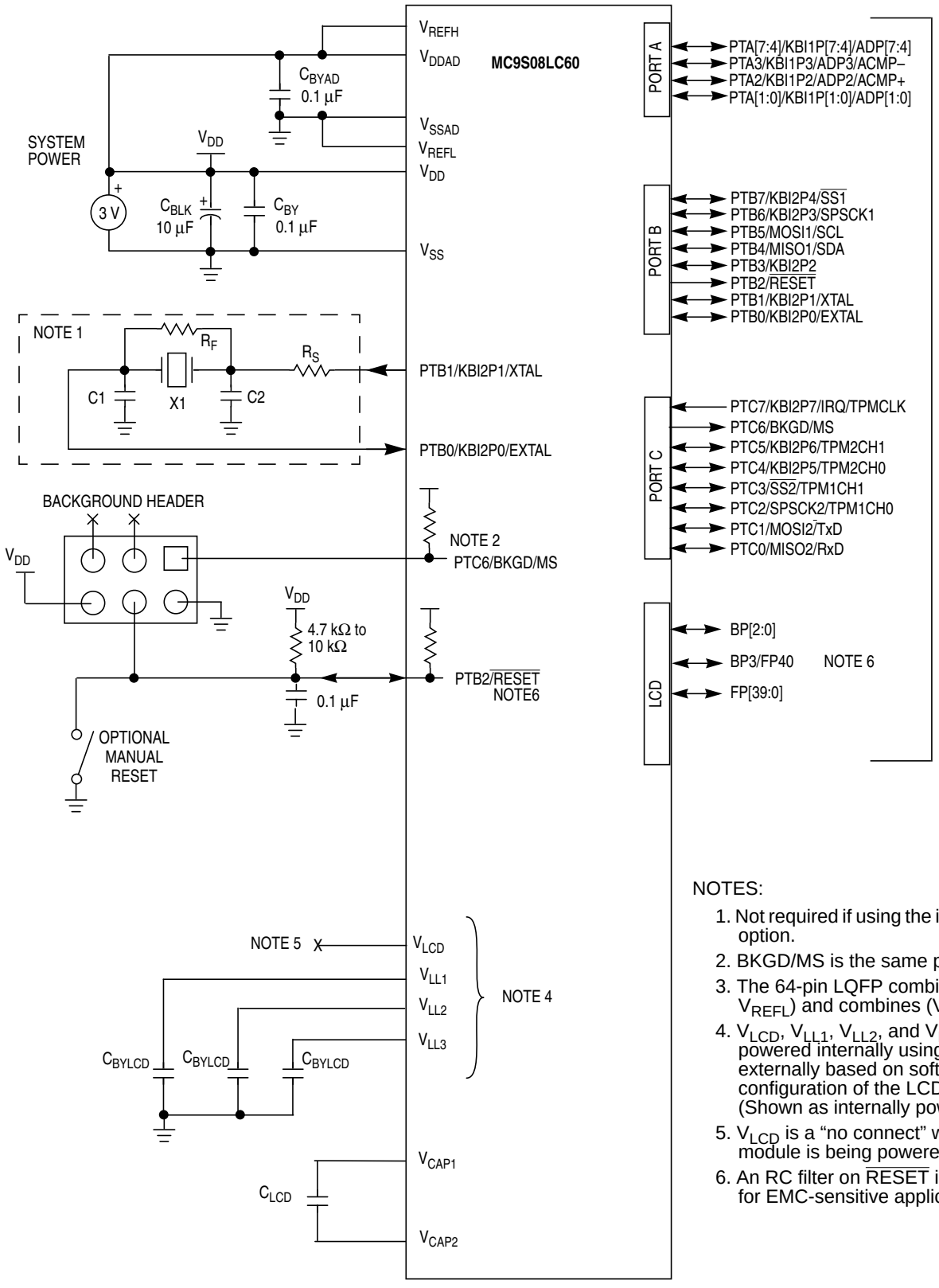
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SCI, SPI
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 2x12b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08lc60lh

Chapter 6
Parallel Input/Output

Chapter 7
Keyboard Interrupt (S08KBIV2)



NOTES:

1. Not required if using the internal oscillator option.
2. BKGD/MS is the same pin as PTC6.
3. The 64-pin LQFP combines (V_{SSAD} to V_{REFL}) and combines (V_{DDAD} to V_{REFH})
4. V_{LCD}, V_{LL1}, V_{LL2}, and V_{LL3} can be powered internally using V_{DD} or externally based on software configuration of the LCD module. (Shown as internally powered).
5. V_{LCD} is a “no connect” when the LCD module is being powered via V_{DD}.
6. An RC filter on $\overline{\text{RESET}}$ is recommended for EMC-sensitive applications.

Figure 2-3. Basic System Connections

Table 3-2. Stop Mode Behavior

Peripheral	Mode		
	Stop1	Stop2	Stop3
CPU	Off	Off	Standby
RAM	Off	Standby	Standby
FLASH	Off	Off	Standby
Parallel Port Registers	Off	Off	Standby
ADC	Off	Off	Optionally On[1]
ACMP	Off	Off	Standby
ICG	Off	Off	Optionally On[2]
IIC	Off	Off	Standby
LCD	Off	Off	Optionally On[3]
SCI	Off	Off	Standby
SPI	Off	Off	Standby
TPM	Off	Off	Standby
Voltage Regulator	Off	Standby	Standby
I/O Pins	Hi-Z	States Held	States Held

1 Requires the asynchronous ADC clock and LVD to be enabled, else in standby.

2 OSCSPEN set in ICGC1, else in standby.

3 LCDSTP3 = 1 in the LCDCR1 register.

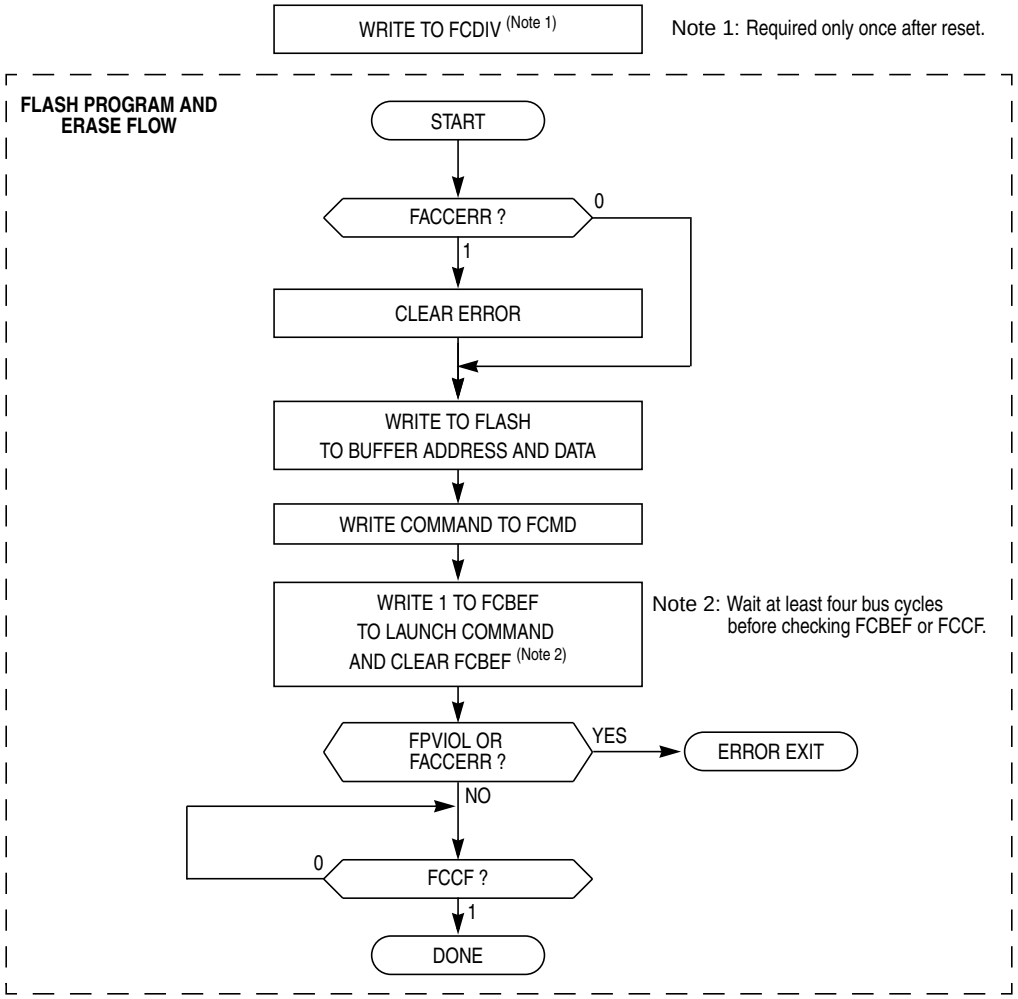


Figure 4-2. FLASH Program and Erase Flowchart

4.4.4 Burst Program Execution

The burst program command is used to program sequential bytes of data in less time than would be required using the standard program command. For the MC9S08LC60 Series, it is possible to burst across FLASH array boundaries as long as the addresses are consecutive. This is possible because the high voltage to the FLASH array does not need to be disabled between program operations. Ordinarily, when a program or erase command is issued, an internal charge pump associated with the FLASH memory must be enabled to supply high voltage to the array. Upon completion of the command, the charge pump is turned off. When a burst program command is issued, the charge pump is enabled and then remains enabled after completion of the burst program operation if these two conditions are met:

- The next burst program command has been queued before the current program operation has completed.
- The next sequential address selects a byte on the same physical row as the current byte being programmed. A row of FLASH memory consists of 64 bytes. A byte within a row is selected by addresses A5 through A0. A new row begins when addresses A5 through A0 are all zero.

Chapter 7
Keyboard Interrupt (S08KBIV2)

7.1 Introduction

This on-chip peripheral module is called a keyboard interrupt (KBI) module because originally it was designed to simplify the connection and use of row-column matrices of keyboard switches. However, these inputs are also useful as extra external interrupt inputs and as an external means of waking up the MCU from stop or wait low-power modes.

The KBI module allows up to eight pins to act as additional interrupt sources. These pins can be configured for either rising-edge sensing or falling-edge sensing. The sensing mode for all eight pins can also be modified to detect edges and levels instead of only edges.

MC9S08LC60 Series MCUs have two KBIs. When they are described individually, they are called KBI1 and/or KBI2. When referring to the module in general or both KBIs collectively, they are called KBIx.

Figure 7-1 Shows the MC9S08LC60 Series block guide with the KBIs highlighted.

Synchronous logic is used to detect edges. Prior to detecting an edge, enabled keyboard inputs must be at the deasserted logic level. A falling edge is detected when an enabled keyboard input signal is seen as a logic 1 (the deasserted level) during one bus cycle and then a logic 0 (the asserted level) during the next cycle. A rising edge is detected when the input signal is seen as a logic 0 during one bus cycle and then a logic 1 during the next cycle.

7.4.1 Edge Only Sensitivity

A valid edge on an enabled KBI pin will set KBF in KBIxSC. If KBIE in KBIxSC is set, an interrupt request will be presented to the CPU. Clearing of KBF is accomplished by writing a 1 to KBACK in KBIxSC.

7.4.2 Edge and Level Sensitivity

A valid edge or level on an enabled KBI pin will set KBF in KBIxSC. If KBIE in KBIxSC is set, an interrupt request will be presented to the CPU. Clearing of KBF is accomplished by writing a 1 to KBACK in KBIxSC provided all enabled keyboard inputs are at their deasserted levels. KBF will remain set if any enabled KBI pin is asserted while attempting to clear by writing a 1 to KBACK.

7.4.3 KBI Pullup/Pulldown Resistors

The KBI pins can be configured to use an internal pullup/pulldown resistor using the associated I/O port pullup enable register. If an internal resistor is enabled, the KBIxES register is used to select whether the resistor is a pullup (KBEDGn = 0) or a pulldown (KBEDGn = 1).

7.4.4 KBI Initialization

When a keyboard interrupt pin is first enabled it is possible to get a false keyboard interrupt flag. To prevent a false interrupt request during keyboard initialization, the user should do the following:

1. Mask keyboard interrupts by clearing KBIE in KBIxSC.
2. Enable the KBI polarity by setting the appropriate KBEDGn bits in KBIxES.
3. If using internal pullup/pulldown device, configure the associated pullup enable bits in PTxPE.
4. Enable the KBI pins by setting the appropriate KBIPEn bits in KBIxPE.
5. Write to KBACK in KBIxSC to clear any false interrupts.
6. Set KBIE in KBIxSC to enable interrupts.

8.3.5 Extended Addressing Mode (EXT)

In extended addressing mode, the full 16-bit address of the operand is located in the next two bytes of program memory after the opcode (high byte first).

8.3.6 Indexed Addressing Mode

Indexed addressing mode has seven variations including five that use the 16-bit H:X index register pair and two that use the stack pointer as the base reference.

8.3.6.1 Indexed, No Offset (IX)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair as the address of the operand needed to complete the instruction.

8.3.6.2 Indexed, No Offset with Post Increment (IX+)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair as the address of the operand needed to complete the instruction. The index register pair is then incremented (H:X = H:X + 0x0001) after the operand has been fetched. This addressing mode is only used for MOV and CBEQ instructions.

8.3.6.3 Indexed, 8-Bit Offset (IX1)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction.

8.3.6.4 Indexed, 8-Bit Offset with Post Increment (IX1+)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction. The index register pair is then incremented (H:X = H:X + 0x0001) after the operand has been fetched. This addressing mode is used only for the CBEQ instruction.

8.3.6.5 Indexed, 16-Bit Offset (IX2)

This variation of indexed addressing uses the 16-bit value in the H:X index register pair plus a 16-bit offset included in the instruction as the address of the operand needed to complete the instruction.

8.3.6.6 SP-Relative, 8-Bit Offset (SP1)

This variation of indexed addressing uses the 16-bit value in the stack pointer (SP) plus an unsigned 8-bit offset included in the instruction as the address of the operand needed to complete the instruction.

Table 8-3. Opcode Map (Sheet 2 of 2)

Bit-Manipulation		Branch	Read-Modify-Write					Control		Register/Memory					
						9E60 6 NEG 3 SP1							9ED0 5 SUB 4 SP2	9EE0 4 SUB 3 SP1	
						9E61 6 CBEQ 4 SP1							9ED1 5 CMP 4 SP2	9EE1 4 CMP 3 SP1	
													9ED2 5 SBC 4 SP2	9EE2 4 SBC 3 SP1	
						9E63 6 COM 3 SP1							9ED3 5 CPX 4 SP2	9EE3 4 CPX 3 SP1	9EF3 6 CPHX 3 SP1
						9E64 6 LSR 3 SP1							9ED4 5 AND 4 SP2	9EE4 4 AND 3 SP1	
													9ED5 5 BIT 4 SP2	9EE5 4 BIT 3 SP1	
						9E66 6 ROR 3 SP1							9ED6 5 LDA 4 SP2	9EE6 4 LDA 3 SP1	
						9E67 6 ASR 3 SP1							9ED7 5 STA 4 SP2	9EE7 4 STA 3 SP1	
						9E68 6 LSL 3 SP1							9ED8 5 EOR 4 SP2	9EE8 4 EOR 3 SP1	
						9E69 6 ROL 3 SP1							9ED9 5 ADC 4 SP2	9EE9 4 ADC 3 SP1	
						9E6A 6 DEC 3 SP1							9EDA 5 ORA 4 SP2	9EEA 4 ORA 3 SP1	
						9E6B 8 DBNZ 4 SP1							9EDB 5 ADD 4 SP2	9EEB 4 ADD 3 SP1	
						9E6C 6 INC 3 SP1									
						9E6D 5 TST 3 SP1									
										9EAE 5 LDHX 2 IX	9EBE 6 LDHX 4 IX2	9ECE 5 LDHX 3 IX1	9EDE 5 LDX 4 SP2	9EEE 4 LDX 3 SP1	9EFE 5 LDHX 3 SP1
						9E6F 6 CLR 3 SP1							9EDF 5 STX 4 SP2	9EEF 4 STX 3 SP1	9EFF 5 STHX 3 SP1

INH	**Inherent**	**REL**	**Relative**	**SP1**	**Stack Pointer, 8-Bit Offset**
IMM	**Immediate**	**IX**	**Indexed, No Offset**	**SP2**	**Stack Pointer, 16-Bit Offset**
DIR	**Direct**	**IX1**	**Indexed, 8-Bit Offset**	**IX+**	**Indexed, No Offset with**
EXT	**Extended**	**IX2**	**Indexed, 16-Bit Offset**		**Post Increment**
DD	**DIR to DIR**	**IMD**	**IMM to DIR**	**IX1+**	**Indexed, 1-Byte Offset with**
IX+D	**IX+ to DIR**	**DIX+**	**DIR to IX+**		**Post Increment**

Note: All Sheet 2 Opcodes are Preceded by the Page 2 Prebyte (9E)

Prebyte (9E) and Opcode in Hexadecimal
Number of Bytes

HCS08 Cycles
Instruction Mnemonic
Addressing Mode

9.6.1.1 LCD Module Waveforms

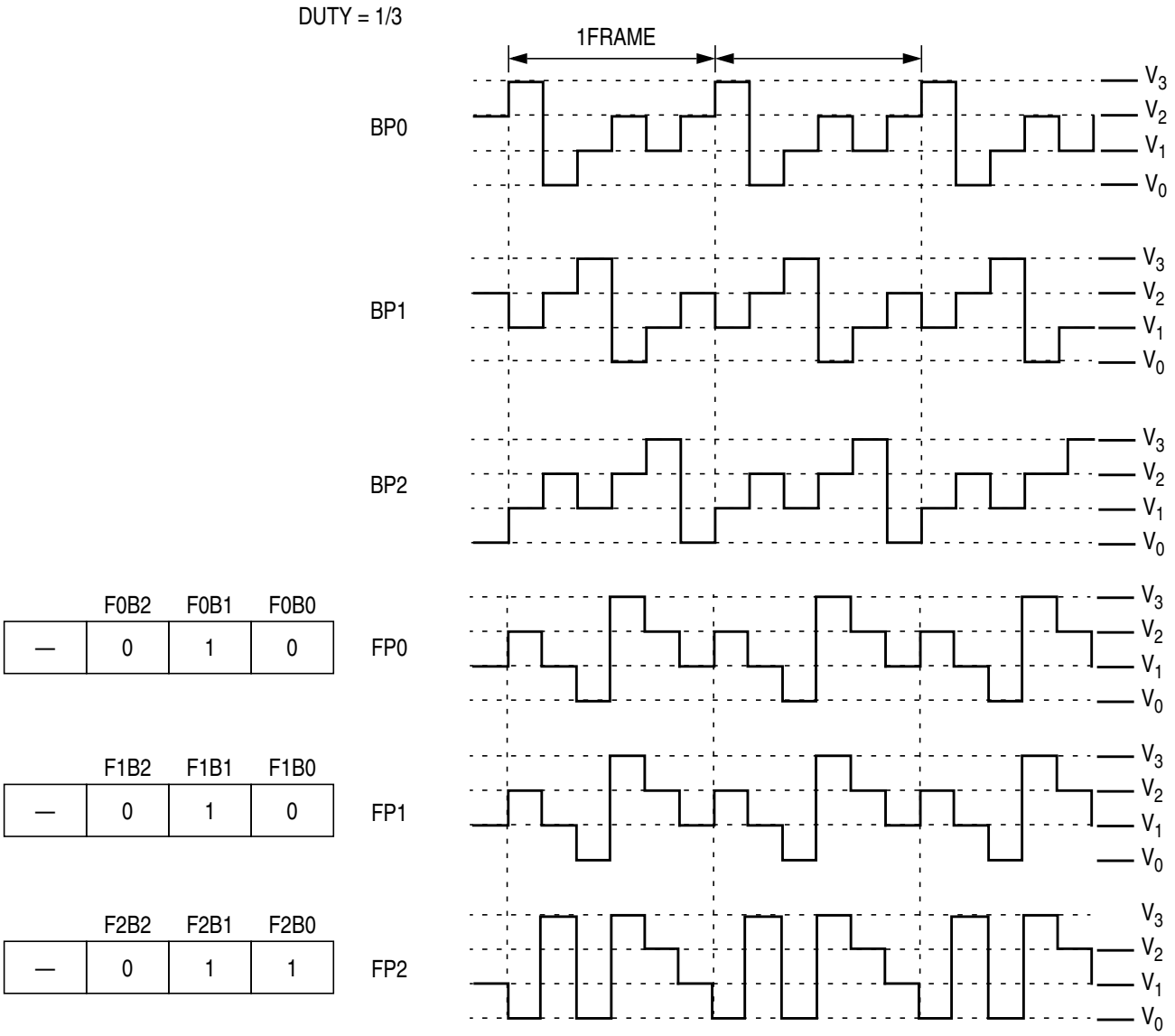


Figure 9-20. LCD Waveforms (LPWAVE = 0)

Chapter 10
Internal Clock Generator (S08ICGV4)

10.1 Introduction

The ICG module is used to generate the system clocks for the MC9S08LC60/36/20 MCU. Figure 10-1 shows the clock distribution for the MC9S08LC60/36/20 MCU. Electrical parametric data for the ICG may be found in Appendix.

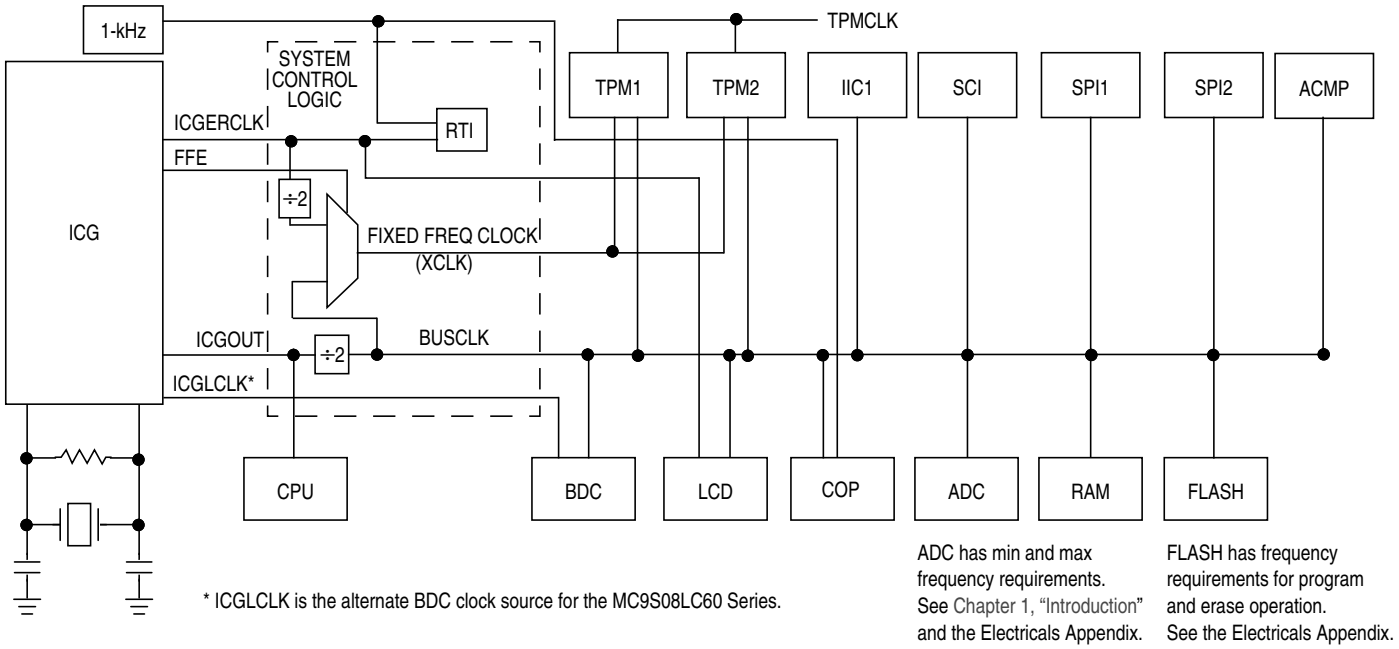


Figure 10-1. System Clock Distribution Diagram

NOTE

Freescale Semiconductor programs a factory trim value for ICGTRM into the FLASH location $FFBE (NVICGTRM). Leaving this address for the ICGTRM value also allows debugger and programmer vendors to perform a manual trim operation and store the resultant ICGTRM value into NVICGTRM for users to access at a later time. The value in NVICGTRM is not automatically loaded and therefore must be copied into ICGTRM by user code.

Figure 10-2 shows the MC9S08LC60 Series block diagram with the ICG highlighted.

10.5.1 Off Mode (Off)

Normally when the CPU enters stop mode, the ICG will cease all clock activity and is in the off state. However there are two cases to consider when clock activity continues while the CPU is in stop mode,

10.5.1.1 BDM Active

When the BDM is enabled, the ICG continues activity as originally programmed. This allows access to memory and control registers via the BDC controller.

10.5.1.2 OSCSTEN Bit Set

When the oscillator is enabled in stop mode (OSCSTEN = 1), the individual clock generators are enabled but the clock feed to the rest of the MCU is turned off. This option is provided to avoid long oscillator startup times if necessary, or to run the RTI from the oscillator during stop3.

10.5.1.3 Stop/Off Mode Recovery

Upon the CPU exiting stop mode due to an interrupt, the previously set control bits are valid and the system clock feed resumes. If FEE is selected, the ICG will source the internal reference until the external clock is stable. If FBE is selected, the ICG will wait for the external clock to stabilize before enabling ICGOUT.

Upon the CPU exiting stop mode due to a reset, the previously set ICG control bits are ignored and the default reset values applied. Therefore the ICG will exit stop in SCM mode configured for an approximately 8 MHz DCO output (4 MHz bus clock) with trim value maintained. If using a crystal, 4096 clocks are detected prior to engaging ICGERCLK. This is incorporated in crystal start-up time.

10.5.2 Self-Clocked Mode (SCM)

Self-clocked mode (SCM) is the default mode of operation and is entered when any of the following conditions occur:

- After any reset.
- Exiting from off mode when CLKS does not equal 10. If CLKS = X1, the ICG enters this state temporarily until the DCO is stable (DCOS = 1).
- CLKS bits are written from X1 to 00.
- CLKS = 1X and ICGERCLK is not detected (both ERCS = 0 and LOCS = 1).

In this state, the FLL loop is open. The DCO is on, and the output clock signal ICGOUT frequency is given by $f_{ICGDCLK}$ / R. The ICGDCLK frequency can be varied from 8 MHz to 40 MHz by writing a new value into the filter registers (ICGFLTH and ICGFLTL). This is the only mode in which the filter registers can be written.

If this mode is entered due to a reset, $f_{ICGDCLK}$ will default to f_{Self_reset} which is nominally 8 MHz. If this mode is entered from FLL engaged internal, $f_{ICGDCLK}$ will maintain the previous frequency.If this mode is entered from FLL engaged external (either by programming CLKS or due to a loss of external reference clock), $f_{ICGDCLK}$ will maintain the previous frequency, but ICGOUT will double if the FLL was unlocked. If this mode is entered from off mode, $f_{ICGDCLK}$ will be equal to the frequency of ICGDCLK before

10.6.4 Example #3: No External Crystal Connection, 5.4 MHz Bus Frequency

In this example, the FLL will be used (in FEI mode) to multiply the internal 243 kHz (approximate) reference clock up to 10.8 MHz to achieve 5.4 MHz bus frequency. This system will also use the trim function to fine tune the frequency based on an external reference signal.

After the MCU is released from reset, the ICG is in self-clocked mode (SCM) and supplies approximately 8 MHz on ICGOUT which corresponds to a 4 MHz bus frequency (f_{Bus}).

The clock scheme will be FLL engaged, internal (FEI). So

$$f_{ICGOUT} = (f_{IRG} / 7) * P * N / R ; P = 64,\ f_{IRG} = 243\ kHz \qquad \textit{Eqn. 10-5}$$

Solving for N / R gives:

$$N / R = 10.8\ MHz /(243/7\ kHz * 64) = 4.86 ;\ \text{We can choose N = 10 and R = 2.} \qquad \textit{Eqn. 10-6}$$

A trim procedure will be required to hone the frequency to exactly 5.4 MHz. An example of the trim procedure is shown in example #4.

The values needed in each register to set up the desired operation are:

ICGC1 = $28 (%00101000)

Bit 7	HGO	0	Configures oscillator for low power
Bit 6	RANGE	0	Configures oscillator for low-frequency range; FLL prescale factor is 64
Bit 5	REFS	1	Oscillator using crystal or resonator requested (bit is really a don’t care)
Bits 4:3	CLKS	01	FLL engaged, internal reference clock mode
Bit 2	OSCSTEN	0	Disables the oscillator
Bit 1	LOCD	0	Loss-of-clock enabled
Bit 0		0	Unimplemented or reserved, always reads zero

ICGC2 = $31 (%00110001)

Bit 7	LOLRE	0	Generates an interrupt request on loss of lock
Bit 6:4	MFD	011	Sets the MFD multiplication factor to 10
Bit 3	LOCRE	0	Generates an interrupt request on loss of clock
Bit 2:0	RFD	001	Sets the RFD division factor to ÷2

ICGS1 = $xx

This is read only except for clearing interrupt flag

ICGS2 = $xx

This is read only; good idea to read this before performing time critical operations

ICGFLTLU/L = $xx

Not used in this example

When center-aligned PWM operation is specified, the counter counts upward from 0x0000 through its terminal count and then counts downward to 0x0000 where it returns to up-counting. Both 0x0000 and the terminal count value (value in TPMxMODH:TPMxMODL) are normal length counts (one timer clock period long).

An interrupt flag and enable are associated with the main 16-bit counter. The timer overflow flag (TOF) is a software-accessible indication that the timer counter has overflowed. The enable signal selects between software polling (TOIE = 0) where no hardware interrupt is generated, or interrupt-driven operation (TOIE = 1) where a static hardware interrupt is automatically generated whenever the TOF flag is 1.

The conditions that cause TOF to become set depend on the counting mode (up or up/down). In up-counting mode, the main 16-bit counter counts from 0x0000 through 0xFFFF and overflows to 0x0000 on the next counting clock. TOF becomes set at the transition from 0xFFFF to 0x0000. When a modulus limit is set, TOF becomes set at the transition from the value set in the modulus register to 0x0000. When the main 16-bit counter is operating in up-/down-counting mode, the TOF flag gets set as the counter changes direction at the transition from the value set in the modulus register and the next lower count value. This corresponds to the end of a PWM period. (The 0x0000 count value corresponds to the center of a period.)

Because the HCS08 MCU is an 8-bit architecture, a coherency mechanism is built into the timer counter for read operations. Whenever either byte of the counter is read (TPMxCNTH or TPMxCNTL), both bytes are captured into a buffer so when the other byte is read, the value will represent the other byte of the count at the time the first byte was read. The counter continues to count normally, but no new value can be read from either byte until both bytes of the old count have been read.

The main timer counter can be reset manually at any time by writing any value to either byte of the timer count TPMxCNTH or TPMxCNTL. Resetting the counter in this manner also resets the coherency mechanism in case only one byte of the counter was read before resetting the count.

11.4.2 Channel Mode Selection

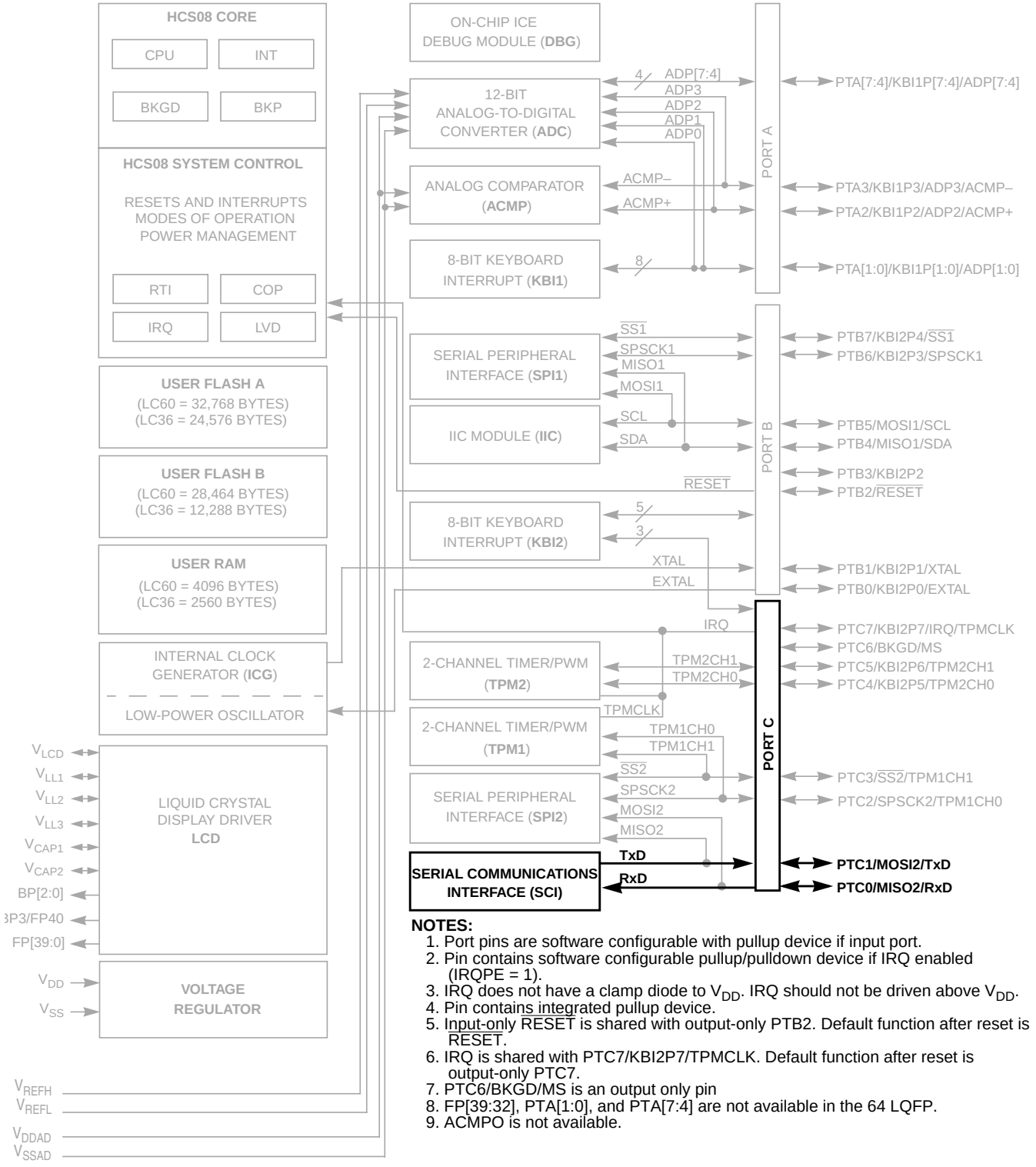
Provided CPWMS = 0 (center-aligned PWM operation is not specified), the MSnB and MSnA control bits in the channel n status and control registers determine the basic mode of operation for the corresponding channel. Choices include input capture, output compare, and buffered edge-aligned PWM.

11.4.2.1 Input Capture Mode

With the input capture function, the TPM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TPM latches the contents of the TPM counter into the channel value registers (TPMxCnVH:TPMxCnVL). Rising edges, falling edges, or any edge may be chosen as the active edge that triggers an input capture.

When either byte of the 16-bit capture register is read, both bytes are latched into a buffer to support coherent 16-bit accesses regardless of order. The coherency sequence can be manually reset by writing to the channel status/control register (TPMxCnSC).

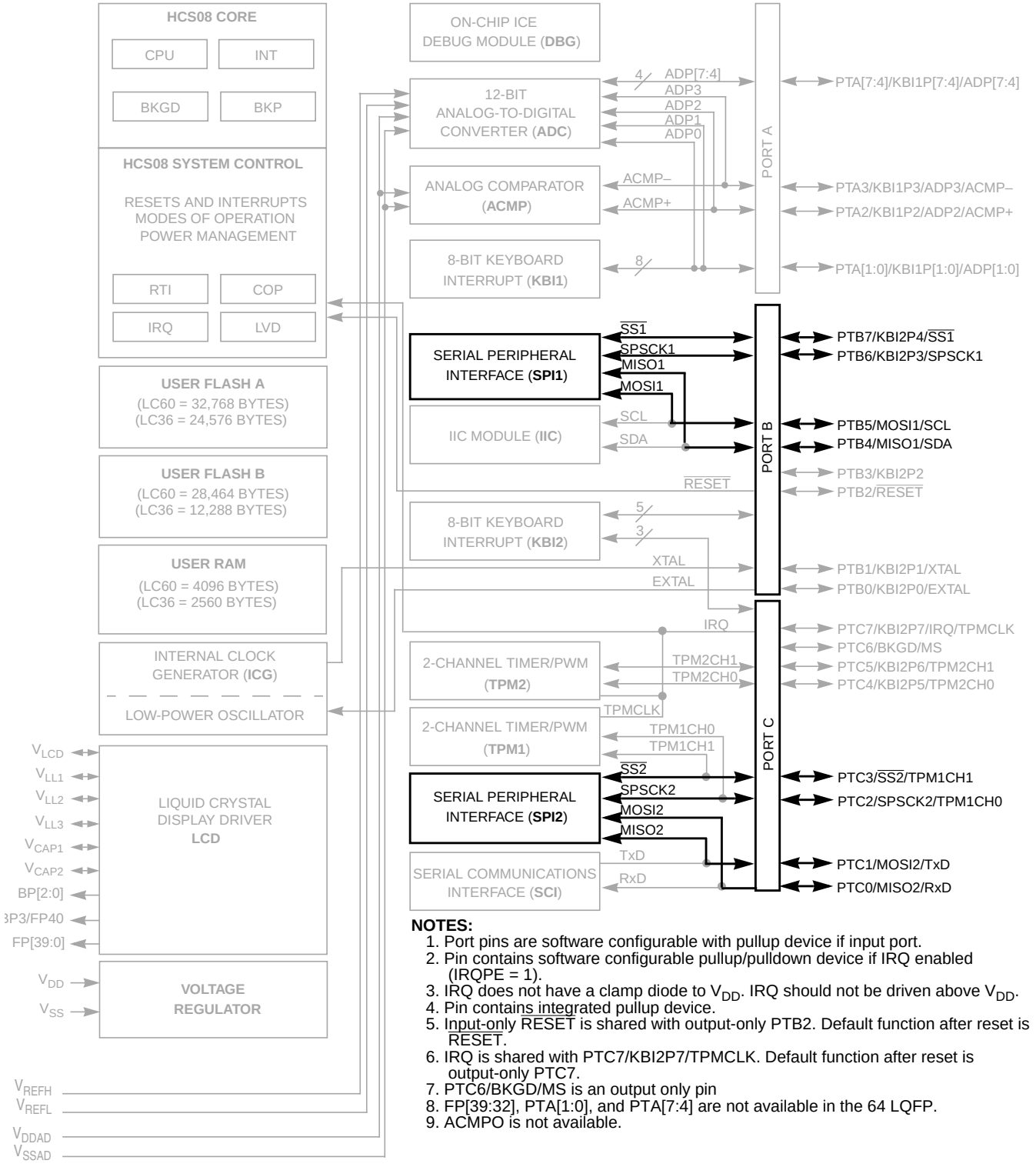
An input capture event sets a flag bit (CHnF) that can optionally generate a CPU interrupt request.



NOTES:

1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. Input-only RESET is shared with output-only PTB2. Default function after reset is RESET.
6. IRQ is shared with PTC7/KBI2P7/TPMCLK. Default function after reset is output-only PTC7.
7. PTC6/BKGD/MS is an output only pin
8. FP[39:32], PTA[1:0], and PTA[7:4] are not available in the 64 LQFP.
9. ACMPO is not available.

Figure 12-1. MC9S08LC60 Series Block Diagram Highlighting SCI Block and Pins



NOTES:

1. Port pins are software configurable with pullup device if input port.
2. Pin contains software configurable pullup/pulldown device if IRQ enabled (IRQPE = 1).
3. IRQ does not have a clamp diode to V_{DD}. IRQ should not be driven above V_{DD}.
4. Pin contains integrated pullup device.
5. Input-only RESET is shared with output-only PTB2. Default function after reset is RESET.
6. IRQ is shared with PTC7/KBI2P7/TPMCLK. Default function after reset is output-only PTC7.
7. PTC6/BKGD/MS is an output only pin
8. FP[39:32], PTA[1:0], and PTA[7:4] are not available in the 64 LQFP.
9. ACMPO is not available.

Figure 13-1. MC9S08LC60 Series Block Diagram Highlighting SPI Blocks and Pins

Chapter 16
Analog Comparator (S08ACMPV2)

16.1 Introduction

The analog comparator module (ACMP) provides a circuit for comparing two analog input voltages or for comparing one analog input voltage to an internal reference voltage. The comparator circuit is designed to operate across the full range of the supply voltage (rail to rail operation).

16.1.1 ACMP/TPM1 Configuration Information

The ACMP module can be configured to connect the output of the analog comparator to TPM1 input capture channel 0 by setting ACIC in SOPT2. With ACIC set, the TPM1CH0 pin is not available externally regardless of the configuration of the TPM1 module

Figure 16-1 shows the MC9S08LC60 Series block diagram with the ACMP highlighted.

16.1.2 AMCPO Availability

For the MC9S08LC60 Series, the AMCPO pin is not available, so the ACOPE bit in the ACMPSC register is reserved and does not have any effect.

Table A-7. 3 Volt 12-bit ADC Operating Conditions

Characteristic	Conditions	Symbol	Min	Typ(1)	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
	8 bit mode (all valid f_{ADCK})		—	—	10		
ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
	Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

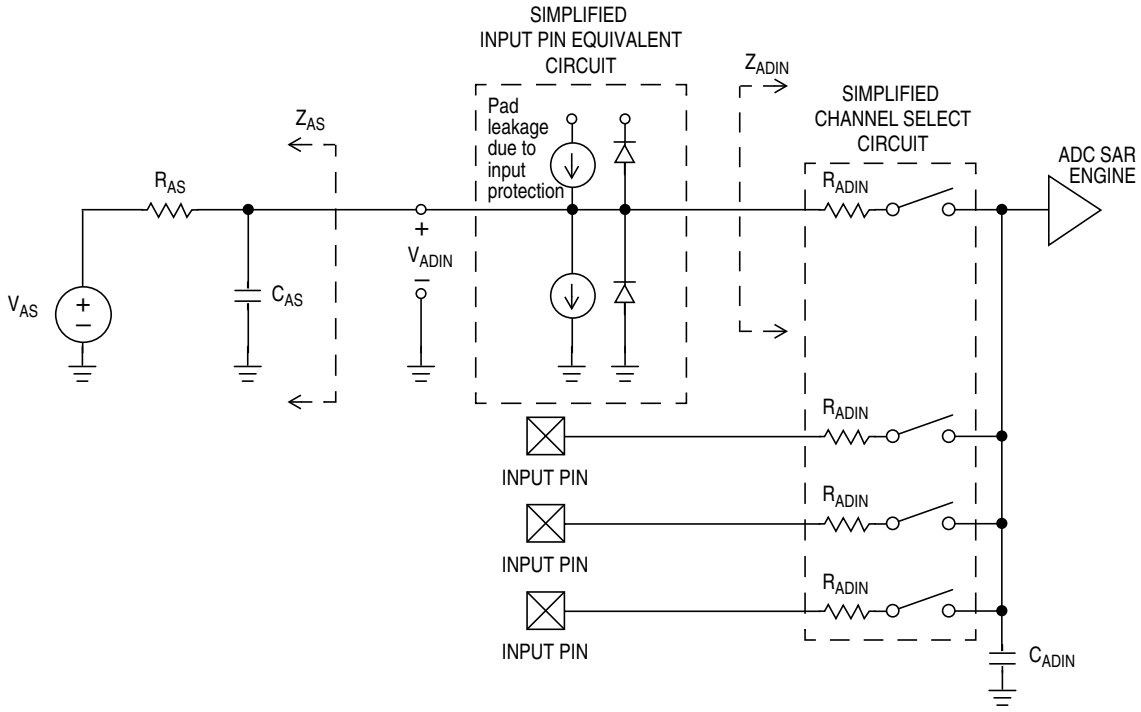
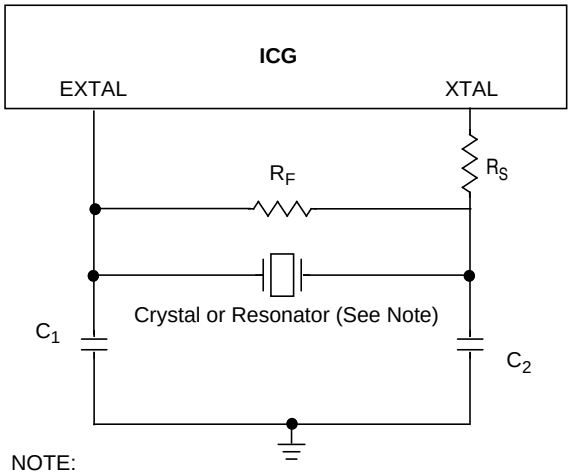


Figure A-10. ADC Input Impedance Equivalency Diagram

Table A-8. 3 Volt 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symbol	Min	Typ(1)	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	µA	

A.9 Internal Clock Generation Module Characteristics



NOTE:
Use fundamental mode crystal or ceramic resonator only.

Table A-11. ICG DC Electrical Specifications (Temperature Range = 0 to 70°C Ambient)

Characteristic	Symbol	Min	Typ(1)	Max	Unit
Load capacitors	C_1 C_2	See Note (2)			
Feedback resistor Low range (32k to 100 kHz) High range (1M – 16 MHz)	R_F		 10 1		 MΩ MΩ
Series resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_S	 0 0	 0 0	 10 0	 kΩ

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 See crystal or resonator manufacturer's recommendation.

A.9.1 ICG Frequency Specifications

Table A-12. ICG Frequency Specifications
(V_{DDA} = V_{DDA} (min) to V_{DDA} (max), Temperature Range = 0 to 70°C Ambient)

Characteristic	Symbol	Min	Typical	Max	Unit
Oscillator crystal or resonator (REFS = 1) (Fundamental mode crystal or ceramic resonator) Low range High range, FLL bypassed external (CLKS = 10) High range, FLL engaged external (CLKS = 11)	 f_{lo} f_{hi_byp} f_{hi_eng}	 32 1 2	 — — —	 100 16 10	 kHz MHz MHz
Input clock frequency (CLKS = 11, REFS = 0) Low range High range	 f_{lo} f_{hi_eng}	 32 2	 — —	 100 10	 kHz MHz
Input clock frequency (CLKS = 10, REFS = 0)	f_{Extal}	0	—	40	MHz
Internal reference frequency (untrimmed)	$f_{ICGIRCLK}$	182.25	243	303.75	kHz

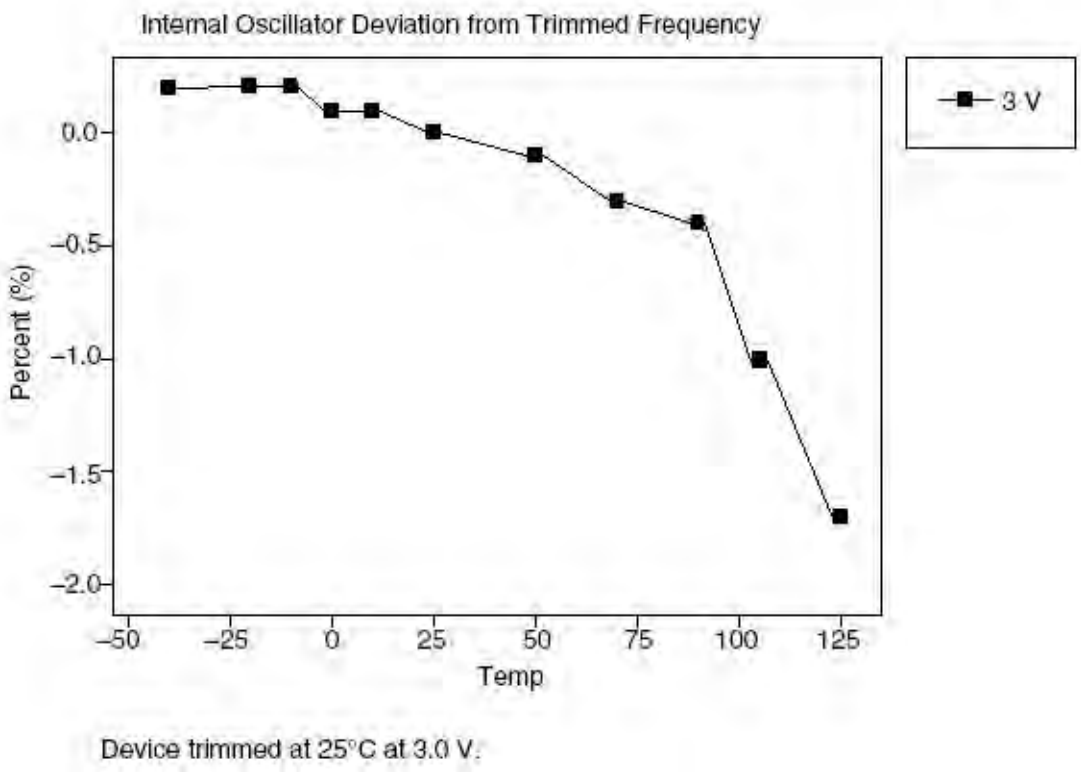


Figure A-11. Internal Oscillator Deviation from Trimmed Frequency

A.10 AC Characteristics

This section describes ac timing characteristics for each peripheral system. For detailed information about how clocks for the bus are generated, see Chapter 7, “Internal Clock Generator (ICG) Module.”

A.10.1 Control Timing

Table A-13. Control Timing

Parameter	Symbol	Min	Typical	Max	Unit
Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	20	MHz
Real-time interrupt internal oscillator period	t_{RTI}	700		1300	µs
External reset pulse width[1]	t_{extrst}	1.5 x f_{Self_reset}		—	ns
Reset low drive[2]	t_{rstdrv}	34 x f_{Self_reset}		—	ns
Active background debug mode latch setup time	t_{MSSU}	25		—	ns
Active background debug mode latch hold time	t_{MSH}	25		—	ns
IRQ pulse width[3]	t_{ILIH}	1.5 x t_{cyc}		—	ns
Port rise and fall time (load = 50 pF)[4] Slew rate control disabled Slew rate control enabled	t_{Rise}, t_{Fall}	— —	3 30		ns

1 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

2 When any reset is initiated, internal circuitry drives the reset pin low for about 34 cycles of f_{Self_reset} and then samples the level on the reset pin about 38 cycles later to distinguish external reset requests from internal requests.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 85°C.

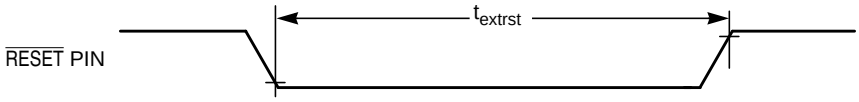


Figure A-12. Reset Timing

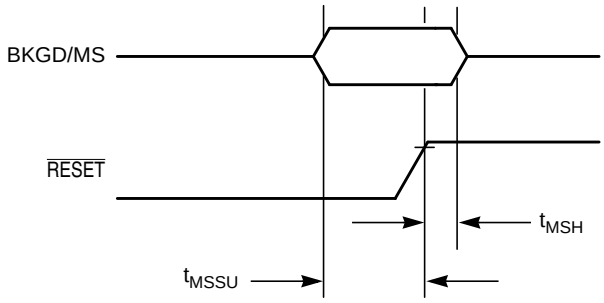


Figure A-13. Active Background Debug Mode Latch Timing