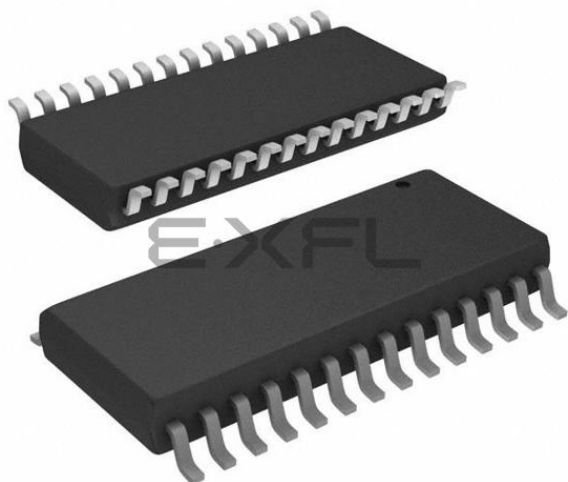




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0412sj020ec00tr

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

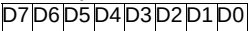
Date	Revision Level	Description	Page Number
May 2008	17	Removed Flash Microcontrollers from the title throughout the document.	All
February 2008	16	Updated the flag status for BCLR, BIT, and BSET in Table 126.	219
December 2007	15	Updated Zilog logo, Zilog text, Disclaimer section, and implemented style guide. Updated Z8 Encore! 8K Series to Z8 Encore! XP F0822 Series Flash Microcontrollers throughout the document.	All
June 2007 and August 2007	13 and 14	No Changes.	All
December 2006	12	Updated Ordering Information and minor edits done.	All

Operation	69
Timer Operating Modes	70
Reading the Timer Count Values	77
Timer Output Signal Operation	78
Timer Control Register Definitions	78
Timer 0–1 High and Low Byte Registers	78
Timer Reload High and Low Byte Registers	79
Timer 0–1 PWM High and Low Byte Registers	79
Timer 0–3 Control 0 Registers	80
Timer 0–1 Control 1 Registers	81
Watchdog Timer	83
Operation	83
Watchdog Timer Refresh	84
Watchdog Timer Time-Out Response	84
Watchdog Timer Reload Unlock Sequence	85
Watchdog Timer Control Register Definitions	86
Watchdog Timer Control Register	86
Watchdog Timer Reload Upper, High and Low Byte Registers	87
Universal Asynchronous Receiver/Transmitter	89
Architecture	89
Operation	90
Data Format	90
Transmitting Data using Polled Method	91
Transmitting Data Using Interrupt-Driven Method	92
Receiving Data using the Polled Method	93
Receiving Data Using Interrupt-Driven Method	94
Clear To Send Operation	95
Multiprocessor (9-bit) Mode	95
External Driver Enable	96
UART Interrupts	97
UART Baud Rate Generator	99
UART Control Register Definitions	100
UART Transmit Data Register	100
UART Receive Data Register	101
UART Status 0 Register	101
UART Status 1 Register	102
UART Control 0 and Control 1 Registers	103
UART Address Compare Register	105
UART Baud Rate High and Low Byte Registers	106
Infrared Encoder/Decoder	109
Architecture	109

Control Register Summary

Timer 0 High Byte

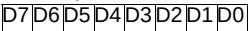
T0H (F00H - Read/Write)



Timer 0 current count value

Timer 0 Low Byte

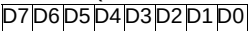
T0L (F01H - Read/Write)



Timer 0 current count value

Timer 0 Reload High Byte

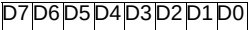
T0RH (F02H - Read/Write)



Timer 0 reload value [15:8]

Timer 0 Reload Low Byte

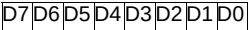
T0RL (F03H - Read/Write)



Timer 0 reload value [7:0]

Timer 0 PWM High Byte

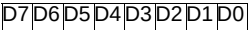
T0PWMH (F04H - Read/Write)



Timer 0 PWM value [15:8]

Timer 0 Control 0

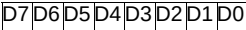
T0CTL0 (F06H - Read/Write)



Reserved
Cascade Timer
0 = Timer 0 Input signal is
GPIO pin
1 = Timer 0 Input signal is
Timer 1 out
Reserved

Timer 0 Control 1

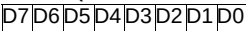
T0CTL1 (F07H - Read/Write)



Timer Mode
000 = One-Shot mode
001 = Continuous mode
010 = Counter mode
011 = PWM mode
100 = Capture mode
101 = Compare mode
110 = Gated mode
111 = Capture/Compare
mode
Prescale Value
000 = Divide by 1
001 = Divide by 2
010 = Divide by 4
011 = Divide by 8
100 = Divide by 16
101 = Divide by 32
110 = Divide by 64
111 = Divide by 128
Timer Input/Output Polarity
Operation of this bit is a
function of
the current operating mode
of the timer
Timer Enable
0 = Timer is disabled
1 = Timer is enabled

Timer 1 High Byte

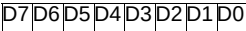
T1H (F08H - Read/Write)



Timer 1 current count value

Timer 1 Low Byte

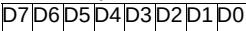
T1L (F09H - Read/Write)



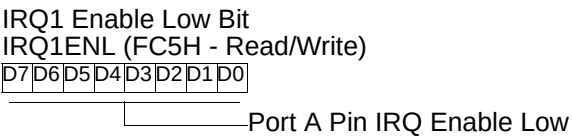
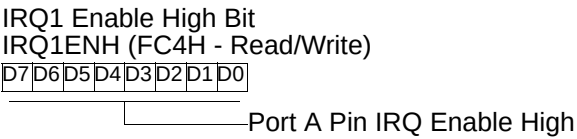
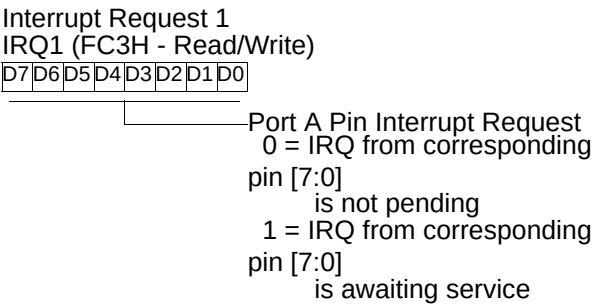
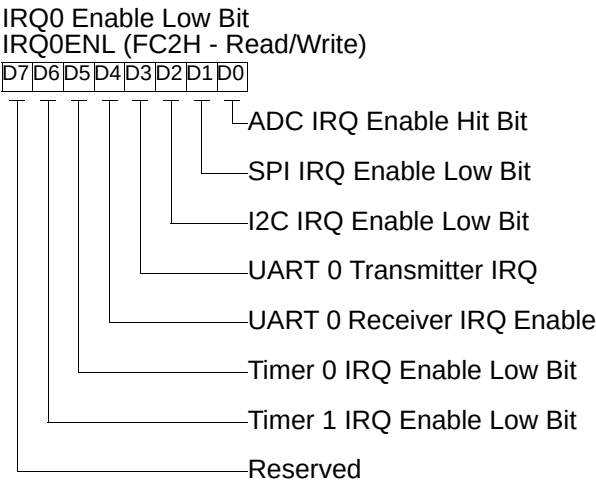
Timer 1 current count value

Timer 1 Reload High Byte

T1RH (F0AH - Read/Write)



Timer 1 reload value [15:8]



Port A Address
PAADDR (FD0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = STOP mode recovery enable
06H = Pull-up enable
07H-FFH = No function

Port A Control
PACTL (FD1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Control[7:0]
Provides Access to Port Sub-Registers

Port A Input Data
PAIN (FD2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Input Data [7:0]

Port A Output Data
PAOUT (FD3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Output Data [7:0]

Port A–C Control Registers

The Port A–C Control Registers set the GPIO port operation. The value in the corresponding Port A–C Address Register determines the control sub-registers accessible using the Port A–C Control Register (Table 15).

Table 15. Port A–C Control Registers (PxCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	PCTL							
RESET	00H							
R/W	R/W							
ADDR	FD1H, FD5H, FD9H							

PCTL[7:0]—Port Control

The Port Control Register provides access to all sub-registers that configure the GPIO Port operation.

Port A–C Data Direction Sub-Registers

The Port A–C Data Direction sub-register is accessed through the Port A–C Control register by writing 01H to the Port A–C Address Register (Table 16).

Table 16. Port A–C Data Direction Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1							
R/W	R/W							
ADDR	If 01H in Port A–C Address Register, accessible through the Port A–C Control Register							

DD[7:0]—Data Direction

These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction register setting.

0 = Output. Data in the Port A–C Output Data Register is driven onto the port pin.

1 = Input. The port pin is sampled and the value written into the Port A–C Input Data Register. The output driver is tri-stated.

Port A–C Alternate Function Sub-Registers

The Port A–C Alternate Function sub-register (Table 17) is accessed through the Port A–C Control Register by writing 02H to the Port A–C Address Register. The Port A–C Alternate Function sub-registers select the alternate functions for the selected

Table 50. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	1							
R/W	R/W*							
ADDR	FF2H							
R/W*—Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTH—WDT Reload High Byte

Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 51. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	1							
R/W	R/W*							
ADDR	FF3H							
R/W*—Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

Write Transaction with a 7-Bit Address

Figure 27 displays the data transfer format for a 7-bit addressed slave. Shaded regions indicate data transferred from the I²C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I²C Controller.

S	Slave Address	W = 0	A	Data	A	Data	A	Data	$\overline{A/A}$	P/S
---	---------------	-------	---	------	---	------	---	------	------------------	-----

Figure 27. 7-Bit Addressed Slave Data Transfer Format

Follow the steps below for a transmit operation to a 7-bit addressed slave:

1. Software asserts the IEN bit in the I²C Control Register.
2. Software asserts the TXI bit of the I²C Control Register to enable Transmit Interrupts.
3. The I²C interrupt asserts, because the I²C Data Register is empty.
4. Software responds to the TDRE bit by writing a 7-bit Slave address plus write bit (=0) to the I²C Data Register.
5. Software asserts the START bit of the I²C Control Register.
6. The I²C Controller sends the START condition to the I²C Slave.
7. The I²C Controller loads the I²C Shift register with the contents of the I²C Data Register.
8. After one bit of address has been shifted out by the SDA signal, the Transmit Interrupt is asserted (TDRE = 1).
9. Software responds by writing the transmit data into the I²C Data Register.
10. The I²C Controller shifts the rest of the address and write bit out by the SDA signal.
11. If the I²C Slave sends an acknowledge (by pulling the SDA signal low) during the next high period of SCL the I²C Controller sets the ACK bit in the I²C Status register. Continue with step 12.

If the slave does not acknowledge, the Not Acknowledge interrupt occurs (NCKI bit is set in the Status register, ACK bit is cleared). Software responds to the Not Acknowledge interrupt by setting the STOP and FLUSH bits and clearing the TXI bit. The I²C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore following steps).

12. The I²C Controller loads the contents of the I²C Shift register with the contents of the I²C Data Register.
13. The I²C Controller shifts the data out of using the SDA signal. After the first bit is sent, the Transmit Interrupt is asserted.

I²C Baud Rate High and Low Byte Registers

The I²C Baud Rate High and Low Byte registers (Tables 73 and 73) combine to form a 16-bit reload value, BRG[15:0], for the I²C Baud Rate Generator. When configured as a general purpose timer, the interrupt interval is calculated using the following equation:

$$\text{Interrupt Interval (s)} = \text{System Clock Period (s)} \times \text{BRG}[15:0]$$

Table 73. I²C Baud Rate High Byte Register (I2CBRH)

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	FFH							
R/W	R/W							
ADDR	F53H							

BRH = I²C Baud Rate High Byte

Most significant byte, BRG[15:8], of the I²C Baud Rate Generator's reload value.

► **Note:** If the DIAG bit in the I²C Diagnostic Control Register is set to 1, a read of the I2CBRH register returns the current value of the I²C Baud Rate Counter[15:8].

Table 74. I²C Baud Rate Low Byte Register (I2CBRL)

BITS	7	6	5	4	3	2	1	0
FIELD	BRL							
RESET	FFH							
R/W	R/W							
ADDR	F54H							

BRL = I²C Baud Rate Low Byte

Least significant byte, BRG[7:0], of the I²C Baud Rate Generator's reload value.

► **Note:** If the DIAG bit in the I²C Diagnostic Control Register is set to 1, a read of the I2CBRL register returns the current value of the I²C Baud Rate Counter [7:0].

I²C Diagnostic State Register

The I²C Diagnostic State register (Table 75) provides observability of internal state. This is a read only register used for I²C diagnostics and manufacturing test.

Flash Memory Address 0000H

Table 89. Option Bits at Flash Memory Address 0000H for 8K Series Flash Devices

BITS	7	6	5	4	3	2	1	0
FIELD	WDT_RES	WDT_AO	OSC_SEL[1:0]		VBO_AO	RP	Reserved	FWP
RESET	U							
R/W	R/W							
ADDR	Program Memory 0000H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

WDT_RES—Watchdog Timer Reset

- 0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request.
- 1 = Watchdog Timer time-out causes a Reset. This setting is the default for unprogrammed (erased) Flash.

WDT_AO—Watchdog Timer Always On

- 0 = Watchdog Timer is automatically enabled upon application of system power. Watchdog Timer can not be disabled.
- 1 = Watchdog Timer is enabled upon execution of the WDT instruction. Once enabled, the Watchdog Timer can only be disabled by a Reset or Stop Mode Recovery. This setting is the default for unprogrammed (erased) Flash.

OSC_SEL[1:0]—OSCILLATOR Mode Selection

- 00 = On-chip oscillator configured for use with external RC networks (<4 MHz).
- 01 = Minimum power for use with very low frequency crystals (32 kHz to 1.0 MHz).
- 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 10.0 MHz).
- 11 = Maximum power for use with high frequency crystals (8.0 MHz to 20.0 MHz). This setting is the default for unprogrammed (erased) Flash.

VBO_AO—Voltage Brownout Protection Always On

- 0 = Voltage Brownout Protection is disabled in STOP mode to reduce total power consumption.
- 1 = Voltage Brownout Protection is always enabled including during STOP mode. This setting is the default for unprogrammed (erased) Flash.

RP—Read Protect

- 0 = User program code is inaccessible. Limited control features are available through the OCD.
- 1 = User program code is accessible. All OCD commands are enabled. This setting is the default for unprogrammed (erased) Flash.

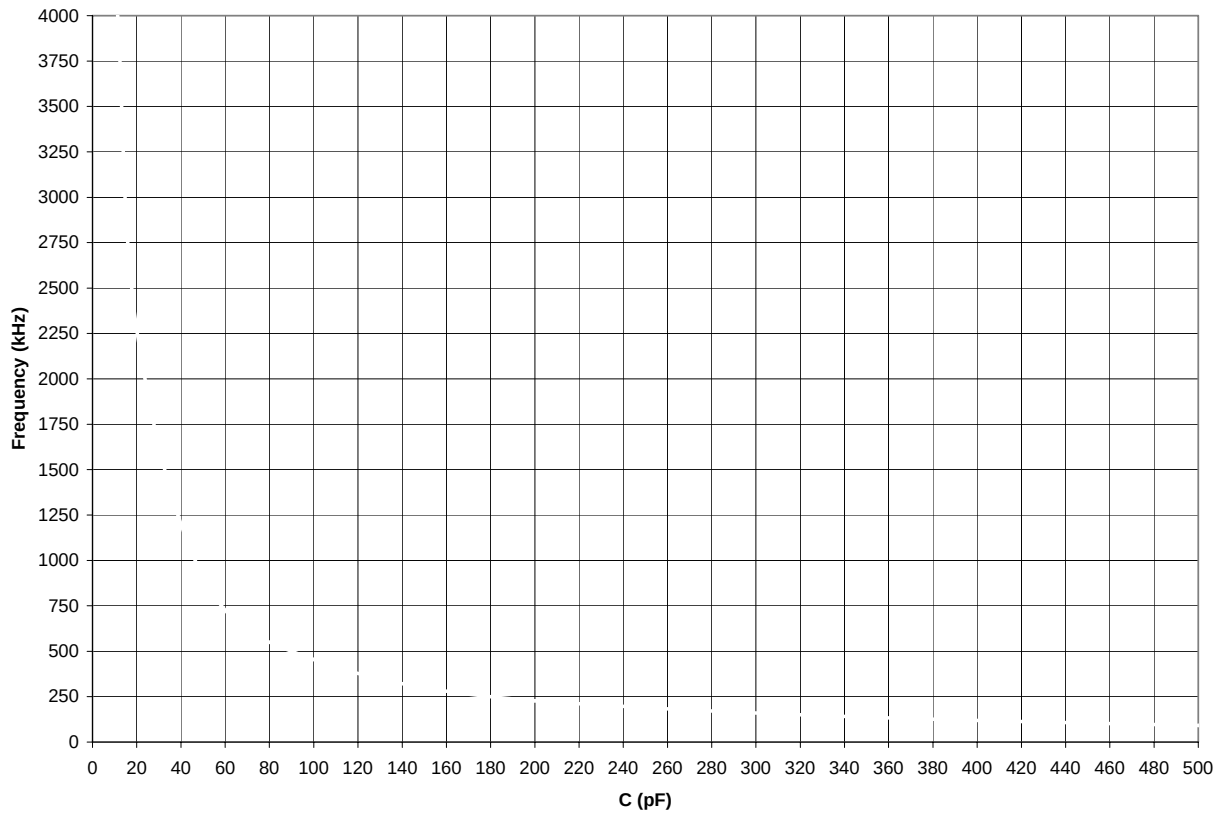


Figure 36. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45 kΩ Resistor

! Caution: *When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brownout threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.*

Debug Mode

The operating characteristics of the Z8 Encore! XP[®] F0822 Series devices in DEBUG mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions.
- The system clock operates unless in STOP mode.
- All enabled on-chip peripherals operate unless in STOP mode.
- Automatically exits HALT mode.
- Constantly refreshes the Watchdog Timer, if enabled.

Entering Debug Mode

The device enters DEBUG mode following any of the following operations:

- Writing the DBGMODE bit in the OCD Control Register to 1 using the OCD interface.
- eZ8 CPU execution of a BRK (Breakpoint) instruction.
- Match of PC to OCDCNTR register (when enabled)
- OCDCNTR register decrements to 0000H (when enabled)
- If the DBG pin is Low when the device exits Reset, the OCD automatically puts the device into DEBUG mode.

Exiting Debug Mode

The device exits DEBUG mode following any of the following operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0.
- Power-On Reset
- Voltage Brownout reset
- Asserting the RESET pin Low to initiate a Reset.
- Driving the DBG pin Low while the device is in STOP mode initiates a System Reset.

OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 Start bit, 8 data bits (least-significant bit first), and 1 STOP bit (see Figure 40).



Figure 40. OCD Data Format

DC Characteristics

Table 97 lists the DC characteristics of the Z8 Encore! XP® F0822 Series products. All voltages are referenced to V_{SS} , the primary system ground.

Table 97. DC Characteristics

Symbol	Parameter	$T_A = -40\text{ °C to }105\text{ °C}$			Units	Conditions
		Minimum	Typical	Maximum		
V_{DD}	Supply Voltage	2.7	—	3.6	V	
V_{IL1}	Low Level Input Voltage	-0.3	—	$0.3 \cdot V_{DD}$	V	For all input pins except $\overline{\text{RESET}}$, DBG, and XIN.
V_{IL2}	Low Level Input Voltage	-0.3	—	$0.2 \cdot V_{DD}$	V	For $\overline{\text{RESET}}$, DBG, and XIN.
V_{IH1}	High Level Input Voltage	$0.7 \cdot V_{DD}$	—	5.5	V	Ports A and C pins when their programmable pull-ups are disabled.
V_{IH2}	High Level Input Voltage	$0.7 \cdot V_{DD}$	—	$V_{DD} + 0.3$	V	Port B pins. Ports A and C pins when their programmable pull-ups are enabled.
V_{IH3}	High Level Input Voltage	$0.8 \cdot V_{DD}$	—	$V_{DD} + 0.3$	V	$\overline{\text{RESET}}$, DBG, and XIN pins.
V_{OL1}	Low Level Output Voltage	—	—	0.4	V	$I_{OL} = 2\text{ mA}$; $V_{DD} = 3.0\text{ V}$ High Output Drive disabled.
V_{OH1}	High Level Output Voltage	2.4	—	—	V	$I_{OH} = -2\text{ mA}$; $V_{DD} = 3.0\text{ V}$ High Output Drive disabled.
V_{OL2}	Low Level Output Voltage High Drive	—	—	0.6	V	$I_{OL} = 20\text{ mA}$; $V_{DD} = 3.3\text{ V}$ High Output Drive enabled $T_A = -40\text{ °C to }+70\text{ °C}$
V_{OH2}	High Level Output Voltage High Drive	2.4	—	—	V	$I_{OH} = -20\text{ mA}$; $V_{DD} = 3.3\text{ V}$ High Output Drive enabled; $T_A = -40\text{ °C to }+70\text{ °C}$
V_{OL3}	Low Level Output Voltage High Drive	—	—	0.6	V	$I_{OL} = 15\text{ mA}$; $V_{DD} = 3.3\text{ V}$ High Output Drive enabled; $T_A = +70\text{ °C to }+105\text{ °C}$
V_{OH3}	High Level Output Voltage High Drive	2.4	—	—	V	$I_{OH} = 15\text{ mA}$; $V_{DD} = 3.3\text{ V}$ High Output Drive enabled; $T_A = +70\text{ °C to }+105\text{ °C}$

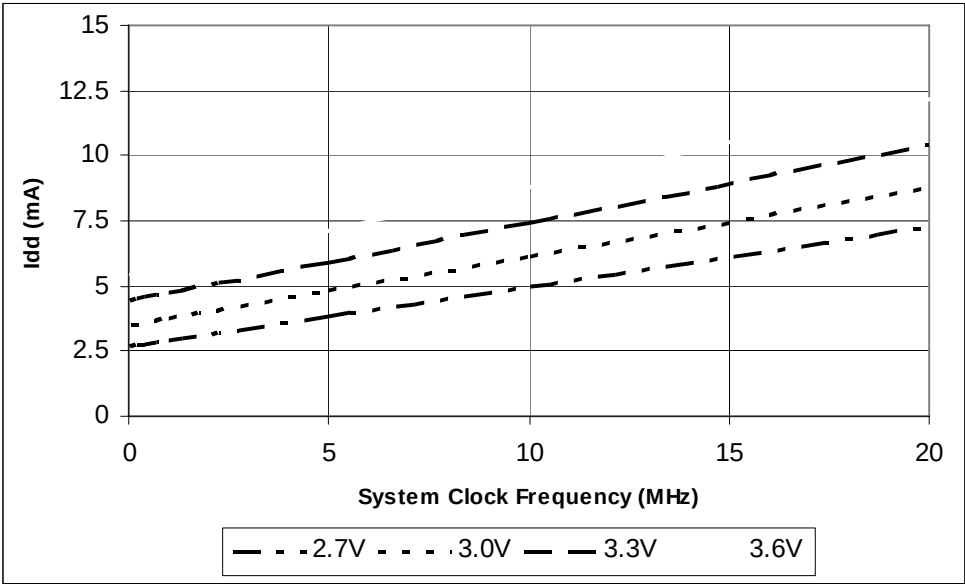


Figure 41. Typical Active Mode I_{DD} Versus System Clock Frequency

Figure 42 displays the maximum active mode current consumption across the full operating temperature range of the device and versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

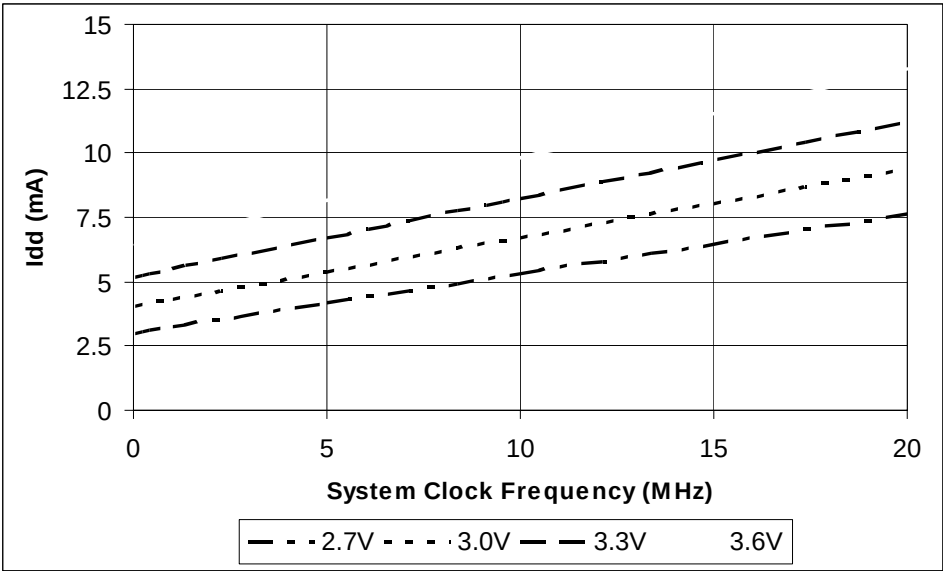


Figure 42. Maximum Active Mode I_{DD} Versus System Clock Frequency

Figure 45 displays the maximum current consumption in STOP mode with the VBO and Watchdog Timer enabled versus the power supply voltage. All GPIO pins are configured as outputs and driven High.

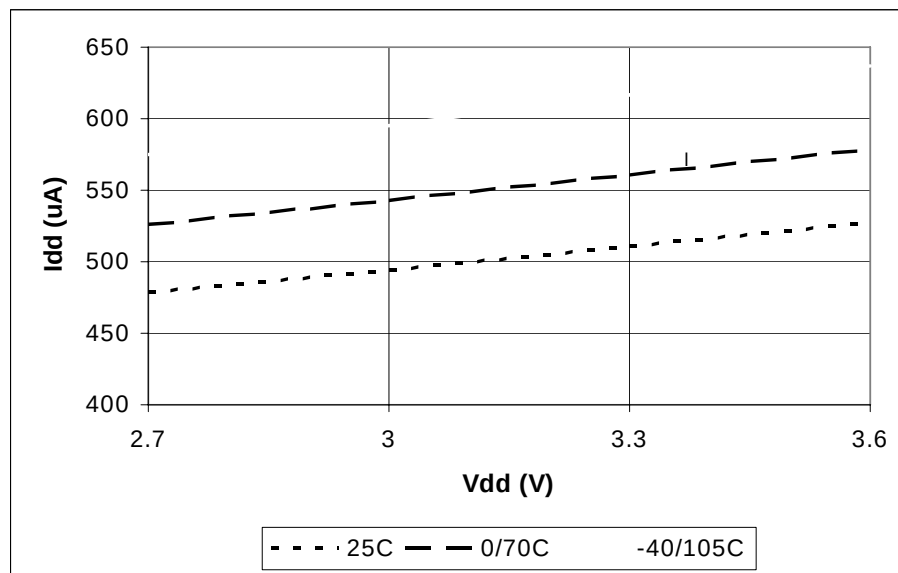


Figure 45. Maximum STOP Mode I_{DD} with VBO Enabled versus Power Supply Voltage

Figure 46 on page 193 displays the maximum current consumption in STOP mode with the VBO disabled and Watchdog Timer enabled versus the power supply voltage. All GPIO pins are configured as outputs and driven High. Disabling the Watchdog Timer and its internal RC oscillator in STOP mode will provide some additional reduction in STOP mode current consumption. This small current reduction is indistinguishable on the scale of Figure 46 on page 193.

Table 101. Flash Memory Electrical Characteristics and Timing (Continued)

Parameter	V _{DD} = 2.7 - 3.6V T _A = -40 °C to 105 °C			Units	Notes
	Minimum	Typical	Maximum		
Data Retention	100	–	–	years	25 °C
Endurance	10,000	–	–	cycles	Program / erase cycles

Table 102 provides information on the Reset and Stop Mode Recovery pin timing and Table 103 provides information on the Watchdog Timer Electrical Characteristics and Timing.

Table 102. Reset and Stop Mode Recovery Pin Timing

Symbol	Parameter	T _A = -40 °C to 105 °C			Units	Conditions
		Minimum	Typical	Maximum		
T _{RESET}	Reset pin assertion to initiate a System Reset	4	–	–	T _{CLK}	Not in STOP mode. T _{CLK} = System Clock period.
T _{SMR}	Stop Mode Recovery pin Pulse Rejection Period	10	20	40	ns	RESET, DBG and GPIO pins configured as SMR sources.

¹ When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7 V.

Table 103. Watchdog Timer Electrical Characteristics and Timing

Symbol	Parameter	V _{DD} = 2.7–3.6 V T _A = -40 °C to 105 °C			Units	Conditions
		Minimum	Typical	Maximum		
F _{WDT}	WDT Oscillator Frequency	5	10	20	kHz	
I _{WDT}	WDT Oscillator Current including internal RC oscillator	–	< 1	5	μA	

Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
CALL dst	SP ← SP -2 @SP ← PC PC ← dst	IRR		D4	-	-	-	-	-	-	2	6
		DA		D6							3	3
CCF	C ← ~C			EF	*	-	-	-	-	-	1	2
CLR dst	dst ← 00H	R		B0	-	-	-	-	-	-	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	-	*	*	0	-	-	2	2
		IR		61							2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	-	-	2	3
		r	lr	A3							2	4
		R	R	A4							3	3
		R	IR	A5							3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	-	-	3	3
		r	lr	1F A3							3	4
		R	R	1F A4							4	3
		R	IR	1F A5							4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	-	-	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	-	-	4	3
		ER	IM	A9							4	3
DA dst	dst ← DA(dst)	R		40	*	*	*	X	-	-	2	2
		IR		41							2	3
DEC dst	dst ← dst - 1	R		30	-	*	*	*	-	-	2	2
		IR		31							2	3

Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LDX dst, src	$\text{dst} \leftarrow \text{src}$	r	ER	84	-	-	-	-	-	-	3	2
		lr	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	lr	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$\text{dst} \leftarrow \text{src} + \text{X}$	r	X(r)	98	-	-	-	-	-	-	3	3
		rr	X(rr)	99							3	5
MULT dst	$\text{dst}[15:0] \leftarrow \text{dst}[15:8] * \text{dst}[7:0]$	RR		F4	-	-	-	-	-	-	2	8
NOP	No operation			0F	-	-	-	-	-	-	1	2
OR dst, src	$\text{dst} \leftarrow \text{dst OR src}$	r	r	42	-	*	*	0	-	-	2	3
		r	lr	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	$\text{dst} \leftarrow \text{dst OR src}$	ER	ER	48	-	*	*	0	-	-	4	3
		ER	IM	49							4	3
POP dst	$\text{dst} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 1$	R		50	-	-	-	-	-	-	2	2
		IR		51							2	3

Packaging

Figure 60 displays the 20-pin SSOP package available for Z8 Encore! XP[®] F0822 Series devices.

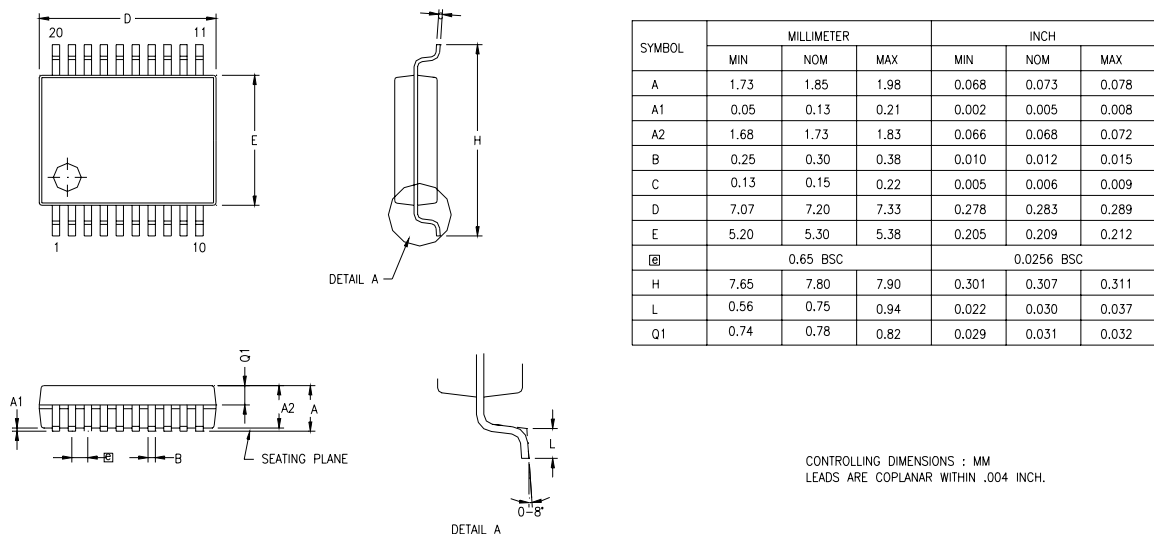


Figure 60. 20-Pin Small Shrink Outline Package (SSOP)

Figure 61 displays the 20-pin PDIP package available for Z8 Encore! XP F0822 Series devices.

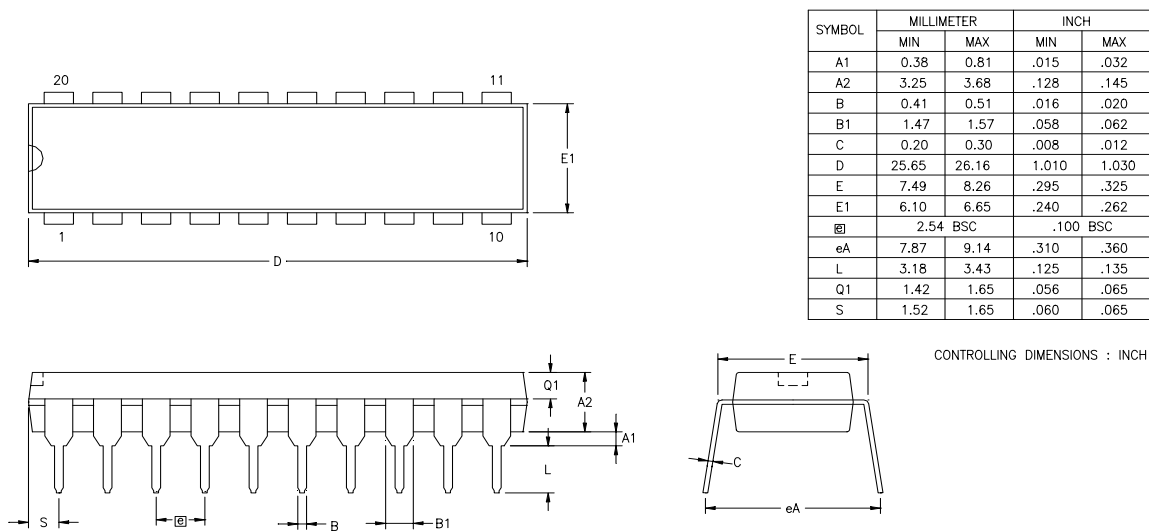


Figure 61. 20-Pin Plastic Dual-Inline Package (PDIP)

Ordering Information

Order Z8 Encore! XP F0822 Series from Zilog[®], using the following part numbers. For more information regarding ordering, consult your local Zilog sales office. Zilog website at www.zilog.com lists all regional offices and provides additional Z8 Encore! XP product information.

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I ² C	SPI	UARTs with IrDA	Description
Z8F08xx with 8 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0821HH020SC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020SC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package
Extended Temperature: -40° to +105°C										
Z8F0821HH020EC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020EC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package