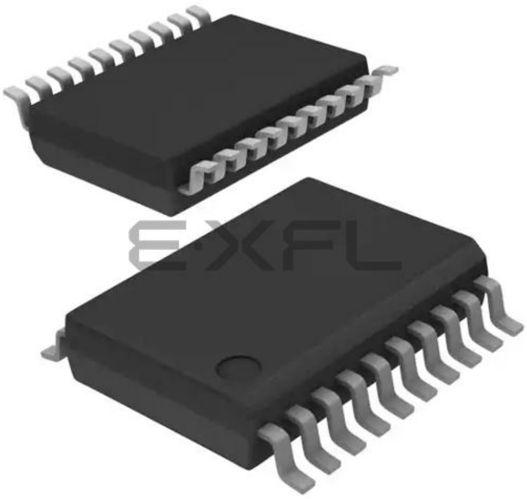
Zilog - Z8F0421HH020EC Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0421hh020ec

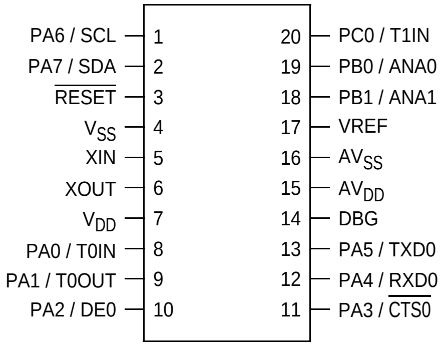


Figure 2. Z8F0821 and Z8F0421 in 20-Pin SSOP and PDIP Packages

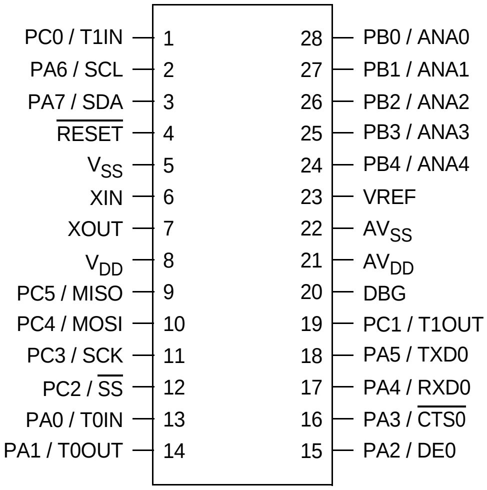


Figure 3. Z8F0822 and Z8F0422 in 28-Pin SOIC and PDIP Packages

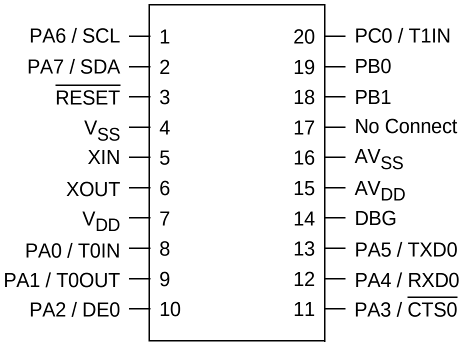
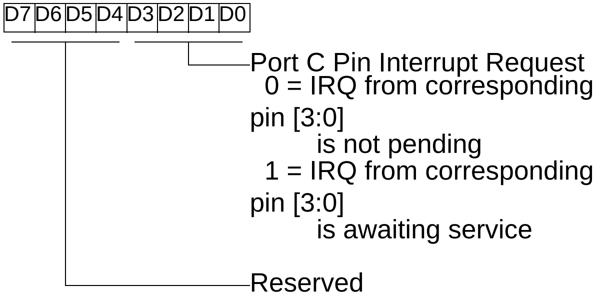


Figure 4. Z8F0811 and Z8F0411 in 20-Pin SSOP and PDIP Packages

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FCE	Reserved	—	00	
FCF	Interrupt Control	IRQCTL	00	67
GPIO Port A				
FD0	Port A Address	PAADDR	00	50
FD1	Port A Control	PACTL	00	51
FD2	Port A Input Data	PAIN	XX	54
FD3	Port A Output Data	PAOUT	00	55
GPIO Port B				
FD4	Port B Address	PBADDR	00	50
FD5	Port B Control	PBCTL	00	51
FD6	Port B Input Data	PBIN	XX	54
FD7	Port B Output Data	PBOUT	00	55
GPIO Port C				
FD8	Port C Address	PCADDR	00	50
FD9	Port C Control	PCCTL	00	51
FDA	Port C Input Data	PCIN	XX	54
FDB	Port C Output Data	PCOUT	00	55
FDC-FEF	Reserved	—	XX	
Watchdog Timer (WDT)				
FF0	Watchdog Timer Control	WDTCTL	XXX00000b	86
FF1	Watchdog Timer Reload Upper Byte	WDTU	FF	87
FF2	Watchdog Timer Reload High Byte	WDTH	FF	87
FF3	Watchdog Timer Reload Low Byte	WDTL	FF	87
FF4-FF7	Reserved	—	XX	
Flash Memory Controller				
FF8	Flash Control	FCTL	00	159
FF8	Flash Status	FSTAT	00	160
FF9	Page Select	FPS	00	160
FF9 (if enabled)	Flash Sector Protect	FPROT	00	161
FFA	Flash Programming Frequency High Byte	FFREQH	00	161
FFB	Flash Programming Frequency Low Byte	FFREQL	00	161
Read-Only Memory				
FF8	Reserved	—	XX	
FF9	Page Select	RPS	00	160
FFA-FFB	Reserved	—	XX	
eZ8 CPU				
XX=Undefined				

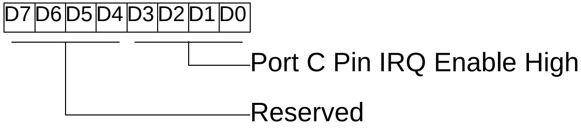
Interrupt Request 2
IRQ2 (FC6H - Read/Write)



Port C Pin Interrupt Request
0 = IRQ from corresponding pin [3:0] is not pending
1 = IRQ from corresponding pin [3:0] is awaiting service

Reserved

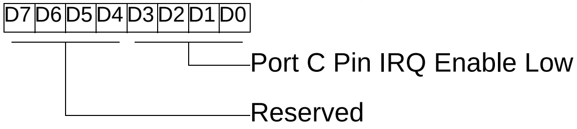
IRQ2 Enable High Bit
IRQ2ENH (FC7H - Read/Write)



Port C Pin IRQ Enable High

Reserved

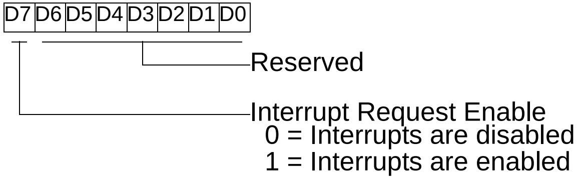
IRQ2 Enable Low Bit
IRQ2ENL (FC8H - Read/Write)



Port C Pin IRQ Enable Low

Reserved

Interrupt Control
IRQCTL (FCFH - Read/Write)



Reserved

Interrupt Request Enable
0 = Interrupts are disabled
1 = Interrupts are enabled

Port A Address
PAADDR (FD0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = STOP mode recovery enable
06H = Pull-up enable
07H-FFH = No function

Port A Control
PACTL (FD1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Control[7:0]
Provides Access to Port Sub-Registers

Port A Input Data
PAIN (FD2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Input Data [7:0]

Port A Output Data
PAOUT (FD3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

Port A Output Data [7:0]

External Pin Reset

The $\overline{\text{RESET}}$ pin contains a Schmitt-triggered input, an internal pull-up, an analog filter, and a digital filter to reject noise. After the $\overline{\text{RESET}}$ pin is asserted for at least 4 system clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, Z8 Encore! XP F0822 Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state immediately following $\overline{\text{RESET}}$ pin deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the `EXT` status bit in the Watchdog Timer Control Register (WDTCTL) is set to 1.

On-Chip Debugger Initiated Reset

A POR is initiated using the OCD by setting the `RST` bit in the OCD Control Register. The OCD block is not reset but the rest of the chip goes through a normal system reset. The `RST` bit automatically clears during the system reset. Following the system reset, the `POR` bit in the WDT Control Register is set.

Stop Mode Recovery

STOP mode is entered by execution of a `STOP` instruction by the eZ8 CPU. For detailed information on STOP mode, see Low-Power Modes on page 45. During Stop Mode Recovery, the device is held in reset for 66 cycles of the WDT oscillator followed by 16 cycles of the system clock. Stop Mode Recovery only affects the contents of the WDT Control Register and does not affect any other values in the Register File, including the Stack Pointer, Register Pointer, Flags, Peripheral Control Registers, and General-Purpose RAM.

The eZ8 CPU fetches the Reset vector at Program Memory addresses `0002H` and `0003H` and loads that value into the Program Counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the `STOP` bit in the WDT Control Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information on each of the Stop Mode Recovery sources.

Table 10. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP mode	WDT time-out when configured for Reset	Stop Mode Recovery
	WDT time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery

Interrupt Controller

The interrupt controller on Z8 Encore! XP® F0822 Series products prioritizes the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of the interrupt controller include the following:

- 19 unique interrupt vectors:
  - 12 GPIO port pin interrupt sources.
  - 7 On-chip peripheral interrupt sources.
- Flexible GPIO interrupts:
  - 8 selectable rising and falling edge GPIO interrupts.
  - 4 dual-edge interrupts.
- Three levels of individually programmable interrupt priority.
- WDT is configured to generate an interrupt.

Interrupt Requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an Interrupt Service Routine (ISR). Usually this ISR is involved with the exchange of data, status information, or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the interrupt control has no effect on operation. For more information on interrupt servicing, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

Interrupt Vector Listing

Table 24 lists all the interrupts available in order of priority. The interrupt vector is stored with the most significant byte (MSB) at the even Program Memory address and the least significant byte (LSB) at the following odd Program Memory address.

Table 24. Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Address	Interrupt Source
Highest	0002H	Reset (not an interrupt)
	0004H	WDT (see Watchdog Timer on page 83)
	0006H	Illegal Instruction Trap (not an interrupt)

Table 29. IRQ0 Enable High Bit Register (IRQ0ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1ENH	T0ENH	U0RENH	U0TENH	I2CENH	SPIENH	ADCENH
RESET	0							
R/W	R/W							
ADDR	FC1H							

Reserved—Must be 0
T1ENH—Timer 1 Interrupt Request Enable High Bit
T0ENH—Timer 0 Interrupt Request Enable High Bit
U0RENH—UART 0 Receive Interrupt Request Enable High Bit
U0TENH—UART 0 Transmit Interrupt Request Enable High Bit
I2CENH—I^{2}C Interrupt Request Enable High Bit
SPIENH—SPI Interrupt Request Enable High Bit
ADCENH—ADC Interrupt Request Enable High Bit

Table 30. IRQ0 Enable Low Bit Register (IRQ0ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved	T1ENL	T0ENL	U0RENL	U0TENL	I2CENL	SPIENL	ADCENL
RESET	0							
R/W	R/W							
ADDR	FC2H							

Reserved—Must be 0
T1ENL—Timer 1 Interrupt Request Enable Low Bit
T0ENL—Timer 0 Interrupt Request Enable Low Bit
U0RENL—UART 0 Receive Interrupt Request Enable Low Bit
U0TENL—UART 0 Transmit Interrupt Request Enable Low Bit
I2CENL—I^{2}C Interrupt Request Enable Low Bit
SPIENL—SPI Interrupt Request Enable Low Bit
ADCENL—ADC Interrupt Request Enable Low Bit

IRQ1 Enable High and Low Bit Registers

Table 31 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit Registers (Table 32 and Table 33) form a priority encoded enabling for interrupts in the Interrupt Request 1 Register. Priority is generated by setting bits in each register.

Table 31. IRQ1 Enable and Priority Encoding

IRQ1ENH[*x*]	IRQ1ENL[*x*]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

where *x* indicates the register bits from 0 through 7.

Table 32. IRQ1 Enable High Bit Register (IRQ1ENH)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7ENH	PA6ENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0							
R/W	R/W							
ADDR	FC4H							

PA*x*ENH—Port A Bit[*x*] Interrupt Request Enable High Bit

Table 33. IRQ1 Enable Low Bit Register (IRQ1ENL)

BITS	7	6	5	4	3	2	1	0
FIELD	PA7ENL	PA6ENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0							
R/W	R/W							
ADDR	FC5H							

PA*x*ENL—Port A Bit[*x*] Interrupt Request Enable Low Bit

IRQ2 Enable High and Low Bit Registers

Table 34 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit Registers (Table 35 and Table 36) form a priority encoded enabling for interrupts in the Interrupt Request 2 register. Priority is generated by setting bits in each register.

4. If required, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control Register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

$$\text{COUNTER Mode Timer Input Transitions} = \text{Current Count Value} - \text{Start Value}$$

PWM Mode

In PWM mode, the timer outputs a Pulse-Width Modulator output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte Registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte Registers is reset to `0001H` and counting resumes.

If the `TPOL` bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and then transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to `0001H`.

If the `TPOL` bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and then transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to `0001H`.

Follow the steps below for configuring a timer for PWM mode and initiating the PWM operation:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for PWM mode.
   - Set the prescale value.
   - Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function.
2. Write to the Timer High and Low Byte Registers to set the starting count value (typically `0001H`). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of `0001H`.

TH and TL—Timer High and Low Bytes
These 2 bytes, {TMRH[7:0], TMRL[7:0]}, contain the current 16-bit timer count value.

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) Registers (Table 41) store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit Timer Reload value.

In COMPARE mode, the Timer Reload High and Low Byte Registers store the 16-bit Compare value.

Table 41. Timer 0–1 Reload High Byte Register (TxRH)

BITS	7	6	5	4	3	2	1	0
FIELD	TRH							
RESET	1							
R/W	R/W							
ADDR	F02H, F0AH							

Table 42. Timer 0–1 Reload Low Byte Register (TxRL)

BITS	7	6	5	4	3	2	1	0
FIELD	TRL							
RESET	1							
R/W	R/W							
ADDR	F03H, F0BH							

TRH and TRL—Timer Reload Register High and Low
These two bytes form the 16-bit Reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to `0001H`. In COMPARE mode, these two bytes form the 16-bit Compare value.

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers (Table 43 and Table 44) are used for Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 61. UART Baud Rates (Continued)

3.579545 MHz System Clock				1.8432 MHz System Clock			
Desired Rate	BRG Divisor	Actual Rate	Error	Desired Rate	BRG Divisor	Actual Rate	Error
(kHz)	(Decimal)	(kHz)	(%)	(kHz)	(Decimal)	(kHz)	(%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	223.72	-10.51	250.0	N/A	N/A	N/A
115.2	2	111.9	-2.90	115.2	1	115.2	0.00
57.6	4	55.9	-2.90	57.6	2	57.6	0.00
38.4	6	37.3	-2.90	38.4	3	38.4	0.00
19.2	12	18.6	-2.90	19.2	6	19.2	0.00
9.60	23	9.73	1.32	9.60	12	9.60	0.00
4.80	47	4.76	-0.83	4.80	24	4.80	0.00
2.40	93	2.41	0.23	2.40	48	2.40	0.00
1.20	186	1.20	0.23	1.20	96	1.20	0.00
0.60	373	0.60	-0.04	0.60	192	0.60	0.00
0.30	746	0.30	-0.04	0.30	384	0.30	0.00

I^{2}C Controller sets the NCKI bit and clears the ACK bit in the I^{2}C Status register. Software responds to the Not Acknowledge interrupt by setting the STOP and FLUSH bits and clearing the TXI bit. The I2C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore the following steps).

17. The I^{2}C Controller shifts the data out by the SDA signal. After the first bit is sent, the Transmit Interrupt is asserted.
18. If more bytes remain to be sent, return to step 14.
19. If the last byte is currently being sent, software sets the STOP bit of the I^{2}C Control Register (or START bit to initiate a new transaction). In the STOP case, software also clears the TXI bit of the I^{2}C Control Register at the same time.
20. The I^{2}C Controller completes transmission of the last data byte on the SDA signal.
21. The slave can either Acknowledge or Not Acknowledge the last byte. Because either the STOP or START bit is already set, the NCKI interrupt does not occur.
22. The I^{2}C Controller sends the STOP (or RESTART) condition to the I^{2}C bus and clears the STOP (or START) bit.

Read Transaction with a 7-Bit Address

Figure 30 displays the data transfer format for a read operation to a 7-bit addressed slave. The shaded regions indicate data transferred from the I^{2}C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I^{2}C Controller.

S	Slave Address	R = 1	A	Data	A	Data	$\overline{A}$	P/S

Figure 30. Receive Data Transfer Format for a 7-Bit Addressed Slave

Follow the steps below for a read operation to a 7-bit addressed slave:

1. Software writes the I^{2}C Data Register with a 7-bit Slave address plus the read bit (=1).
2. Software asserts the START bit of the I^{2}C Control Register.
3. If this is a single byte transfer, Software asserts the NAK bit of the I^{2}C Control Register so that after the first byte of data has been read by the I^{2}C Controller, a Not Acknowledge is sent to the I^{2}C Slave.
4. The I^{2}C Controller sends the START condition.
5. The I^{2}C Controller shifts the address and read bit out the SDA signal.
6. If the I^{2}C Slave acknowledges the address by pulling the SDA signal Low during the next high period of SCL, the I^{2}C Controller sets the ACK bit in the I^{2}C Status register. Continue with step 7.

RD—Read
This bit indicates the direction of transfer of the data. It is active High during a read. The status of this bit is determined by the least-significant bit of the I^{2}C Shift register after the START bit is set.

TAS—Transmit Address State
This bit is active High while the address is being shifted out of the I^{2}C Shift Register.

DSS—Data Shift State
This bit is active High while data is being shifted to or from the I^{2}C Shift Register.

NCKI—NACK Interrupt
This bit is set high when a Not Acknowledge condition is received or sent and neither the START nor the STOP bit is active. When set, this bit generates an interrupt that can only be cleared by setting the START or STOP bit, allowing you to specify whether you want to perform a STOP or a repeated START.

I^{2}C Control Register

The I^{2}C Control Register (Table 72) enables the I^{2}C operation.

Table 72. I^{2}C Control Register (I2CCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	IEN	START	STOP	BIRQ	TXI	NAK	FLUSH	FILTEN
RESET	0							
R/W	R/W	R/W1	R/W1	R/W	R/W	R/W1	W1	R/W
ADDR	F52H							

IEN—I^{2}C Enable
1 = The I^{2}C transmitter and receiver are enabled.
0 = The I^{2}C transmitter and receiver are disabled.

START—Send Start Condition
This bit sends the Start condition. Once asserted, it is cleared by the I^{2}C Controller after it sends the START condition or if the IEN bit is deasserted. If this bit is 1, it cannot be cleared to 0 by writing to the register. After this bit is set, the Start condition is sent if there is data in the I^{2}C Data or I^{2}C Shift register. If there is no data in one of these registers, the I^{2}C Controller waits until the data register is written. If this bit is set while the I^{2}C Controller is shifting out data, it generates a START condition after the byte shifts and the acknowledge phase completes. If the STOP bit is also set, it also waits until the STOP condition is sent before sending the START condition.

STOP—Send Stop Condition
This bit causes the I^{2}C Controller to issue a STOP condition after the byte in the I^{2}C Shift register has completed transmission or after a byte is received in a receive operation. Once

5. Re-write the page written in step 2 to the Page Select Register.
6. Write Flash Memory using LDC or LDCI instructions to program the Flash.
7. Repeat step 6 to program additional memory locations on the same page.
8. Write `00H` to the Flash Control Register to lock the Flash Controller.

Page Erase

Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value `FFH`. The Page Select Register identifies the page to be erased. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. Interrupts that occur when the Page Erase operation is in progress are serviced once the Page Erase operation is complete. When the Page Erase operation is complete, the Flash Controller returns to its locked state. Only pages located in unprotected sectors can be erased.

Follow the steps below to perform a Page Erase operation:

1. Write `00H` to the Flash Control Register to reset the Flash Controller.
2. Write the page to be erased to the Page Select Register.
3. Write the first unlock command `73H` to the Flash Control Register.
4. Write the second unlock command `8CH` to the Flash Control Register.
5. Re-write the page written in step 2 to the Page Select Register.
6. Write the Page Erase command `95H` to the Flash Control Register.

Mass Erase

The Flash memory cannot be Mass Erased by user code.

Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Programming algorithms by controlling the Flash programming signals directly.

Flash Controller Bypass is recommended for gang programming applications and large volume customers who do not require in-circuit programming of the Flash memory.

For more information on bypassing the Flash Controller, refer to *Third-Party Flash Programming Support for Z8 Encore! XP*, available for download at www.zilog.com.

Flash Controller Behavior in Debug Mode

The following changes in behavior of the Flash Controller occur when the Flash Controller is accessed using the OCD:

- The Flash Write Protect option bit is ignored
- The Flash Sector Protect Register is ignored for programming and erase operations
- Programming operations are not limited to the page selected in the Page Select Register
- Bits in the Flash Sector Protect Register can be written to 1 or 0
- The second write of the Page Select Register to unlock the Flash Controller is not necessary
- The Page Select Register is written when the Flash Controller is unlocked
- The Mass Erase command is enabled

Flash Control Register Definitions

Flash Control Register

The Flash Control Register (Table 83) is used to unlock the Flash Controller for programming and erase operations, or to select the Flash Sector Protect Register. The Write-only Flash Control Register shares its Register File address with the Read-only Flash Status Register.

Table 83. Flash Control Register (FCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	FCMD							
RESET	0							
R/W	W							
ADDR	FF8H							

FCMD—Flash Command
73H = First unlock command.
8CH = Second unlock command.
95H = Page erase command.
63H = Mass erase command
5EH = Flash Sector Protect Register select.

* All other commands, or any command out of sequence, lock the Flash Controller.

automatically set to 1. If this bit is set, the OCDCNTR register does not count when the CPU is running.
0 = OCDCNTR is setup as counter
1 = OCDCNTR generates hardware break when PC == OCDCNTR

BRKZRO—Break when OCDCNTR == `0000H`
If this bit is set, then the OCD automatically sets the DBGMODE bit when the OCDCNTR register counts down to `0000H`. If this bit is set, the OCDCNTR register is not reset when the part leaves DEBUG Mode.
0 = OCD does not generate BRK when OCDCNTR decrements to 0000H
1 = OCD sets DBGMODE to 1 when OCDCNTR decrements to 0000H

Reserved
These bits are reserved and must be 0.

RST—Reset
Setting this bit to 1 resets the Z8 Encore! XP® F0822 Series device. The device goes through a normal POR sequence with the exception that the OCD is not reset. This bit is automatically cleared to 0 when the reset finishes.
0 = No effect.
1 = Reset the Z8 Encore! XP F0822 Series device.

OCD Status Register

The OCD Status register reports status information about the current state of the debugger and the system.

Table 95. OCD Status Register (OCDSTAT)

BITS	7	6	5	4	3	2	1	0
FIELD	IDLE	HALT	RPEN	Reserved				
RESET	0							
R/W	R							

IDLE—CPU Idling
This bit is set if the part is in DEBUG mode (DBGMODE is 1), or if a BRK instruction occurred since the last time OCDCTL was written. This can be used to determine if the CPU is running or if it is idling.
0 = The eZ8 CPU is running.
1 = The eZ8 CPU is either stopped or looping on a BRK instruction.

HALT—HALT Mode
0 = The device is not in HALT mode.
1 = The device is in HALT mode.

Table 97. DC Characteristics (Continued)

Symbol	Parameter	T_A = -40 °C to 105 °C			Units	Conditions
		Minimum	Typical	Maximum		
V_{RAM}	RAM Data Retention	0.7	–	–	V	
I_{IL}	Input Leakage Current	-5	–	+5	µA	V_{DD} = 3.6 V; V_{IN} = VDD or VSS[1]
I_{TL}	Tri-State Leakage Current	-5	–	+5	µA	V_{DD} = 3.6 V
C_{PAD}	GPIO Port Pad Capacitance	–	8.0[2]	–	pF	
C_{XIN}	XIN Pad Capacitance	–	8.0[2]	–	pF	
C_{XOUT}	XOUT Pad Capacitance	–	9.5[2]	–	pF	
I_{PU1}	Weak Pull-up Current	9	20	50	µA	VDD = 2.7–3.6 V. T_A = 0 °C to +70 °C
I_{PU2}	Weak Pull-up Current	7	20	75	µA	VDD = 2.7–3.6 V. T_A = -40 °C to +105 °C

[1] This condition excludes all pins that have on-chip pull-ups, when driven Low.

[2] These values are provided for design guidance only and are not tested in production.

Figure 41 on page 189 displays the typical active mode current consumption while operating at 25 ºC, 3.3 V, versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

Figure 44 displays the maximum HALT mode current consumption across the full operating temperature range of the device and versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

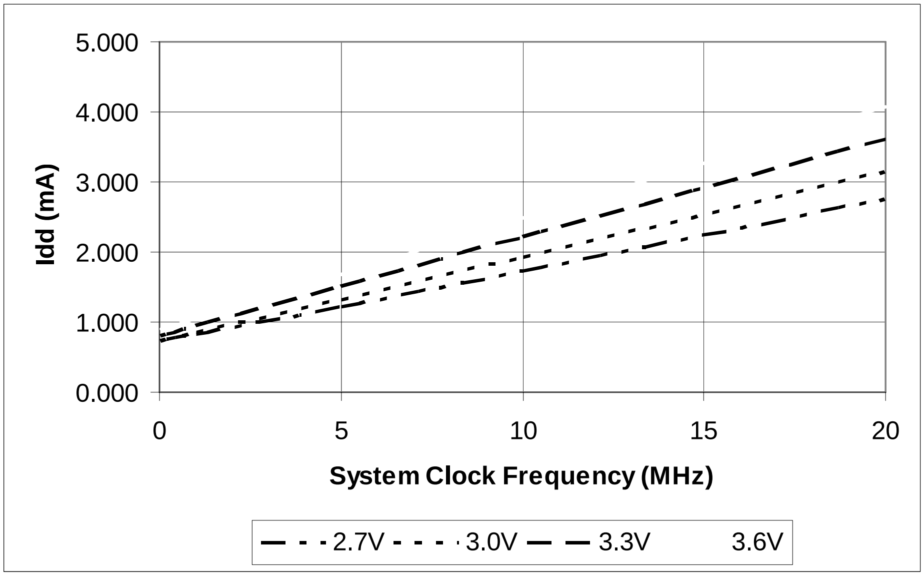


Figure 44. Maximum HALT Mode I_{CC} Versus System Clock Frequency

Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Opcode(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
DECW dst	dst ← dst - 1	RR		80	-	*	*	*	-	-	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	-	-	-	-	-	-	1	2
DJNZ dst, RA	dst ← dst – 1 if dst ≠ 0 PC ← PC + X	r		0A-FA	-	-	-	-	-	-	2	3
EI	IRQCTL[7] ← 1			9F	-	-	-	-	-	-	1	2
HALT	HALT Mode			7F	-	-	-	-	-	-	1	2
INC dst	dst ← dst + 1	R		20	-	*	*	*	-	-	2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	dst ← dst + 1	RR		A0	-	*	*	*	-	-	2	5
		IRR		A1							2	6
IRET	FLAGS ← @SP SP ← SP + 1 PC ← @SP SP ← SP + 2 IRQCTL[7] ← 1			BF	*	*	*	*	*	*	1	5
JP dst	PC ← dst	DA		8D	-	-	-	-	-	-	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true PC ← dst	DA		0D-FD	-	-	-	-	-	-	3	2
JR dst	PC ← PC + X	DA		8B	-	-	-	-	-	-	2	2
JR cc, dst	if cc is true PC ← PC + X	DA		0B-FB	-	-	-	-	-	-	2	2