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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0422sj020sc

I2C Diagnostic Control Register 145
Analog-to-Digital Converter 147
Architecture 147
Operation 148
Automatic Power-Down 148
Single-Shot Conversion 148
Continuous Conversion 148
ADC Control Register Definitions 150
ADC Control Register 150
ADC Data High Byte Register 151
ADC Data Low Bits Register 151
Flash Memory 153
Information Area 154
Operation 155
Timing Using the Flash Frequency Registers 155
Flash Read Protection 156
Flash Write/Erase Protection 156
Byte Programming 157
Page Erase 158
Mass Erase 158
Flash Controller Bypass 158
Flash Controller Behavior in Debug Mode 159
Flash Control Register Definitions 159
Flash Control Register 159
Flash Status Register 160
Page Select Register 160
Flash Sector Protect Register 161
Flash Frequency High and Low Byte Registers 161
Option Bits 163
Operation 163
Option Bit Configuration By Reset 163
Option Bit Address Space 163
Flash Memory Address 0000H 164
Flash Memory Address 0001H 165
On-Chip Oscillator 167
Operating Modes 167
Crystal Oscillator Operation 167
Oscillator Operation with an External RC Network 168
On-Chip Debugger 171
Architecture 171
Operation 171

The eZ8 CPU features include:

- Direct register-to-register architecture allows each register to function as an accumulator, improving execution time and decreasing the required Program Memory.
- Software stack allows much greater depth in subroutine calls and interrupts than hardware stacks.
- Compatible with existing Z8® code.
- Expanded internal Register File allows access of up to 4 KB.
- New instructions improve execution efficiency for code developed using higher-level programming languages, including C.
- Pipelined instruction fetch and execution.
- New instructions for improved performance including BIT, BSWAP, BTJ, CPC, LDC, LDCI, LEA, MULT, and SRL.
- New instructions support 12-bit linear addressing of the Register File.
- Up to 10 MIPS operation.
- C-Compiler friendly.
- 2 to 9 clock cycles per instruction.

For more information regarding the eZ8 CPU, refer to *eZ8 CPU Core User Manual (UM0128)* available for download at www.zilog.com.

General Purpose Input/Output

Z8 Encore! XP® F0822 Series features 11 to 19 port pins (Ports A–C) for General Purpose Input/Output (GPIO). The number of GPIO pins available is a function of package. Each pin is individually programmable. Ports A and C supports 5 V-tolerant inputs.

Flash Controller

The Flash Controller programs and erases the Flash memory.

10-Bit Analog-to-Digital Converter

The optional Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from 2 to 5 different analog input sources.

UART

The Universal Asynchronous Receiver/Transmitter (UART) is full-duplex and capable of handling asynchronous data transfers. The UART supports 8-bit and 9-bit data modes and selectable parity.

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
F47	UART0 Baud Rate Low Byte	U0BRL	FF	106
F48-F4F	Reserved	—	XX	
I²C				
F50	I²C Data	I2CDATA	00	139
F51	I²C Status	I2CSTAT	80	140
F52	I²C Control	I2CCTL	00	141
F53	I²C Baud Rate High Byte	I2CBRH	FF	143
F54	I²C Baud Rate Low Byte	I2CBRL	FF	143
F55	I²C Diagnostic State	I2CDST	XX000000b	143
F56	I²C Diagnostic Control	I2CDIAG	00	145
F57-F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI) Unavailable in 20-Pin Package Devices				
F60	SPI Data	SPIDATA	01	121
F61	SPI Control	SPICTL	00	122
F62	SPI Status	SPISTAT	00	123
F63	SPI Mode	SPIMODE	00	124
F64	SPI Diagnostic State	SPIDST	00	125
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	125
F67	SPI Baud Rate Low Byte	SPIBRL	FF	125
F68-F6F	Reserved	—	XX	
Analog-to-Digital Converter (ADC)				
F70	ADC Control	ADCCTL	20	150
F71	Reserved	—	XX	
F72	ADC Data High Byte	ADCD_H	XX	151
F73	ADC Data Low Bits	ADCD_L	XX	151
F74-FBF	Reserved	—	XX	
Interrupt Controller				
FC0	Interrupt Request 0	IRQ0	00	61
FC1	IRQ0 Enable High Bit	IRQ0ENH	00	63
FC2	IRQ0 Enable Low Bit	IRQ0ENL	00	63
FC3	Interrupt Request 1	IRQ1	00	62
FC4	IRQ1 Enable High Bit	IRQ1ENH	00	64
FC5	IRQ1 Enable Low Bit	IRQ1ENL	00	64
FC6	Interrupt Request 2	IRQ2	00	63
FC7	IRQ2 Enable High Bit	IRQ2ENH	00	65
FC8	IRQ2 Enable Low Bit	IRQ2ENL	00	65
FC9-FCC	Reserved	—	XX	
FCD	Interrupt Edge Select	IRQES	00	67

XX=Undefined

I2C Control
I2CCTL (F52H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

I2C Signal Filter Enable
0 = Digital filtering disabled
1 = Low-pass digital filters enabled on SDA and SCL input signals

Flush Data
0 = No effect
1 = Clears I2C Data register

Send NAK
0 = Do not send NAK
1 = Send NAK after next byte received from slave

Enable TDRE Interrupts
0 = Do not generate an interrupt when the I2C Data register is empty
1 = Generate an interrupt when the I2C Transmit Data register is empty

Baud Rate Generator
0 = Interrupts behave as set by I2C control
1 = BRG generates an interrupt when it counts down to zero

Send STOP Condition
0 = Do not issue STOP condition after data transmission is complete
1 = Issue STOP condition after data transmission is complete

Send Start Condition
0 = Do not send Start Condition
1 = Send Start Condition

I2C Enable
0 = I2C is disabled
1 = I2C is enabled

External Pin Reset

The $\overline{\text{RESET}}$ pin contains a Schmitt-triggered input, an internal pull-up, an analog filter, and a digital filter to reject noise. After the $\overline{\text{RESET}}$ pin is asserted for at least 4 system clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, Z8 Encore! XP F0822 Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state immediately following $\overline{\text{RESET}}$ pin deassertion. Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Watchdog Timer Control Register (WDTCTL) is set to 1.

On-Chip Debugger Initiated Reset

A POR is initiated using the OCD by setting the RST bit in the OCD Control Register. The OCD block is not reset but the rest of the chip goes through a normal system reset. The RST bit automatically clears during the system reset. Following the system reset, the POR bit in the WDT Control Register is set.

Stop Mode Recovery

STOP mode is entered by execution of a STOP instruction by the eZ8 CPU. For detailed information on STOP mode, see Low-Power Modes on page 45. During Stop Mode Recovery, the device is held in reset for 66 cycles of the WDT oscillator followed by 16 cycles of the system clock. Stop Mode Recovery only affects the contents of the WDT Control Register and does not affect any other values in the Register File, including the Stack Pointer, Register Pointer, Flags, Peripheral Control Registers, and General-Purpose RAM.

The eZ8 CPU fetches the Reset vector at Program Memory addresses 0002H and 0003H and loads that value into the Program Counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the STOP bit in the WDT Control Register is set to 1. Table 10 lists the Stop Mode Recovery sources and resulting actions. The text following provides more detailed information on each of the Stop Mode Recovery sources.

Table 10. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
STOP mode	WDT time-out when configured for Reset	Stop Mode Recovery
	WDT time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery

4. If required, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
7. Write to the Timer Control Register to enable the timer.

In COUNTER mode, the number of Timer Input transitions since the timer start is given by the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value – Start Value

PWM Mode

In PWM mode, the timer outputs a Pulse-Width Modulator output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte Registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the Reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the Reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte Registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and then transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the Reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and then transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the Reload value and is reset to 0001H.

Follow the steps below for configuring a timer for PWM mode and initiating the PWM operation:

1. Write to the Timer Control Register to:
   – Disable the timer
   – Configure the timer for PWM mode.
   – Set the prescale value.
   – Set the initial logic level (High or Low) and PWM High/Low transition for the Timer Output alternate function.
2. Write to the Timer High and Low Byte Registers to set the starting count value (typically 0001H). This only affects the first pass in PWM mode. After the first timer reset in PWM mode, counting always begins at the reset value of 0001H.

0, then reading the UART Receive Data Register clears this bit.
0 = No overrun error occurred.
1 = An overrun error occurred.

FE—Framing Error
This bit indicates that a framing error (no STOP bit following data reception) was detected. Reading the UART Receive Data Register clears this bit.
0 = No framing error occurred.
1 = A framing error occurred.

BRKD—Break Detect
This bit indicates that a break occurred. If the data bits, parity/multiprocessor bit, and STOP bit(s) are all zeros then this bit is set to 1. Reading the UART Receive Data Register clears this bit.
0 = No break occurred.
1 = A break occurred.

TDRE—Transmitter Data Register Empty
This bit indicates that the UART Transmit Data Register is empty and ready for additional data. Writing to the UART Transmit Data Register resets this bit.
0 = Do not write to the UART Transmit Data Register.
1 = The UART Transmit Data Register is ready to receive an additional byte to be transmitted.

TXE—Transmitter Empty
This bit indicates that the transmit shift register is empty and character transmission is finished.
0 = Data is currently transmitting.
1 = Transmission is complete.

CTS—$\overline{\text{CTS}}$ Signal
When this bit is read it returns the level of the $\overline{\text{CTS}}$ signal.

UART Status 1 Register

This register contains multiprocessor control and status bits.

Table 55. UART Status 1 Register (U0STAT1)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved						NEWFRM	MPRX
RESET	0							
R/W	R				R/W		R	
ADDR	F44H							

Table 58. UART Address Compare Register (U0ADDR)

BITS	7	6	5	4	3	2	1	0
FIELD	COMP_ADDR							
RESET	0							
R/W	R/W							
ADDR	F45H							

COMP_ADDR—Compare Address
This 8-bit value is compared to the incoming address bytes.

UART Baud Rate High and Low Byte Registers

The UART Baud Rate High and Low Byte registers (Table 59 and Table 60) combine to create a 16-bit baud rate divisor value (BRG[15:0]) that sets the data transmission rate (baud rate) of the UART.

Table 59. UART Baud Rate High Byte Register (U0BRH)

BITS	7	6	5	4	3	2	1	0
FIELD	BRH							
RESET	1							
R/W	R/W							
ADDR	F46H							

Table 60. UART Baud Rate Low Byte Register (U0BRL)

BITS	7	6	5	4	3	2	1	0
FIELD	BRL							
RESET	1							
R/W	R/W							
ADDR	F47H							

The UART data rate is calculated using the following equation:

$$\text{UART Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a synchronous interface allowing several SPI-type devices to be interconnected. SPI-compatible devices include EEPROMs, Analog-to-Digital Converters, and ISDN devices. Features of the SPI include:

- Full-duplex, synchronous, and character-oriented communication
- Four-wire interface
- Data transfers rates up to a maximum of one-half the system clock frequency
- Error detection
- Dedicated Baud Rate Generator

The SPI is not available in 20-pin package devices.

Architecture

The SPI is be configured as either a Master (in single or multi-master systems) or a Slave as displayed in Figure 20 through Figure 22.

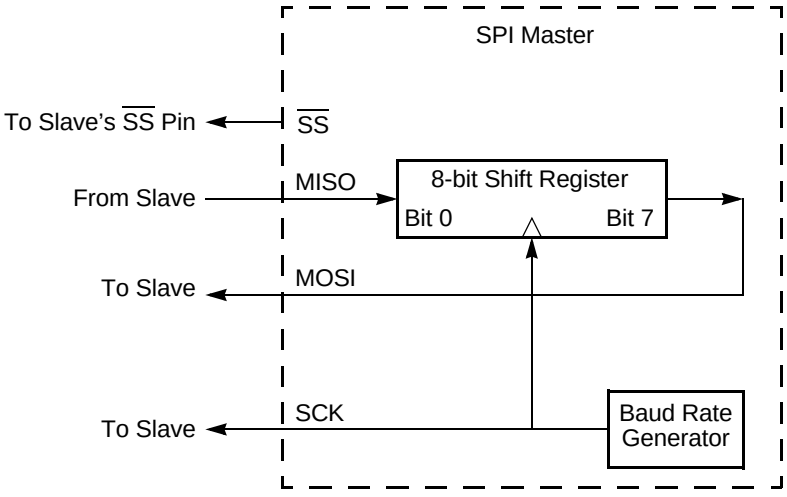


Figure 20. SPI Configured as a Master in a Single Master, Single Slave System

9. Software responds by writing the second byte of address into the contents of the I²C Data Register.
10. The I²C Controller shifts the rest of the first byte of address and write bit out the SDA signal.
11. If the I²C Slave sends an acknowledge by pulling the SDA signal low during the next high period of SCL the I²C Controller sets the ACK bit in the I²C Status register. Continue with step 12.

    If the slave does not acknowledge the first address byte, the I²C Controller sets the NCKI bit and clears the ACK bit in the I²C Status register. Software response to the Not Acknowledge interrupt by setting the STOP and FLUSH bits and clearing the TXI bit. The I2C Controller sends the STOP condition on the bus and clears the STOP and NCKI bits. The transaction is complete (ignore following steps).
12. The I²C Controller loads the I²C Shift register with the contents of the I²C Data Register (2nd byte of address).
13. The I²C Controller shifts the second address byte out the SDA signal. After the first bit has been sent, the Transmit Interrupt is asserted.
14. Software responds by setting the STOP bit in the I²C Control Register. The TXI bit can be cleared at the same time.
15. Software polls the STOP bit of the I²C Control Register. Hardware deasserts the STOP bit when the transaction is completed (STOP condition has been sent).
16. Software checks the ACK bit of the I²C Status register. If the slave acknowledged, the ACK bit is equal to 1. If the slave does not acknowledge, the ACK bit is equal to 0. The NCKI interrupt do not occur because the STOP bit was set.

Write Transaction with a 10-Bit Address

Figure 29 displays the data transfer format for a 10-bit addressed slave. Shaded regions indicate data transferred from the I²C Controller to slaves and unshaded regions indicate data transferred from the slaves to the I²C Controller.

S	Slave Address 1st 7 bits	W = 0	A	Slave Address 2nd Byte	A	Data	A	Data	$\overline{A}$/A	P/S

Figure 29. 10-Bit Addressed Slave Data Transfer Format

The first seven bits transmitted in the first byte are 11110XX. The two bits XX are the two most-significant bits of the 10-bit address. The lowest bit of the first byte transferred is the read/write control bit (=0). The transmit operation is carried out in the same manner as 7-bit addressing.

On-Chip Debugger

Z8 Encore! XP® F0822 Series products have an integrated On-Chip Debugger (OCD) that provides advanced debugging features including:

- Reading and writing of the Register File
- Reading and (Flash version only) writing of Program and Data Memory
- Setting of Breakpoints
- Executing eZ8 CPU instructions

Architecture

The OCD consists of four primary functional blocks: transmitter, receiver, autobaud generator, and debug controller. Figure 37 displays the architecture of the OCD.

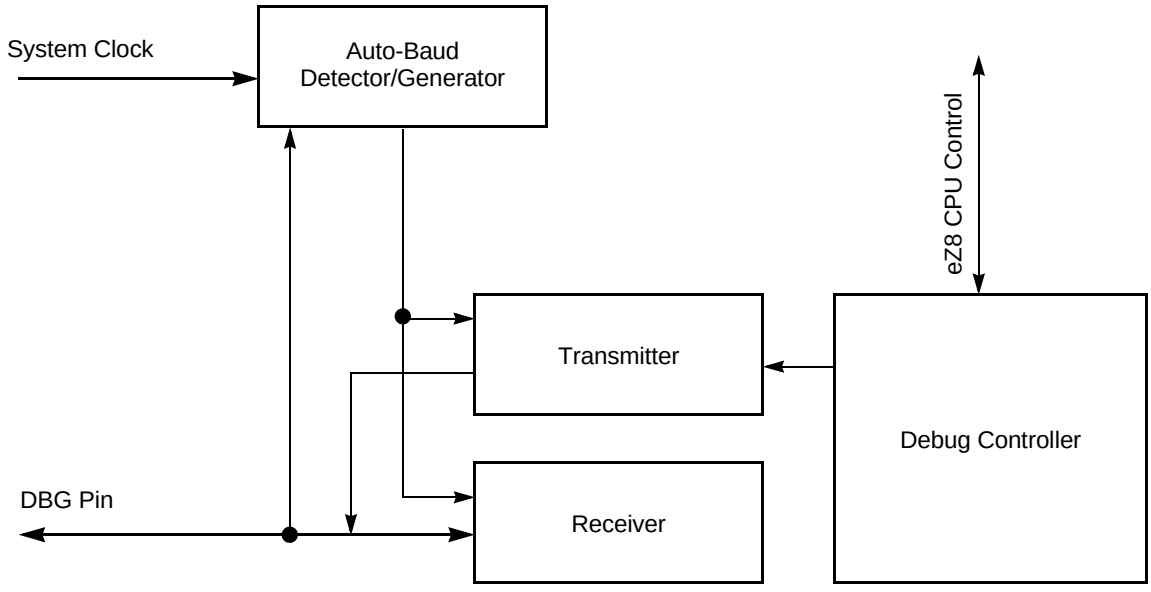


Figure 37. On-Chip Debugger Block Diagram

Operation

OCD Interface

The OCD uses the DBG pin for communication with an external host. This one-pin interface is a bi-directional open-drain interface that transmits and receives data. Data

RPEN—Read Protect Option Bit Enabled
0 = The Read Protect Option Bit is disabled (1).
1 = The Read Protect Option Bit is enabled (0), disabling many OCD commands.

Reserved. Must be 0

Table 97. DC Characteristics (Continued)

Symbol	Parameter	T_A = -40 °C to 105 °C			Units	Conditions
		Minimum	Typical	Maximum		
V_{RAM}	RAM Data Retention	0.7	–	–	V	
I_{IL}	Input Leakage Current	-5	–	+5	µA	V_{DD} = 3.6 V; V_{IN} = VDD or VSS[1]
I_{TL}	Tri-State Leakage Current	-5	–	+5	µA	V_{DD} = 3.6 V
C_{PAD}	GPIO Port Pad Capacitance	–	8.0[2]	–	pF	
C_{XIN}	XIN Pad Capacitance	–	8.0[2]	–	pF	
C_{XOUT}	XOUT Pad Capacitance	–	9.5[2]	–	pF	
I_{PU1}	Weak Pull-up Current	9	20	50	µA	VDD = 2.7–3.6 V. T_A = 0 °C to +70 °C
I_{PU2}	Weak Pull-up Current	7	20	75	µA	VDD = 2.7–3.6 V. T_A = -40 °C to +105 °C

[1] This condition excludes all pins that have on-chip pull-ups, when driven Low.

[2] These values are provided for design guidance only and are not tested in production.

Figure 41 on page 189 displays the typical active mode current consumption while operating at 25 ºC, 3.3 V, versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

General Purpose I/O Port Input Data Sample Timing

Figure 48 displays timing of the GPIO Port input sampling. Table 105 lists the GPIO port input timing.

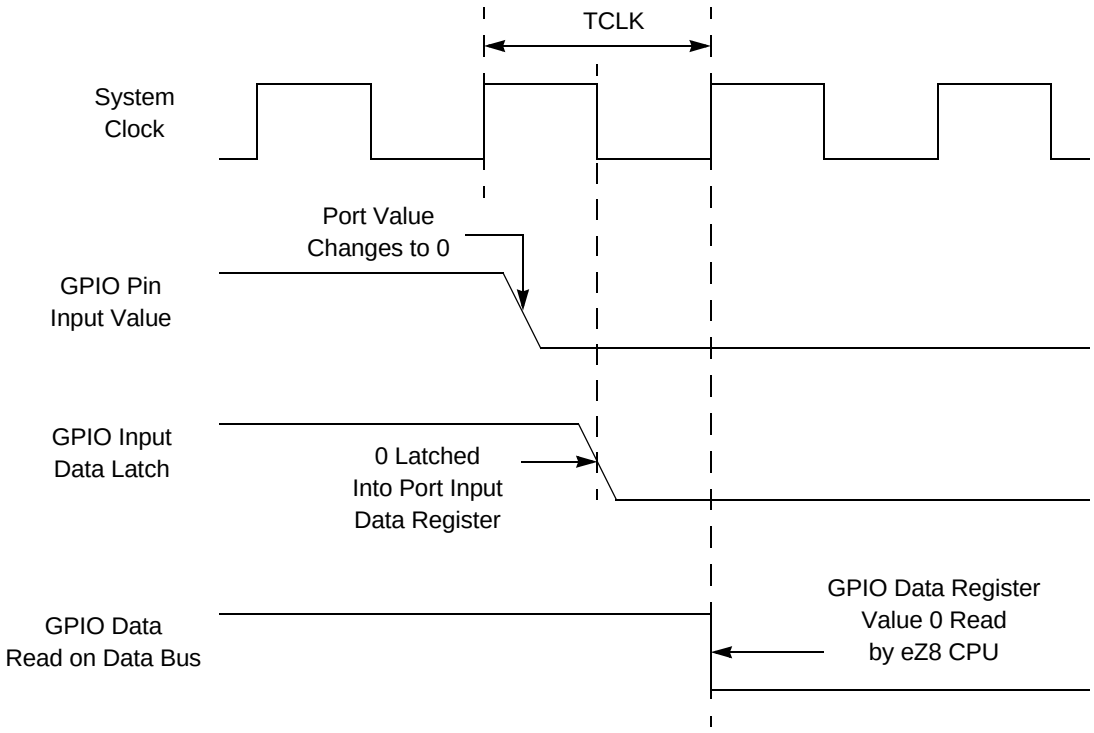


Figure 48. Port Input Sample Timing

Table 105. GPIO Port Input Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
T_{S_PORT}	Port Input Transition to XIN Fall Setup Time (Not pictured)	5	–
T_{H_PORT}	XIN Fall to Port Input Transition Hold Time (Not pictured)	5	–
T_{SMR}	GPIO Port Pin Pulse Width to Insure Stop Mode Recovery (for GPIO Port Pins enabled as SMR sources)	1µs	

Table 123. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 124. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-Chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 126. eZ8 CPU Instruction Summary (Continued)

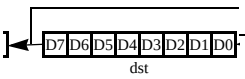
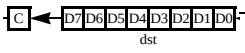
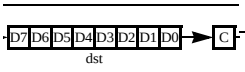
Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	-	-	-	-	-	-	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	-	-	-	-	-	-	2	2
		IR		71							2	3
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	-	-	-	-	-	-	3	2
RCF	C ← 0			CF	0	-	-	-	-	-	1	2
RET	PC ← @SP SP ← SP + 2			AF	-	-	-	-	-	-	1	4
RL dst		R		90	*	*	*	*	-	-	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	-	-	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	-	-	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	-	-	2	2
		IR		C1							2	3
SBC dst, src	dst ← dst – src - C	r	r	32	*	*	*	*	1	*	2	3
		r	Ir	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	dst ← dst – src - C	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3

Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
TM dst, src	dst AND src	r	r	72	-	*	*	0	-	-	2	3
		r	Ir	73							2	4
		R	R	74							3	3
		R	IR	75							3	4
		R	IM	76							3	3
		IR	IM	77							3	4
TMX dst, src	dst AND src	ER	ER	78	-	*	*	0	-	-	4	3
		ER	IM	79							4	3
TRAP Vector	SP ← SP – 2 @SP ← PC SP ← SP – 1 @SP ← FLAGS PC ← @Vector		Vector	F2	-	-	-	-	-	-	2	6
WDT				5F	-	-	-	-	-	-	1	2
XOR dst, src	dst ← dst XOR src	r	r	B2	-	*	*	0	-	-	2	3
		r	Ir	B3							2	4
		R	R	B4							3	3
		R	IR	B5							3	4
		R	IM	B6							3	3
		IR	IM	B7							3	4
XORX dst, src	dst ← dst XOR src	ER	ER	B8	-	*	*	0	-	-	4	3
		ER	IM	B9							4	3

Flags Notation: * = Value is a function of the result of the operation.
- = Unaffected
X = Undefined
0 = Reset to 0
1 = Set to 1

Ordering Information

Order Z8 Encore! XP F0822 Series from Zilog®, using the following part numbers. For more information regarding ordering, consult your local Zilog sales office. Zilog website at www.zilog.com lists all regional offices and provides additional Z8 Encore! XP product information.

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F08xx with 8 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0821HH020SC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020SC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package
Extended Temperature: -40° to +105°C										
Z8F0821HH020EC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020EC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F04xx with 4 KB Flash										
Standard Temperature: 0 °C to 70 °C										
Z8F0411HH020SC	4 KB	1 KB	11	16	2	0	1	0	1	SSOP 20-pin package
Z8F0411PH020SC	4 KB	1 KB	11	16	2	0	1	0	1	PDIP 20-pin package
Z8F0412SJ020SC	4 KB	1 KB	19	19	2	0	1	1	1	SOIC 28-pin package
Z8F0412PJ020SC	4 KB	1 KB	19	19	2	0	1	1	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C										
Z8F0411HH020EC	4 KB	1 KB	11	16	2	0	1	0	1	SSOP 20-pin package
Z8F0411PH020EC	4 KB	1 KB	11	16	2	0	1	0	1	PDIP 20-pin package
Z8F0412SJ020EC	4 KB	1 KB	19	19	2	0	1	1	1	SOIC 28-pin package
Z8F0412PJ020EC	4 KB	1 KB	19	19	2	0	1	1	1	PDIP 28-pin package
Z8F08200100KITG										Development Kit (20- and 28-pin)
ZUSBSC00100ZACG										USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG										Opto-Isolated USB Smart Cable Accessory Kit

Note: Replace C with G for lead-free packaging.

bit manipulation 215
block transfer 215
BRK 217
BSET 215
BSWAP 215, 218
BTJ 217
BTJNZ 217
BTJZ 217
CALL 217
CCF 215, 216
CLR 216
COM 217
CP 214
CPC 214
CPCX 214
CPU control 216
CPX 214
DA 214
DEC 214
DECW 214
DI 216
DJNZ 217
EI 216
HALT 216
INC 214
INCW 214
IRET 217
JP 217
LD 216
LDC 216
LDCI 215, 216
LDE 216
LDEI 215
LDX 216
LEA 216
load 216
logical 217
MULT 214
NOP 216
OR 217
ORX 217
POP 216
POPX 216
program control 217
PUSH 216
PUSHX 216
RCF 215, 216
RET 217
RL 218
RLC 218
rotate and shift 218
RR 218
RRC 218
SBC 215
SCF 215, 216
SRA 218
SRL 218
SRP 216
STOP 216
SUB 215
SUBX 215
SWAP 218
TCM 215
TCMX 215
TM 215
TMX 215
TRAP 217
watch-dog timer refresh 216
XOR 217
XORX 217
instructions, eZ8 classes of 214
interrupt control register 67
interrupt controller 5, 57
architecture 57
interrupt assertion types 60
interrupt vectors and priority 60
operation 59
register definitions 61
software interrupt assertion 60
interrupt edge select register 67
interrupt request 0 register 61
interrupt request 1 register 62
interrupt request 2 register 63
interrupt return 217
interrupt vector listing 57
interrupts
not acknowledge 128
receive 128