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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0811hh020sc00tr

- 2.7 V to 3.6 V operating voltage with 5 V-tolerant inputs
- 20-pin and 28-pin packages
- 0 °C to +70 °C standard temperature and -40 °C to +105 °C extended temperature operating ranges

Part Selection Guide

Table 1 identifies the basic features and package styles available for each device within the Z8 Encore! XP® F0822 Series product line.

Table 1. Z8 Encore! XP® F0822 Series Part Selection Guide

Part Number	Flash (KB)	RAM (KB)	I/O	16-bit Timers with PWM	ADC Inputs	UARTs with IrDA	I^2C	SPI	Package Pin Counts	
									20	28
Z8F0822	8	1	19	2	5	1	1	1		X
Z8F0821	8	1	11	2	2	1	1		X	
Z8F0812	8	1	19	2	0	1	1	1		X
Z8F0811	8	1	11	2	0	1	1		X	
Z8F0422	4	1	19	2	5	1	1	1		X
Z8F0421	4	1	11	2	2	1	1		X	
Z8F0412	4	1	19	2	0	1	1	1		X
Z8F0411	4	1	11	2	0	1	1		X	

Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FCE	Reserved	—	00	
FCF	Interrupt Control	IRQCTL	00	67
GPIO Port A				
FD0	Port A Address	PAADDR	00	50
FD1	Port A Control	PACTL	00	51
FD2	Port A Input Data	PAIN	XX	54
FD3	Port A Output Data	PAOUT	00	55
GPIO Port B				
FD4	Port B Address	PBADDR	00	50
FD5	Port B Control	PBCTL	00	51
FD6	Port B Input Data	PBIN	XX	54
FD7	Port B Output Data	PBOUT	00	55
GPIO Port C				
FD8	Port C Address	PCADDR	00	50
FD9	Port C Control	PCCTL	00	51
FDA	Port C Input Data	PCIN	XX	54
FDB	Port C Output Data	PCOUT	00	55
FDC-FEF	Reserved	—	XX	
Watchdog Timer (WDT)				
FF0	Watchdog Timer Control	WDTCTL	XXX00000b	86
FF1	Watchdog Timer Reload Upper Byte	WDTU	FF	87
FF2	Watchdog Timer Reload High Byte	WDTH	FF	87
FF3	Watchdog Timer Reload Low Byte	WDTL	FF	87
FF4-FF7	Reserved	—	XX	
Flash Memory Controller				
FF8	Flash Control	FCTL	00	159
FF8	Flash Status	FSTAT	00	160
FF9	Page Select	FPS	00	160
FF9 (if enabled)	Flash Sector Protect	FPROT	00	161
FFA	Flash Programming Frequency High Byte	FFREQH	00	161
FFB	Flash Programming Frequency Low Byte	FFREQL	00	161
Read-Only Memory				
FF8	Reserved	—	XX	
FF9	Page Select	RPS	00	160
FFA-FFB	Reserved	—	XX	
eZ8 CPU				
XX=Undefined				

UART0 Control 1
U0CTL1 (F43H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

- D0: Infrared Encoder/Decoder
  0 = Infrared endec is disabled
  1 = Infrared endec is enabled
- D1: Received Data Interrupt
  0 = Received data and errors generate interrupt requests
  1 = Only errors generate interrupt requests. Received data does not.
- D2: Baud Rate Registers Control
  See UART chapter for operation
- D3: Driver Enable Polarity
  0 = DE signal is active High
  1 = DE signal is active Low
- D4: Multiprocessor Bit Transmit
  0 = Send a 0 as the multiprocessor bit
  1 = Send a 1 as the multiprocessor bit
- D5: Multiprocessor Mode [0]
  See Multiprocessor Mode [1] below
- D6: Multiprocessor (9-bit) Enable
  0 = Multiprocessor mode is disabled
  1 = Multiprocessor mode is enabled
- D7: Multiprocessor Mode [1]
  with Multiprocess Mode bit 0:
  00 = Interrupt on all received bytes
  01 = Interrupt only on address bytes
  10 = Interrupt on address match and following data
  11 = Interrupt on data following an address match

ADC Control
ADCCTL (F70H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0

D3–D0: Analog Input Select
- 0000 = ANA0
- 0001 = ANA1
- 0010 = ANA2
- 0011 = ANA3
- 0100 = ANA4
- 0101 through 21111 = Reserved

D4: Continuous Mode Select
- 0 = Single-shot conversion
- 1 = Continuous conversion

D5: External VREF select
- 0 = Internal voltage reference selected
- 1 = External voltage reference selected

D6: Reserved

D7: Conversion Enable
- 0 = Conversion is complete
- 1 = Begin conversion

ADC Data High Byte
ADCD_H (F72H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

D7–D0: ADC Data [9:2]

ADC Data Low Bits
ADCD_L (F73H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0

D5–D0: Reserved

D7–D6: ADC Data [1:0]

Reset and Stop Mode Recovery

The Reset Controller within the Z8 Encore! XP® F0822 Series controls Reset and Stop Mode Recovery operation. In typical operation, the following events cause a Reset to occur:

- Power-On Reset (POR)
- Voltage Brownout
- WDT time-out (when configured through the WDT_RES Option Bit to initiate a Reset)
- External $\overline{\text{RESET}}$ pin assertion
- On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)

When the Z8 Encore! XP F0822 Series device is in STOP mode, a Stop Mode Recovery is initiated by any of the following events:

- WDT time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source
- DBG pin driven Low

Reset Types

Z8 Encore! XP F0822 Series provides two types of reset operation (System Reset and Stop Mode Recovery). The type of reset is a function of both the current operating mode of the Z8 Encore! XP F0822 Series device and the source of the Reset. Table 8 lists the types of Resets and their operating characteristics.

Table 8. Reset and Stop Mode Recovery Characteristics and Latency

	Reset Characteristics and Latency		
Reset Type	**Control Registers**	**eZ8 CPU**	**Reset Latency (Delay)**
System Reset	Reset (as applicable)	Reset	66 WDT Oscillator cycles + 16 System Clock cycles
Stop Mode Recovery	Unaffected, except WDT_CTL register	Reset	66 WDT Oscillator cycles + 16 System Clock cycles

Power-On Reset

Each device in the Z8 Encore! XP® F0822 Series contains an internal POR circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the POR Counter is enabled and counts 66 cycles of the WDT oscillator. After the POR counter times out, the XTAL Counter is enabled to count a total of 16 system clock pulses. The device is held in the Reset state until both the POR Counter and XTAL counter have timed out. After the Z8 Encore! XP F0822 Series device exits the POR state, the eZ8 CPU fetches the Reset vector. Following POR, the `POR` status bit in the Watchdog Timer Control Register (WDTCTL) is set to 1.

Figure 6 displays POR operation. See Electrical Characteristics for POR threshold voltage (V_{POR}).

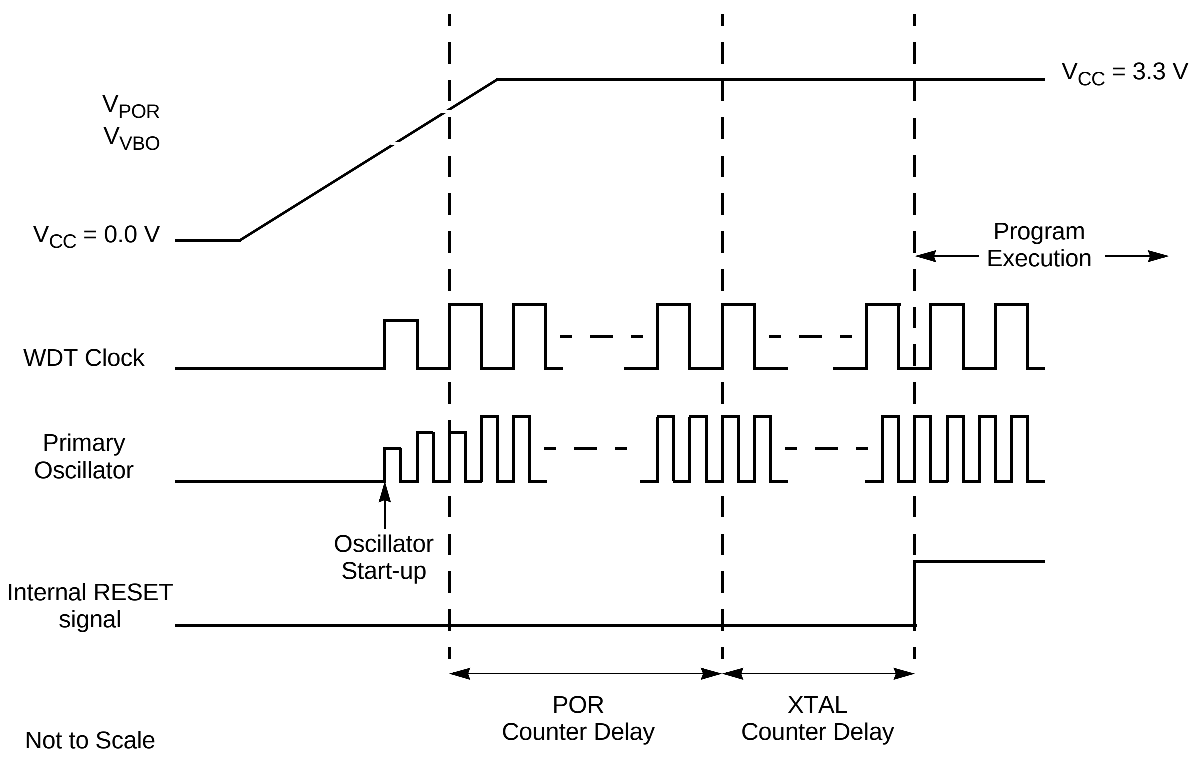

Figure 6. Power-On Reset Operation

Voltage Brownout Reset

The devices in Z8 Encore! XP F0822 Series provide low Voltage Brownout protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage

Table 43. Timer 0–1 PWM High Byte Register (TxPWMH)

BITS	7	6	5	4	3	2	1	0
FIELD	PWMH							
RESET	0							
R/W	R/W							
ADDR	F04H, F0CH							

Table 44. Timer 0–1 PWM Low Byte Register (TxPWML)

BITS	7	6	5	4	3	2	1	0
FIELD	PWML							
RESET	0							
R/W	R/W							
ADDR	F05H, F0DH							

PWMH and PWML—Pulse-Width Modulator High and Low Bytes
These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the `TPOL` bit in the Timer Control Register (TxCTL) register.

The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

Timer 0–3 Control 0 Registers

The Timer 0–3 Control 0 (TxCTL0) registers (Table 45) allow cascading of the Timers.

Table 45. Timer 0–3 Control 0 Register (TxCTL0)

BITS	7	6	5	4	3	2	1	0
FIELD	Reserved			CSC	Reserved			
RESET	0							
R/W	R/W							
ADDR	F06H, F0EH, F16H, F1EH							

CSC—Cascade Timers
0 = Timer Input signal comes from the pin.
1 = For Timer 0, input signal is connected to Timer 1 output.
For Timer 1, input signal is connected to Timer 0 output.

PSEL—Parity Select
0 = Even parity is transmitted and expected on all received data.
1 = Odd parity is transmitted and expected on all received data.

SBRK—Send Break
This bit pauses or breaks data transmission by forcing the Transmit data output to 0. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. The UART does not automatically generate a STOP Bit when SBRK is deasserted. Software must time the duration of the Break and the duration of any STOP Bit time desired following the Break.
0 = No break is sent.
1 = The output of the transmitter is zero.

STOP—STOP Bit Select
0 = The transmitter sends one stop bit.
1 = The transmitter sends two stop bits.

LBEN—Loop Back Enable
0 = Normal operation.
1 = All transmitted data is looped back to the receiver.

Table 57. UART Control 1 Register (U0CTL1)

BITS	7	6	5	4	3	2	1	0
FIELD	MPMD[1]	MPEN	MPMD[0]	MPBT	DEPOL	BRGCTL	RDAIRQ	IREN
RESET	0							
R/W	R/W							
ADDR	F43H							

MPMD[1:0]—Multiprocessor Mode
If Multiprocessor (9-bit) mode is enabled,
00 = The UART generates an interrupt request on all received bytes (data and address).
01 = The UART generates an interrupt request only on received address bytes.
10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs.
11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register.

MPEN—Multiprocessor (9-bit) Enable
This bit is used to enable Multiprocessor (9-bit) mode.
0 = Disable Multiprocessor (9-bit) mode.
1 = Enable Multiprocessor (9-bit) mode.

The Master and Slave are each capable of exchanging a character of data during a sequence of NUMBITS clock cycles (see NUMBITS field in the SPIMODE Register). In both Master and Slave SPI devices, data is shifted on one edge of the SCK and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI phase and polarity control.

Slave Select

The active Low Slave Select ($\overline{SS}$) input signal selects a Slave SPI device. $\overline{SS}$ must be Low prior to all data communication to and from the Slave device. $\overline{SS}$ must stay Low for the full duration of each character transferred. The $\overline{SS}$ signal can stay Low during the transfer of multiple characters or can deassert between each character.

When the SPI is configured as the only Master in an SPI system, the $\overline{SS}$ pin is set as either an input or an output. For communication between the Z8 Encore! XP F0822 Series device's SPI Master and external Slave devices, the $\overline{SS}$ signal, as an output, asserts the $\overline{SS}$ input pin on one of the Slave devices. Other GPIO output pins can also be employed to select external SPI Slave devices.

When the SPI is configured as one Master in a multi-master SPI system, the $\overline{SS}$ pin should be set as an input. The $\overline{SS}$ input signal on the Master must be High. If the $\overline{SS}$ signal goes Low (indicating another Master is driving the SPI bus), a Collision error flag is set in the SPI Status Register.

SPI Clock Phase and Polarity Control

The SPI supports four combinations of serial clock phase and polarity using two bits in the SPI Control Register. The clock polarity bit, `CLKPOL`, selects an active high or active low clock and has no effect on the transfer format. Table 62 lists the SPI Clock Phase and Polarity Operation parameters. The clock phase bit, `PHASE`, selects one of two fundamentally different transfer formats. For proper data transmission, the clock phase and polarity must be identical for the SPI Master and the SPI Slave. The Master always places data on the MOSI line a half-cycle before the receive clock edge (SCK signal), in order for the Slave to latch the data.

Table 62. SPI Clock Phase (PHASE) and Clock Polarity (CLKPOL) Operation

PHASE	CLKPOL	SCK Transmit Edge	SCK Receive Edge	SCK Idle State
0	0	Falling	Rising	Low
0	1	Rising	Falling	High
1	0	Rising	Falling	Low
1	1	Falling	Rising	High

RD—Read
This bit indicates the direction of transfer of the data. It is active High during a read. The status of this bit is determined by the least-significant bit of the I^2C Shift register after the START bit is set.

TAS—Transmit Address State
This bit is active High while the address is being shifted out of the I^2C Shift Register.

DSS—Data Shift State
This bit is active High while data is being shifted to or from the I^2C Shift Register.

NCKI—NACK Interrupt
This bit is set high when a Not Acknowledge condition is received or sent and neither the START nor the STOP bit is active. When set, this bit generates an interrupt that can only be cleared by setting the START or STOP bit, allowing you to specify whether you want to perform a STOP or a repeated START.

I^2C Control Register

The I^2C Control Register (Table 72) enables the I^2C operation.

Table 72. I^2C Control Register (I2CCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	IEN	START	STOP	BIRQ	TXI	NAK	FLUSH	FILTEN
RESET	0							
R/W	R/W	R/W1	R/W1	R/W	R/W	R/W1	W1	R/W
ADDR	F52H							

IEN—I^2C Enable
1 = The I^2C transmitter and receiver are enabled.
0 = The I^2C transmitter and receiver are disabled.

START—Send Start Condition
This bit sends the Start condition. Once asserted, it is cleared by the I^2C Controller after it sends the START condition or if the IEN bit is deasserted. If this bit is 1, it cannot be cleared to 0 by writing to the register. After this bit is set, the Start condition is sent if there is data in the I^2C Data or I^2C Shift register. If there is no data in one of these registers, the I^2C Controller waits until the data register is written. If this bit is set while the I^2C Controller is shifting out data, it generates a START condition after the byte shifts and the acknowledge phase completes. If the STOP bit is also set, it also waits until the STOP condition is sent before sending the START condition.

STOP—Send Stop Condition
This bit causes the I^2C Controller to issue a STOP condition after the byte in the I^2C Shift register has completed transmission or after a byte is received in a receive operation. Once

5. Re-write the page written in step 2 to the Page Select Register.
6. Write Flash Memory using LDC or LDCI instructions to program the Flash.
7. Repeat step 6 to program additional memory locations on the same page.
8. Write `00H` to the Flash Control Register to lock the Flash Controller.

Page Erase

Flash memory can be erased one page (512 bytes) at a time. Page Erasing the Flash memory sets all bytes in that page to the value `FFH`. The Page Select Register identifies the page to be erased. While the Flash Controller executes the Page Erase operation, the eZ8 CPU idles but the system clock and on-chip peripherals continue to operate. The eZ8 CPU resumes operation after the Page Erase operation completes. Interrupts that occur when the Page Erase operation is in progress are serviced once the Page Erase operation is complete. When the Page Erase operation is complete, the Flash Controller returns to its locked state. Only pages located in unprotected sectors can be erased.

Follow the steps below to perform a Page Erase operation:

1. Write `00H` to the Flash Control Register to reset the Flash Controller.
2. Write the page to be erased to the Page Select Register.
3. Write the first unlock command `73H` to the Flash Control Register.
4. Write the second unlock command `8CH` to the Flash Control Register.
5. Re-write the page written in step 2 to the Page Select Register.
6. Write the Page Erase command `95H` to the Flash Control Register.

Mass Erase

The Flash memory cannot be Mass Erased by user code.

Flash Controller Bypass

The Flash Controller can be bypassed and the control signals for the Flash memory brought out to the GPIO pins. Bypassing the Flash Controller allows faster Programming algorithms by controlling the Flash programming signals directly.

Flash Controller Bypass is recommended for gang programming applications and large volume customers who do not require in-circuit programming of the Flash memory.

For more information on bypassing the Flash Controller, refer to *Third-Party Flash Programming Support for Z8 Encore! XP*, available for download at www.zilog.com.

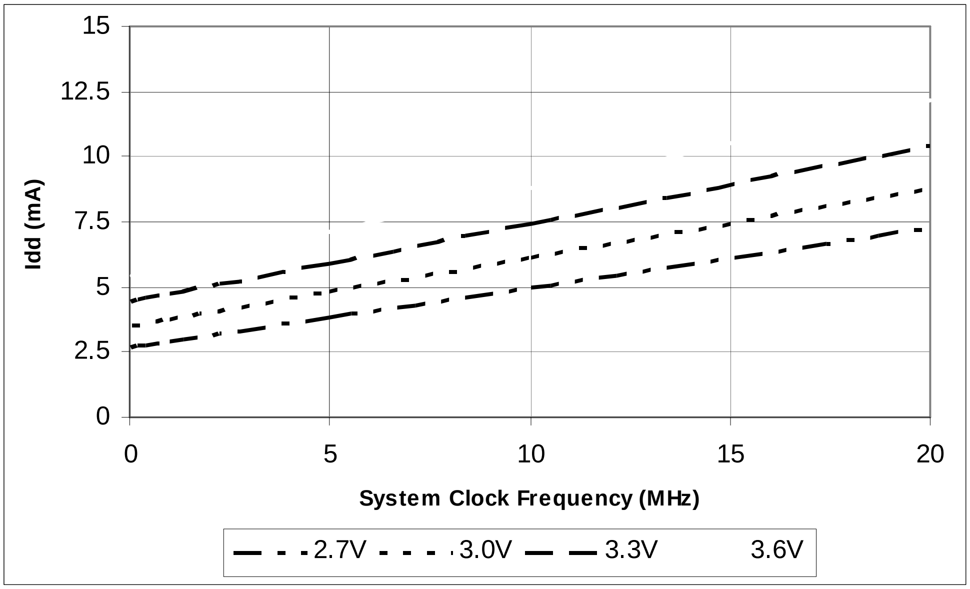

Figure 41. Typical Active Mode I_{DD} Versus System Clock Frequency

Figure 42 displays the maximum active mode current consumption across the full operating temperature range of the device and versus the system clock frequency. All GPIO pins are configured as outputs and driven High.

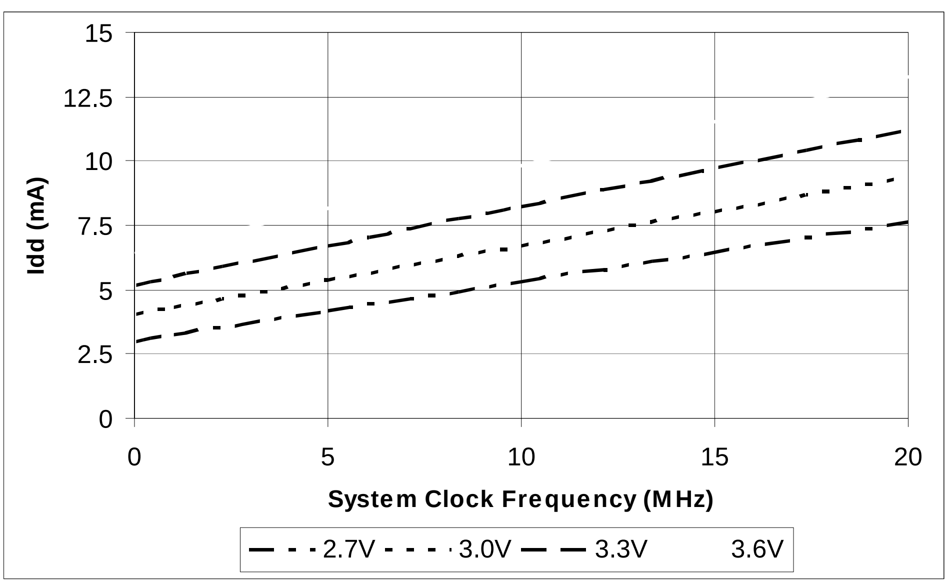

Figure 42. Maximum Active Mode I_{DD} Versus System Clock Frequency

SPI MASTER Mode Timing

Figure 51 and Table 108 provide timing information for SPI MASTER mode pins. Timing is shown with SCK rising edge used to source MOSI output data, SCK falling edge used to sample MISO input data. Timing on the SS output pin(s) is controlled by software.

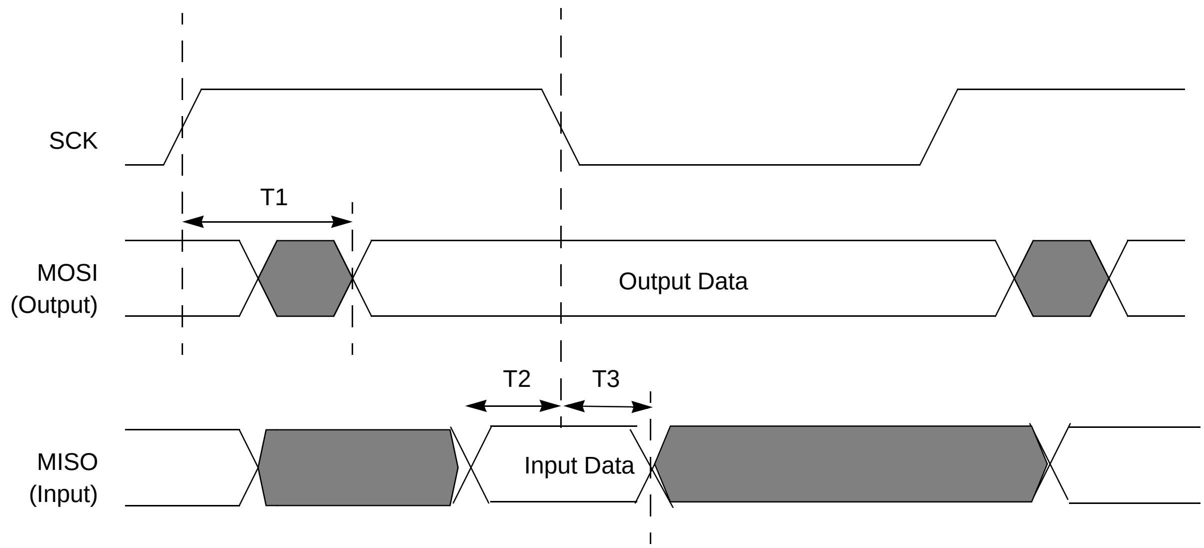

Figure 51. SPI MASTER Mode Timing

Table 108. SPI MASTER Mode Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
SPI MASTER			
T_1	SCK Rise to MOSI output Valid Delay	-5	+5
T_2	MISO input to SCK (receive edge) Setup Time	20	
T_3	MISO input to SCK (receive edge) Hold Time	0	

Table 126. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Opcode(s) (Hex)	Flags C	Flags Z	Flags S	Flags V	Flags D	Flags H	Fetch Cycles	Instr. Cycles
LD dst, rc	dst ← src	r	IM	0C-FC	-	-	-	-	-	-	2	2
		r	X(r)	C7							3	3
		X(r)	r	D7							3	4
		r	Ir	E3							2	3
		R	R	E4							3	2
		R	IR	E5							3	4
		R	IM	E6							3	2
		IR	IM	E7							3	3
		Ir	r	F3							2	3
		IR	R	F5							3	3
LDC dst, src	dst ← src	r	Irr	C2	-	-	-	-	-	-	2	5
		Ir	Irr	C5							2	9
		Irr	r	D2							2	5
LDCI dst, src	dst ← src r ← r + 1 rr ← rr + 1	Ir	Irr	C3	-	-	-	-	-	-	2	9
		Irr	Ir	D3							2	9
LDE dst, src	dst ← src	r	Irr	82	-	-	-	-	-	-	2	5
		Irr	r	92							2	5
LDEI dst, src	dst ← src r ← r + 1 rr ← rr + 1	Ir	Irr	83	-	-	-	-	-	-	2	9
		Irr	Ir	93							2	9

Ordering Information

Order Z8 Encore! XP F0822 Series from Zilog®, using the following part numbers. For more information regarding ordering, consult your local Zilog sales office. Zilog website at www.zilog.com lists all regional offices and provides additional Z8 Encore! XP product information.

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F08xx with 8 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0821HH020SC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020SC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020SC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package
Extended Temperature: -40° to +105°C										
Z8F0821HH020EC	8 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0821PH020EC	8 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0822SJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0822PJ020EC	8 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package

Part Number	Flash	RAM	I/O Lines	Interrupts	16-Bit Timers w/PWM	10-Bit A/D Channels	I^2C	SPI	UARTs with IrDA	Description
Z8F04xx with 4 KB Flash, 10-Bit Analog-to-Digital Converter										
Standard Temperature: 0 °C to 70 °C										
Z8F0421HH020SC	4 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0421PH020SC	4 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0422SJ020SC	4 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0422PJ020SC	4 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package
Extended Temperature: -40 °C to 105 °C										
Z8F0421HH020EC	4 KB	1 KB	11	16	2	2	1	0	1	SSOP 20-pin package
Z8F0421PH020EC	4 KB	1 KB	11	16	2	2	1	0	1	PDIP 20-pin package
Z8F0422SJ020EC	4 KB	1 KB	19	19	2	5	1	1	1	SOIC 28-pin package
Z8F0422PJ020EC	4 KB	1 KB	19	19	2	5	1	1	1	PDIP 28-pin package