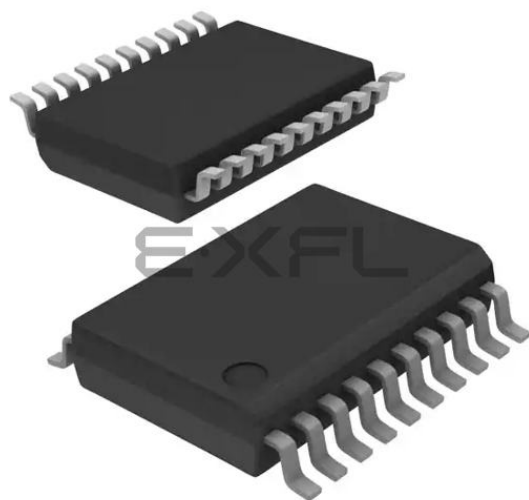




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0821hh020ec00tr

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Port A Address

PAADDR (FD0H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Address[7:0]
Selects Port Sub-Registers:
00H = No function
01H = Data direction
02H = Alternate function
03H = Output control (open-drain)
04H = High drive enable
05H = STOP mode recovery enable
06H = Pull-up enable
07H-FFH = No function

Port A Control

PACTL (FD1H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Control[7:0]
Provides Access to Port Sub-Registers

Port A Input Data

PAIN (FD2H - Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Input Data [7:0]

Port A Output Data

PAOUT (FD3H - Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

Port A Output Data [7:0]

- WDT's internal RC oscillator continues to operate.
- If enabled, the WDT continues to operate.
- All other on-chip peripherals continue to operate.

The eZ8 CPU can be brought out of HALT mode by any of the following operations:

- Interrupt
- WDT time-out (interrupt or reset)
- Power-On Reset
- Voltage Brownout reset
- External $\overline{\text{RESET}}$ pin assertion

To minimize current in HALT mode, all GPIO pins which are configured as inputs must be driven to one of the supply rails (V_{CC} or GND).

1 = The port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP mode initiates Stop Mode Recovery.

Port A–C Pull-up Enable Sub-Registers

The Port A–C Pull-Up Enable sub-register (Table 21) is accessed through the Port A–C Control Register by writing 06H to the Port A–C Address Register. Setting the bits in the Port A–C Pull-Up Enable sub-registers enables a weak internal resistive pull-up on the specified Port pins.

Table 21. Port A–C Pull-Up Enable Sub-Registers

BITS	7	6	5	4	3	2	1	0
FIELD	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
RESET	0							
R/W	R/W							
ADDR	If 06H in Port A–C Address Register, accessible through the Port A–C Control Register							

PPUE[7:0]—Port Pull-up Enabled

0 = The weak pull-up on the Port pin is disabled.
 1 = The weak pull-up on the Port pin is enabled.

Port A–C Input Data Registers

Reading from the Port A–C Input Data Registers (Table 22) returns the sampled values from the corresponding port pins. The Port A–C Input Data Registers are Read-only.

Table 22. Port A–C Input Data Registers (PxIN)

BITS	7	6	5	4	3	2	1	0
FIELD	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X							
R/W	R							
ADDR	FD2H, FD6H, FDAH							

PIN[7:0]—Port Input Data

Sampled data from the corresponding port pin input.
 0 = Input data is logical 0 (Low).
 1 = Input data is logical 1 (High).

Timer 0–1 Control 1 Registers

The Timer 0–1 Control (TxCTL) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

Table 46. Timer 0–1 Control Register (TxCTL)

BITS	7	6	5	4	3	2	1	0
FIELD	TEN	TPOL	PRES			TMODE		
RESET	0							
R/W	R/W							
ADDR	F07H, F0FH							

TEN—Timer Enable

0 = Timer is disabled.

1 = Timer enabled to count.

TPOL—Timer Input/Output Polarity

Operation of this bit is a function of the current operating mode of the timer.

ONE-SHOT Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit.

When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

CONTINUOUS Mode

When the timer is disabled, the Timer Output signal is set to the value of this bit. When the timer is enabled, the Timer Output signal is complemented upon timer Reload.

COUNTER Mode

If the timer is enabled the Timer Output signal is complemented after timer reload.

0 = Count occurs on the rising edge of the Timer Input signal.

1 = Count occurs on the falling edge of the Timer Input signal.

PWM Mode

0 = Timer Output is forced Low (0) when the timer is disabled. When enabled, the Timer Output is forced High (1) upon PWM count match and forced Low (0) upon Reload.

1 = Timer Output is forced High (1) when the timer is disabled. When enabled, the Timer Output is forced Low (0) upon PWM count match and forced High (1) upon Reload.

CAPTURE Mode

0 = Count is captured on the rising edge of the Timer Input signal.

1 = Count is captured on the falling edge of the Timer Input signal.

Table 50. Watchdog Timer Reload High Byte Register (WDTH)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTH							
RESET	1							
R/W	R/W*							
ADDR	FF2H							
R/W*—Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTH—WDT Reload High Byte

Middle byte, Bits[15:8], of the 24-bit WDT reload value.

Table 51. Watchdog Timer Reload Low Byte Register (WDTL)

BITS	7	6	5	4	3	2	1	0
FIELD	WDTL							
RESET	1							
R/W	R/W*							
ADDR	FF3H							
R/W*—Read returns the current WDT count value. Write sets the desired Reload Value.								

WDTL—WDT Reload Low

Least significant byte (LSB), Bits[7:0], of the 24-bit WDT reload value.

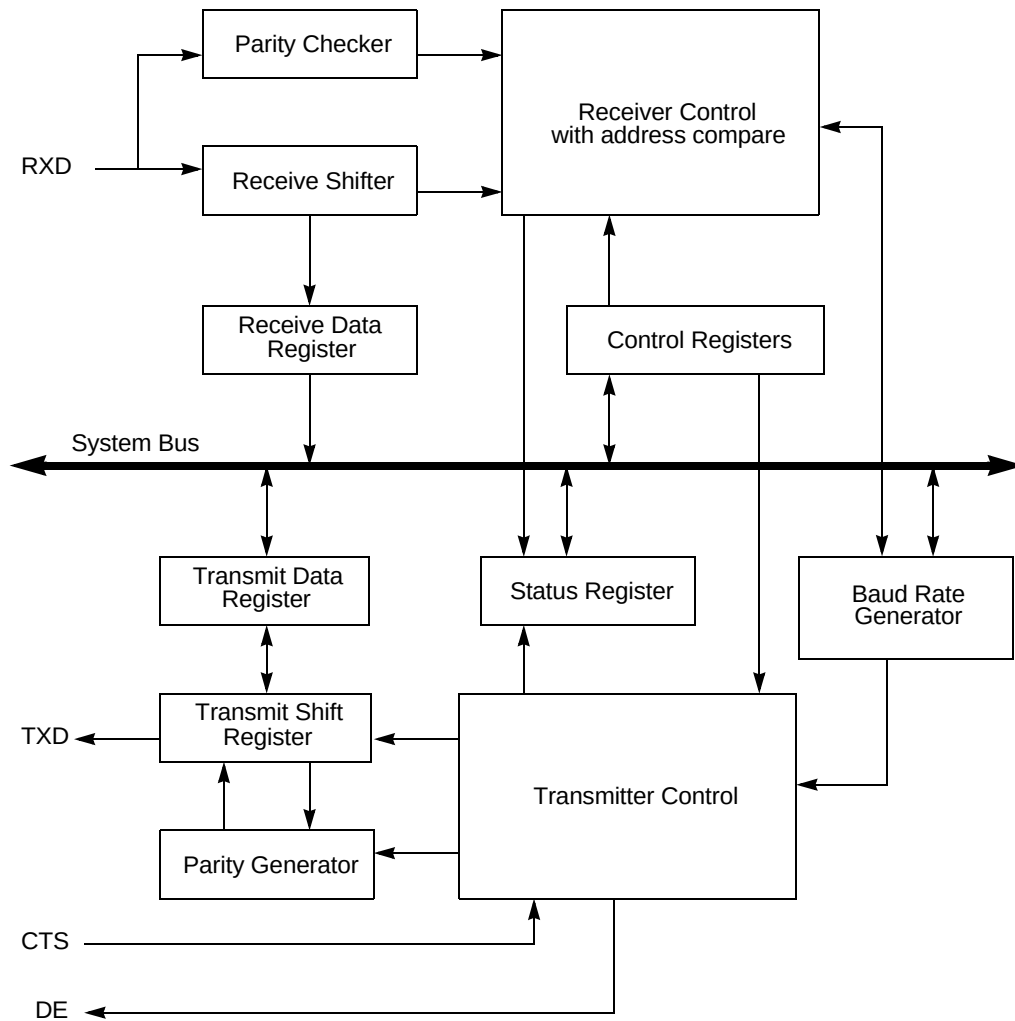


Figure 11. UART Block Diagram

Operation

Data Format

The UART always transmits and receives data in an 8-bit data format, least-significant bit first. An even or odd parity bit is optionally added to the data stream. Each character begins with an active Low *START* bit and ends with either 1 or 2 active High *STOP* bits. Figure12 on page 91 and Figure13 on page 91 display the asynchronous data format used by the UART without parity and with parity, respectively.

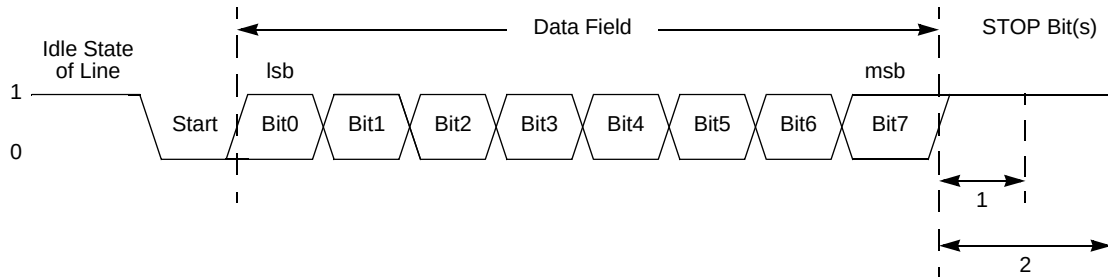


Figure 12. UART Asynchronous Data Format without Parity

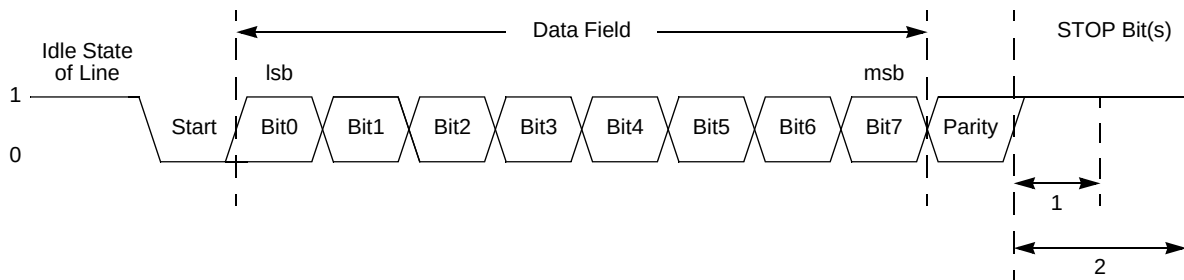


Figure 13. UART Asynchronous Data Format with Parity

Transmitting Data using Polled Method

Follow the steps below to transmit data using polled method of operation:

1. Write to the UART Baud Rate High Byte and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO Port pins for alternate function operation.
3. If MULTIPROCESSOR mode is required, write to the UART Control 1 Register to enable multiprocessor (9-bit) mode functions.
 - Set the Multiprocessor Mode Select ($\overline{\text{MPEN}}$) to enable MULTIPROCESSOR mode.
4. Write to the UART Control 0 Register to:
 - Set the transmit enable bit (TEN) to enable the UART for data transmission
 - If parity is required, and MULTIPROCESSOR mode is not enabled, set the parity enable bit (PEN) and select either even or odd parity (PSEL).
 - Set or clear the CTSE bit to enable or disable control from the remote receiver using the $\overline{\text{CTS}}$ pin.

The baud rate is set by the UART's Baud Rate Generator and supports IrDA standard baud rates from 9600 baud to 115.2 Kbaud. Higher baud rates are possible, but do not meet IrDA specifications. The UART must be enabled to use the Infrared Endec. The Infrared Endec data rate is calculated using the following equation.

$$\text{Infrared Data Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

Transmitting IrDA Data

The data to be transmitted using the infrared transceiver is first sent to the UART. The UART's transmit signal (TXD) and baud rate clock are used by the IrDA to generate the modulation signal (IR_TXD) that drives the infrared transceiver. Each UART/Infrared data bit is 16-clocks wide. If the data to be transmitted is 1, the IR_TXD signal remains low for the full 16-clock period. If the data to be transmitted is 0, a 3-clock high pulse is output following a 7-clock low period. After the 3-clock high pulse, a 6-clock low pulse is output to complete the full 16-clock data period. Figure 18 displays IrDA data transmission. When the Infrared Endec is enabled, the UART's TXD signal is internal to the Z8 Encore! XP® F0822 Series products while the IR_TXD signal is output through the TXD pin.

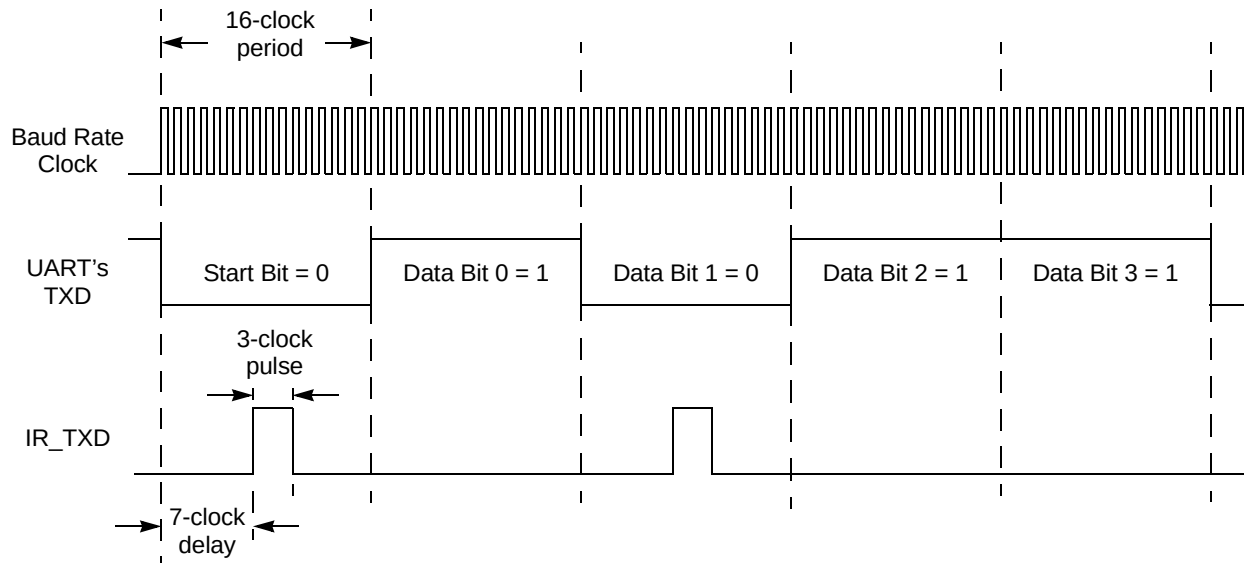


Figure 18. Infrared Data Transmission

0101 = Reserved
011X = Reserved
1XXX = Reserved

ADC Data High Byte Register

The ADC Data High Byte register contains the upper eight bits of the 10-bit ADC output. During a SINGLE-SHOT conversion, this value is invalid. Access to the ADC Data High Byte register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}. Reading the ADC Data High Byte register latches data in the ADC Low Bits register.

Table 78. ADC Data High Byte Register (ADCD_H)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_H							
RESET	X							
R/W	R							
ADDR	F72H							

ADCD_H—ADC Data High Byte

This byte contains the upper eight bits of the 10-bit ADC output. These bits are not valid during a single-shot conversion. During a continuous conversion, the last conversion output is held in this register. These bits are undefined after a Reset.

ADC Data Low Bits Register

The ADC Data Low Bits register contains the lower two bits of the conversion value. The data in the ADC Data Low Bits register is latched each time the ADC Data High Byte register is read. Reading this register always returns the lower two bits of the conversion last read into the ADC High Byte register. Access to the ADC Data Low Bits register is read-only. The full 10-bit ADC result is given by {ADCD_H[7:0], ADCD_L[7:6]}.

Table 79. ADC Data Low Bits Register (ADCD_L)

BITS	7	6	5	4	3	2	1	0
FIELD	ADCD_L		Reserved					
RESET	X							
R/W	R							
ADDR	F73H							

ADCD_L—ADC Data Low Bits

These are the least significant two bits of the 10-bit ADC output. These bits are undefined after a Reset.

Reserved

These bits are reserved and are always undefined.

frequency range for the device. The Flash Frequency High and Low Byte Registers must be loaded with the correct value to insure proper program and erase times.

Table 87. Flash Frequency High Byte Register (FFREQH)

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQH							
RESET	0							
R/W	R/W							
ADDR	FFAH							

Table 88. Flash Frequency Low Byte Register (FFREQL)

BITS	7	6	5	4	3	2	1	0
FIELD	FFREQL							
RESET	0							
R/W	R/W							
ADDR	FFBH							

FFREQH and FFREQL—Flash Frequency High and Low Bytes

These 2 bytes, {FFREQH[7:0], FFREQL[7:0]}, contain the 16-bit Flash Frequency value.

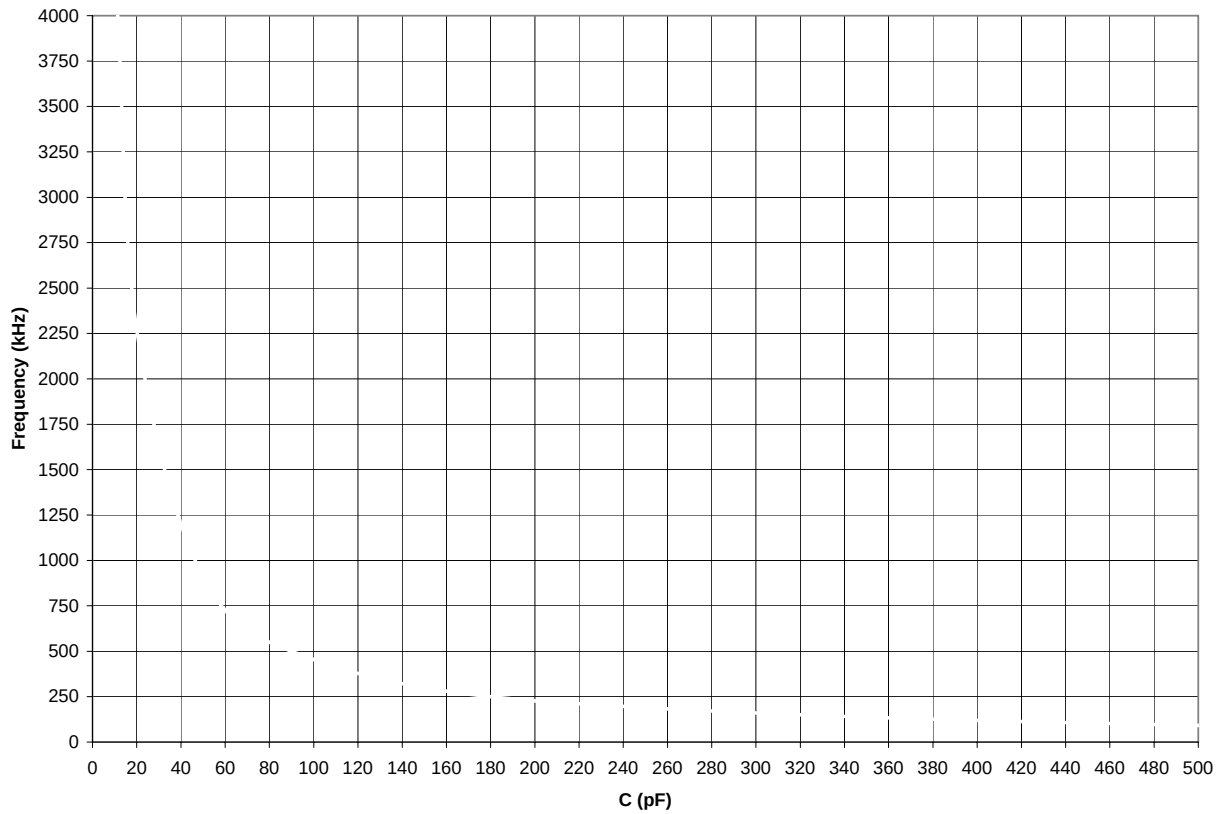


Figure 36. Typical RC Oscillator Frequency as a Function of the External Capacitance with a 45 kΩ Resistor

! Caution: *When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the Voltage Brownout threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7 V.*

DBG ← 04H
DBG ← OCDCTL[7:0]

- **Read OCD Control Register (05H)**—The Read OCD Control Register command reads the value of the OCDCTL register.

DBG ← 05H
DBG → OCDCTL[7:0]

- **Write Program Counter (06H)**—The Write Program Counter command writes the data that follows to the eZ8 CPU's Program Counter. If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, the Program Counter values are discarded.

DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]

- **Read Program Counter (07H)**—The Read Program Counter command reads the value in the eZ8 CPU's Program Counter. If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, this command returns FFFFH.

DBG ← 07H
DBG → ProgramCounter[15:8]
DBG → ProgramCounter[7:0]

- **Write Register (08H)**—The Write Register command writes data to the Register File. Data can be written 1-256 bytes at a time (256 bytes can be written by setting size to zero). If the device is not in DEBUG mode, the address and data values are discarded. If the Read Protect Option Bit is enabled, then only writes to the Flash Control Registers are allowed and all other register write data values are discarded.

DBG ← 08H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG ← 1-256 data bytes

- **Read Register (09H)**—The Read Register command reads data from the Register File. Data can be read 1-256 bytes at a time (256 bytes can be read by setting size to zero). Reading peripheral control registers through the OCD does not effect peripheral operation. For example, register bits that are normally cleared upon a read operation will not be effected (WDTSTAT register is affected by OCD read register operation). If the device is not in DEBUG mode or if the Read Protect Option Bit is enabled, this command returns FFH for all the data values.

DBG ← 09H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG → 1-256 data bytes

AC Characteristics

Table 98 provides information on the AC characteristics and timing. All AC timing information assumes a standard load of 50 pF on all outputs.

Table 98. AC Characteristics

Symbol	Parameter	$V_{DD} = 2.7 - 3.6 \text{ V}$ $T_A = -40 \text{ }^{\circ}\text{C to } 105 \text{ }^{\circ}\text{C}$		Units	Conditions
		Minimum	Maximum		
F _{SYSCLK}	System Clock Frequency (ROM)	–	20.0	MHz	
F _{SYSCLK}	System Clock Frequency (Flash)	–	20.0	MHz	Read-only from Flash memory.
		0.032768	20.0	MHz	Program or erasure of the Flash memory.
F _{XTAL}	Crystal Oscillator Frequency	0.032768	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external clock driver.
T _{XIN}	System Clock Period	50	–	ns	$T_{CLK} = 1/F_{sysclk}$
T _{XINH}	System Clock High Time	20	30	ns	$T_{CLK} = 50 \text{ ns}$
T _{XINL}	System Clock Low Time	20	30	ns	$T_{CLK} = 50 \text{ ns}$

Table 100 provides information on the external RC oscillator electrical characteristics and timing, and Table 101 provides information on the Flash memory electrical characteristics and timing.

Table 100. External RC Oscillator Electrical Characteristics and Timing

Symbol	Parameter	T _A = -40 °C to 105 °C			Units	Conditions
		Minimum	Typical ¹	Maximum		
V _{DD}	Operating Voltage Range	2.70 ¹	—	—	V	
R _{EXT}	External Resistance from XIN to VDD	40	45	200	kΩ	
C _{EXT}	External Capacitance from XIN to VSS	0	20	1000	pF	
F _{OSC}	External RC Oscillation Frequency	—	—	4	MHz	
¹ When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7 V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7 V.						

Table 101. Flash Memory Electrical Characteristics and Timing

Parameter	V _{DD} = 2.7 - 3.6V T _A = -40 °C to 105 °C			Units	Notes
	Minimum	Typical	Maximum		
Flash Byte Read Time	50	—	—	μs	
Flash Byte Program Time	20	—	40	μs	
Flash Page Erase Time	10	—	—	ms	
Flash Mass Erase Time	200	—	—	ms	
Writes to Single Address Before Next Erase	—	—	2		
Flash Row Program Time	—	—	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.

Table 116 contains additional symbols that are used throughout the Instruction Summary and Instruction Set Description sections.

Table 116. Additional Symbols

Symbol	Definition
dst	Destination Operand
src	Source Operand
@	Indirect Address Prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flags Register
RP	Register Pointer
#	Immediate Operand Prefix
B	Binary Number Suffix
%	Hexadecimal Number Prefix
H	Hexadecimal Number Suffix

Assignment of a value is indicated by an arrow. For example,

$$\text{dst} \leftarrow \text{dst} + \text{src}$$

indicates the source data is added to the destination data and the result is stored in the destination location.

Opcode Maps

A description of the opcode map data and the abbreviations are provided in Figure 57 and Table 127 on page 230. Figure 58 on page 231 and Figure 59 on page 232 provide information on each of the eZ8 CPU instructions.

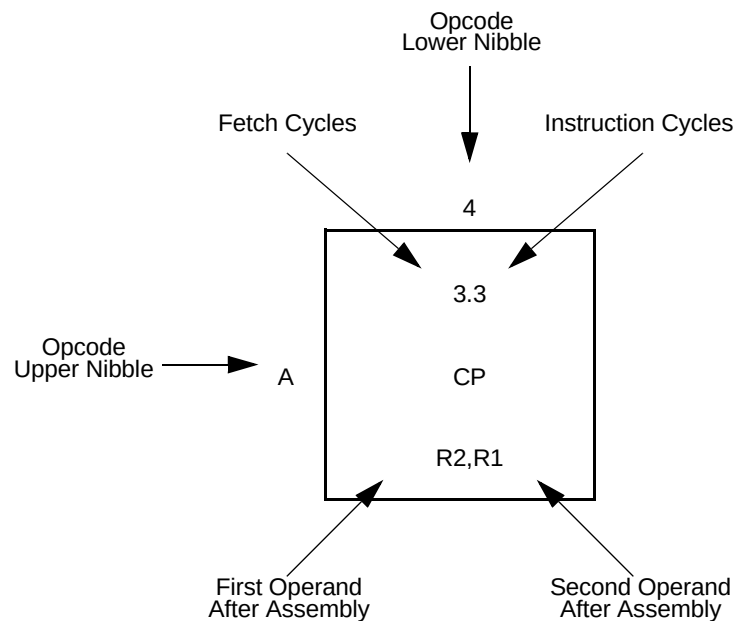


Figure 57. Opcode Map Cell Description

Table 127. Opcode Map Abbreviations

Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
cc	Condition code	p	Polarity (0 or 1)
X	8-bit signed index or displacement	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
Ir	Indirect Working Register	RA	Relative
IR	Indirect register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A			3.3 CPC r1,r2	3.4 CPC r1,lr2	4.3 CPC R2,R1	4.4 CPC IR2,R1	4.3 CPC R1,IM	4.4 CPC IR1,IM	5.3 CPCX ER2,ER1	5.3 CPCX IM,ER1						
	B																
	C	3.2 SRL R1	3.3 SRL IR1														
	D																
	E																
	F																

Figure 59. Second Opcode Map after 1FH