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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373c8t6

List of figures

2 Description

The STM32F373xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an Embedded Trace Macrocell™ (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F373xx devices offer one fast 12-bit ADC (1 Msps), three 16-bit Sigma delta ADCs, two comparators, two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F373xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F373xx family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

Table 7. STM32F373xx I^2C implementation (continued)

I^2C features(1)	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F373xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F373xx USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
51	L12	-	-	VDDSD3	S	-	(2)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S	-	-	External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(4)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(4)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN	SDADC3_AIN7P, SDADC3_AIN8M
55	K9	36	28	PD8	I/O	TC	(4)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8	-	-	PD9	I/O	TC	(4) (2)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12	-	-	PD10	I/O	TC	(4) (2)	USART3_CK	SDADC3_AIN4P
58	J11	-	-	PD11	I/O	TC	(4) (2)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10	-	-	PD12	I/O	TC	(4) (2)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P
60	H12	-	-	PD13	I/O	TC	(4) (2)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11	-	-	PD14	I/O	TC	(4) (2)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10	-	-	PD15	I/O	TC	(4) (2)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37	-	PC6	I/O	FT	(2)	TIM3_CH1, SPI1_NSS/I2S1_WS	-
64	E11	38	-	PC7	I/O	FT	(2)	TIM3_CH2, SPI1_SCK/I2S1_CK,	-
65	E10	39	-	PC8	I/O	FT	(2)	SPI1_MISO/I2S1_MCK, TIM3_CH3	-
66	D12	40	-	PC9	I/O	FT	(2)	SPI1_MOSI/I2S1_SD, TIM3_CH4	-

Table 12. Alternate functions for port PA

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF14	AF15
PA0	-	TIM2_CH1_ETR	TIM5_CH1_ETR	TSC_G1_IO1	-	-	-	USART2_CTS	COMP1_OUT	-	-	TIM19_CH1	-	EVENTOUT
PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	TSC_G1_IO2	-	-	SPI3_SCK/I2S3_CK	USART2_RTS	-	TIM15_CH1N	-	TIM19_CH2	-	EVENTOUT
PA2	-	TIM2_CH3	TIM5_CH3	TSC_G1_IO3	-	-	SPI3_MISO/I2S3_MCK	USART2_TX	COMP2_OUT	TIM15_CH1	-	TIM19_CH3	-	EVENTOUT
PA3	-	TIM2_CH4	TIM5_CH4	TSC_G1_IO4	-	-	SPI3_MOSI/I2S3_SD	USART2_RX	-	TIM15_CH2	-	TIM19_CH4	-	EVENTOUT
PA4	-	-	TIM3_CH2	TSC_G2_IO1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	-	-	TIM12_CH1	-	-	EVENTOUT
PA5	-	TIM2_CH1_ETR	-	TSC_G2_IO2	-	SPI1_SCK/I2S1_CK	-	CEC	-	TIM14_CH1	TIM12_CH2	-	-	EVENTOUT
PA6	-	TIM16_CH1	TIM3_CH1	TSC_G2_IO3	-	SPI1_MISO/I2S1_MCK	-	-	COMP1_OUT	TIM13_CH1	-	-	-	EVENTOUT
PA7	-	TIM17_CH1	TIM3_CH2	TSC_G2_IO4	-	SPI1_MOSI/I2S1_SD	-	-	COMP2_OUT	TIM14_CH1	-	-	-	EVENTOUT
PA8	MCO	-	TIM5_CH1_ETR	-	I2C2_SMBA	SPI2_SCK/I2S2_CK	-	USART1_CK	-	-	TIM4_ETR	-	-	EVENTOUT
PA9	-	-	TIM13_CH1	TSC_G4_IO1	I2C2_SCL	SPI2_MISO/I2S2_MCK	-	USART1_TX	-	TIM15_BKIN	TIM2_CH3	-	-	EVENTOUT
PA10	-	TIM17_BKIN	-	TSC_G4_IO2	I2C2_SDA	SPI2_MOSI/I2S2_SD	-	USART1_RX	-	TIM14_CH1	TIM2_CH4	-	-	EVENTOUT
PA11	-	-	TIM5_CH2	-	-	SPI2_NSS/I2S2_WS	SPI1_NSS/I2S1_WS	USART1_CTS	COMP1_OUT	CAN_RX	TIM4_CH1	-	-	EVENTOUT
PA12	-	TIM16_CH1	TIM5_CH3	-	-	-	SPI1_SCK/I2S1_CK	USART1_RTS	COMP2_OUT	CAN_TX	TIM4_CH2	-	-	EVENTOUT

Table 16. Alternate functions for port PE

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PE0	-	EVENTOUT	TIM4_ETR	-	-	-	-	USART1_TX
PE1	-	EVENTOUT	-	-	-	-	-	USART1_RX
PE2	TRACECLK	EVENTOUT	-	TSC_G7_IO1	-	-	-	-
PE3	TRACED0	EVENTOUT	-	TSC_G7_IO2	-	-	-	-
PE4	TRACED1	EVENTOUT	-	TSC_G7_IO3	-	-	-	-
PE5	TRACED2	EVENTOUT	-	TSC_G7_IO4	-	-	-	-
PE6	TRACED3	EVENTOUT	-	-	-	-	-	-
PE7	-	EVENTOUT	-	-	-	-	-	-
PE8	-	EVENTOUT	-	-	-	-	-	-
PE9	-	EVENTOUT	-	-	-	-	-	-
PE10	-	EVENTOUT	-	-	-	-	-	-
PE11	-	EVENTOUT	-	-	-	-	-	-
PE12	-	EVENTOUT	-	-	-	-	-	-
PE13	-	EVENTOUT	-	-	-	-	-	-
PE14	-	EVENTOUT	-	-	-	-	-	-
PE15	-	EVENTOUT	-	-	-	-	-	USART3_RX

Table 18. STM32F373xx peripheral register boundary addresses[1] (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. Cells in gray indicate Reserved memory locations.

6.3.16 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 56*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I^2C characteristics(1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4	-	0.6	-	0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

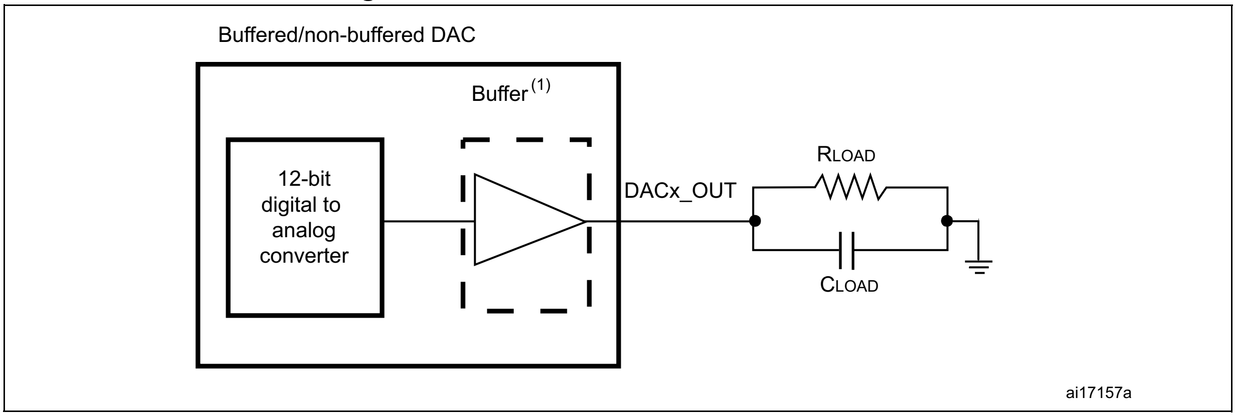
1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

Table 63. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	-	±10	mV
		Given for the DAC in 10-bit at V_{REF+} = 3.6 V	-	-	±3	LSB
		Given for the DAC in 12-bit at V_{REF+} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for the DAC in 12bit configuration	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization.

Figure 29. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 68. TIMx[1] [2] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.65	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM12, TIM13, TIM14, TIM15, TIM16 , TIM17, TIM18 and TIM19 timers.
2. Guaranteed by characterization results.

Table 69. IWDG min/max timeout period at 40 kHz (LSI) [1][2]

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.
2. Guaranteed by characterization results.

Table 70. WWDG min-max timeout value @72 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	0.05687	3.6409
2	1	0.1137	7.2817
4	2	0.2275	14.564
8	3	0.4551	29.127

Table 74. SDADC characteristics (continued)(1)

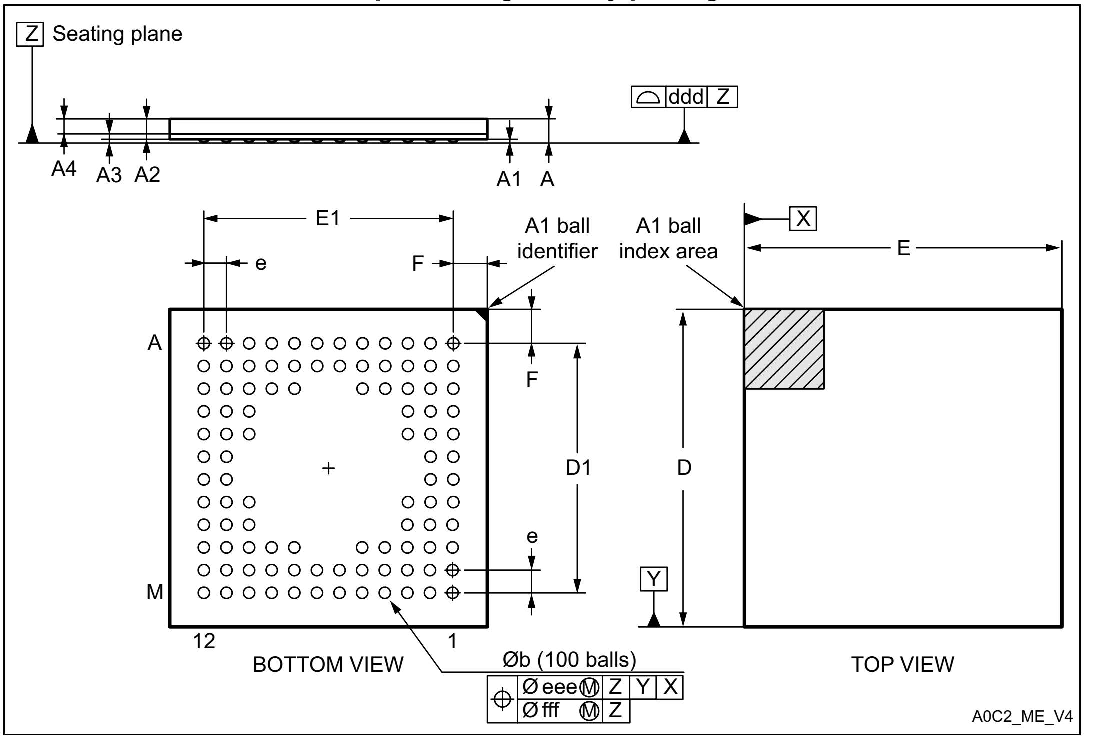
Symbol	Parameter	Conditions				Min	Typ	Max	Unit	Note
EL	Integral linearity error(2)	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	16	LSB	-
EL	Integral linearity error(2)	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	14	LSB	-
EL	Integral linearity error(2)	Differential mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	26	LSB	-
EL	Integral linearity error(2)	Differential mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	14	LSB	-
EL	Integral linearity error(2)	Single ended mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	31	LSB	-
EL	Integral linearity error(2)	Single ended mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	23	LSB	-
EL	Integral linearity error(2)	Single ended mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	80	LSB	-
EL	Integral linearity error(2)	Single ended mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	35	LSB	-
ED	Differential linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	2.4	LSB	-
ED	Differential linearity error	Differential mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	1.8	LSB	-
ED	Differential linearity error	Differential mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	3.6	LSB	-
ED	Differential linearity error	Differential mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	2.9	LSB	-
ED	Differential linearity error	Single ended mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	3.2	LSB	-
ED	Differential linearity error	Single ended mode	gain = 1	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	2.8	LSB	-
ED	Differential linearity error	Single ended mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 1.2	-	-	4.1	LSB	-
ED	Differential linearity error	Single ended mode	gain = 8	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	3.3	LSB	-

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

Figure 32. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118

Table 78. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

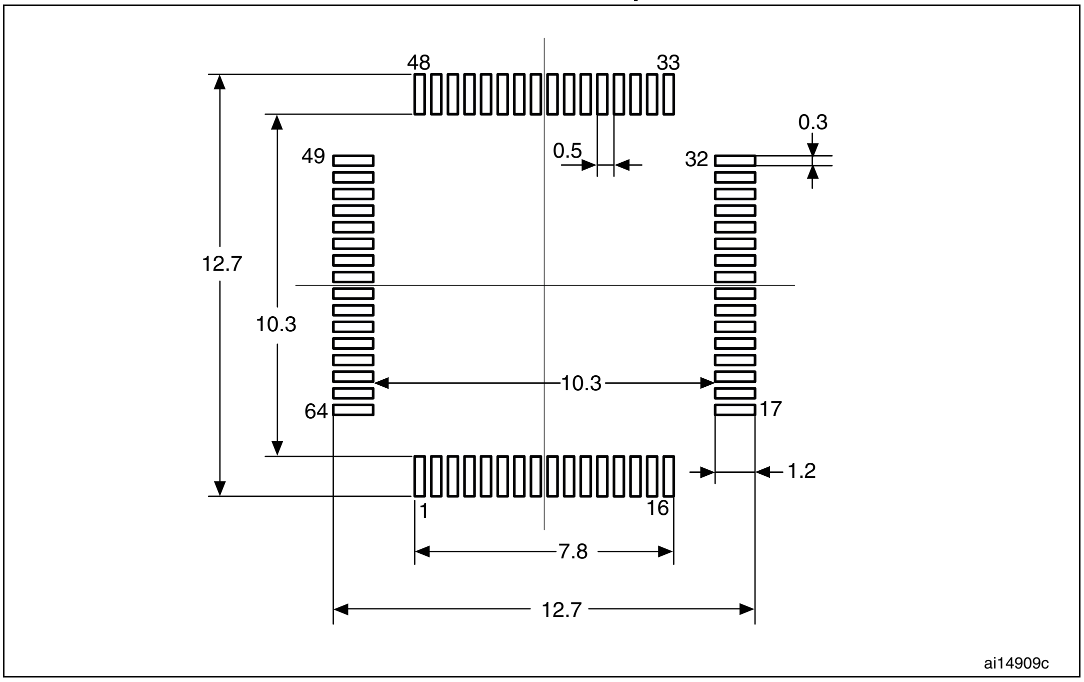
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[(1)]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

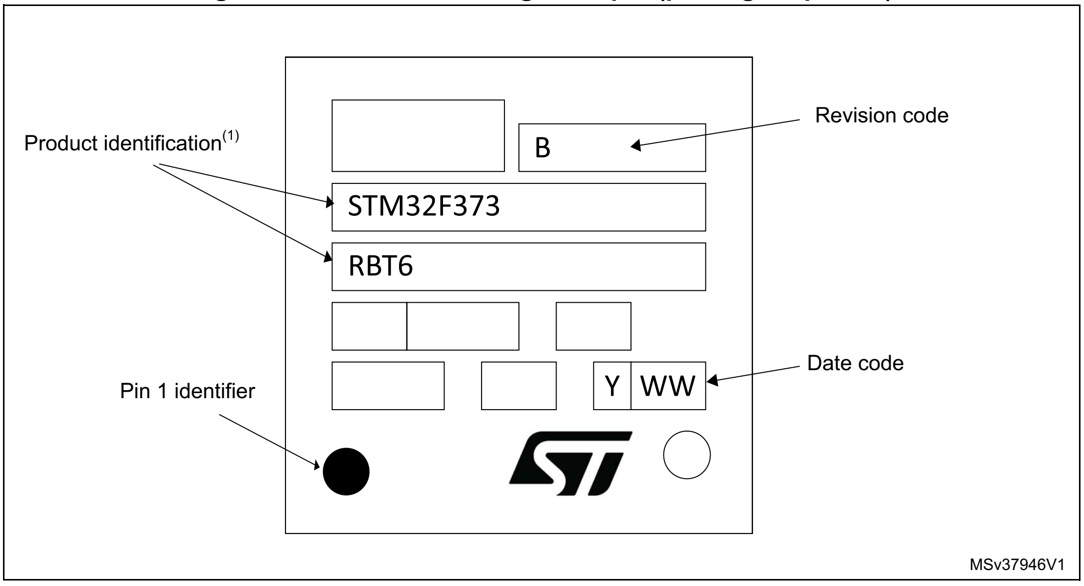


1. Dimensions are expressed in millimeters.

Device marking for LQFP64

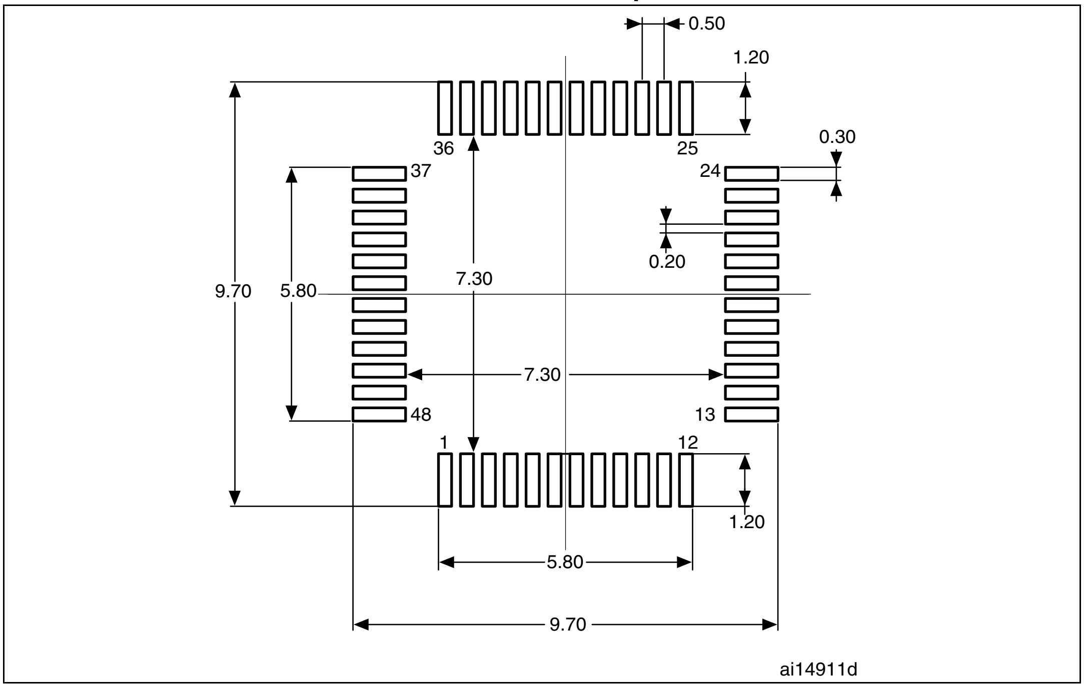
The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

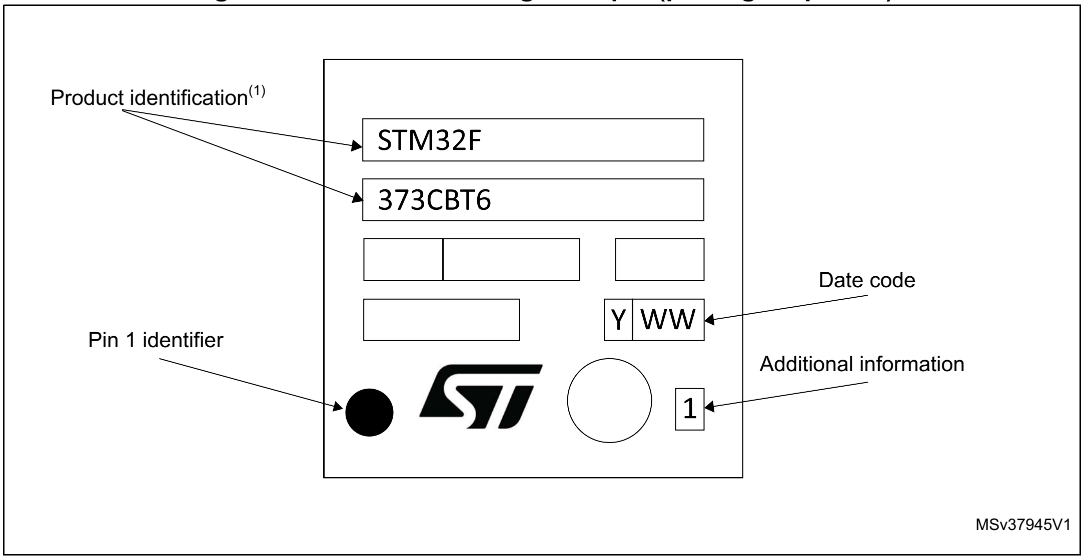


1. Dimensions are expressed in millimeters.

Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. LQFP48 marking example (package top view)



1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

Table 83. Document revision history (continued)

Date	Revision	Changes
21-Dec-2012	3	Updated *Table 2: Device overview*, capacitive sensing channels peripheral added. Updated *Table 3: Capacitive sensing GPIOs available on STM32F373xx devices* Updated *Section 3.19: Inter-integrated circuit interface (I2C)* Updated the function names in *Table 11: STM32F373 pin definitions* Updated *Table 20: Current characteristics* Updated *Table 22: General operating conditions* Updated *Table 30: Typical and maximum VDD consumption in Stop and Standby modes* Updated *Table 32: Typical and maximum current consumption from VBAT supply* Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')* Updated *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM* Added *Table 35: Switching output I/O current consumption* Added *Table 36: Peripheral current consumption*, *Figure 16: HSI oscillator accuracy characterization results* Updated *Section 6.3.6: Wakeup time from low-power mode* Updated *Table 37: Low-power mode wakeup timings* Updated *Table 47: EMS characteristics* Updated *Table 51: I/O current injection susceptibility* Updated *Table 52: I/O static characteristics* Updated , *Figure 18: TC and TTa I/O input characteristics - TTL port*, *Figure 18: Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port* and *Figure 20: Five volt tolerant (FT and FTf) I/O input characteristics - TTL port* Updated *Table 53: Output voltage characteristics* Updated *Table 54: I/O AC characteristics* Updated *Table 55: NRST pin characteristics* Updated *Table 63: DAC characteristics* Updated *Table 74: SDADC characteristics* Updated *Figure 32: LQFP100 –14 x 14 mm 100-pin low-profile quad flat package outline*, *Figure 35: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Figure 38: LQFP48 – 7 x 7 mm, 48-pin low-profile quad flat package outline* Updated *Table 72: LQPF100 – 14 x 14 mm low-profile quad flat package mechanical data*, *Table 73: LQFP64 – 10 x 10 mm low-profile quad flat package mechanical data* and *Table 74: LQFP48 – 7 x 7 mm, low-profile quad flat package mechanical data* Added *Figure 16: HSI oscillator accuracy characterization results*

Table 83. Document revision history (continued)

Date	Revision	Changes
18-Mar-2014	5	Renamed part number STM32F37x to STM32F373xx Added note1 in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V* Updated *Chapter 3.14: Digital-to-analog converter (DAC)* Updated, added note 2 and 3 in *Table 57: I2C analog filter characteristics* Renamed t_{SP} symbol with $t_{AF.}$ Added note for EG Symbol in *Table 74: SDADC characteristics* Added all packages top view
21-Jul-2015	6	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.4* Updated *Table 11: STM32F373xx pin definitions*, *Table 19: Voltage characteristics*, *Table 49: ESD absolute maximum ratings*, *Table 74: SDADC characteristics*, *Table 76: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, and *Table 78: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* Updated *Figure 2: STM32F373xx LQFP48 pinout*, *Figure 9: Power supply scheme*, *Figure 32: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline*, *Figure 34: UFBGA100 marking example (package top view)*, *Figure 36: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 37: LQFP100 marking example (package top view)*, *Figure 38: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 39: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 40: LQFP64 marking example (package top view)*, *Figure 42: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 43: LQFP48 marking example (package top view)*. Added *Table 32: Typical and maximum current consumption from VBAT supply*, *Table 49: ESD absolute maximum ratings*, *Table 64: Comparator characteristics*, *Table 77: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 30: Maximum VREFINT scaler startup time from power down*, *Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.