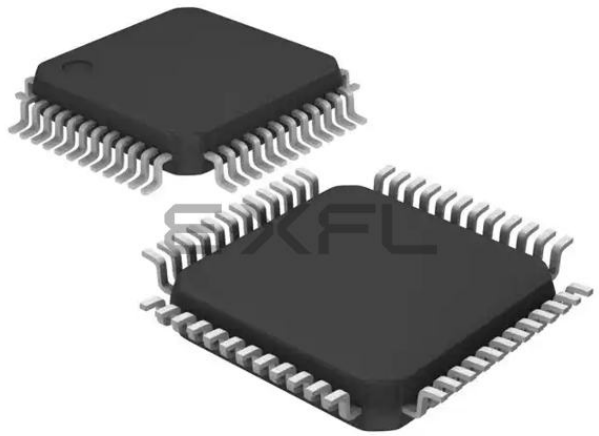

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373c8t6tr

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F373xx (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, 4, 5 and 19

  These five timers are full-featured general-purpose timers:

  – TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers

  – TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM12, 13, 14, 15, 16, 17

  These six timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM12 has 2 channels

  – TIM13 and TIM14 have 1 channel

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.2 Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
51	L12	-	-	VDDSD3	S	-	(2)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S	-	-	External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(4)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(4)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN	SDADC3_AIN7P, SDADC3_AIN8M
55	K9	36	28	PD8	I/O	TC	(4)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8	-	-	PD9	I/O	TC	(4) (2)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12	-	-	PD10	I/O	TC	(4) (2)	USART3_CK	SDADC3_AIN4P
58	J11	-	-	PD11	I/O	TC	(4) (2)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10	-	-	PD12	I/O	TC	(4) (2)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P
60	H12	-	-	PD13	I/O	TC	(4) (2)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11	-	-	PD14	I/O	TC	(4) (2)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10	-	-	PD15	I/O	TC	(4) (2)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37	-	PC6	I/O	FT	(2)	TIM3_CH1, SPI1_NSS/I2S1_WS	-
64	E11	38	-	PC7	I/O	FT	(2)	TIM3_CH2, SPI1_SCK/I2S1_CK,	-
65	E10	39	-	PC8	I/O	FT	(2)	SPI1_MISO/I2S1_MCK, TIM3_CH3	-
66	D12	40	-	PC9	I/O	FT	(2)	SPI1_MOSI/I2S1_SD, TIM3_CH4	-

Table 18. STM32F373xx peripheral register boundary addresses(1)

Bus	Boundary address	Size	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800- 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
-	0x4001 6C00 - 0x4001 FFFF	37 KB	Reserved

Table 18. STM32F373xx peripheral register boundary addresses(1) (continued)

Bus	Boundary address	Size	Peripheral
APB1	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3/I2S3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2/I2S2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 1C00 - 0x4000 1FFF	1 KB	TIM13
	0x4000 1800 - 0x4000 1BFF	1 KB	TIM12
	0x4000 1400 - 0x4000 17FF	1 KB	TIM7
	0x4000 1000 - 0x4000 13FF	1 KB	TIM6
	0x4000 0C00 - 0x4000 0FFF	1 KB	TIM5
	0x4000 0800 - 0x4000 0BFF	1 KB	TIM4
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

1. Cells in gray indicate Reserved memory locations.

Table 22. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(5)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(5)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 60: ADC characteristics*.
2. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
3. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS).
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 23* are derived from tests performed under the ambient temperature condition summarized in *Table 22*.

Table 23. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33	-	-	-	
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4	-	-	-	

1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Guaranteed by characterization results.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 37. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.1	3.9	3.8	3.7	3.6	4.5	µs
		Regulator in low power mode	7.9	6.7	6.1	5.7	5.4	8.6	
$t_{WUSTANDBY}$	Wakeup from Standby mode	LSI and IWDG off	62.6	53.7	49.2	45.7	42.7	100	
$t_{WUSLEEP}$	Wakeup from Sleep mode	After WFE instruction	6						CPU clock cycles

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 12*.

Table 38. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0			
V_{HSEH}	OSC_IN input pin high level voltage	-	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	-	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	-	20	

1. Guaranteed by design.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07^{(2)}$	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2^{(2)}$	
		BOOT0	-	-	$0.3V_{DD}-0.3^{(2)}$	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398^{(2)}$	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}{}^{(2)}$	-	-	
		BOOT0	$0.2V_{DD}+0.95^{(2)}$	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(2)}$	-	mV
		FT and FTf I/O	-	$100^{(2)}$	-	
		BOOT0	-	$300^{(2)}$	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa in digital mode $V_{SS} < V_{IN} < V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Guaranteed by design.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

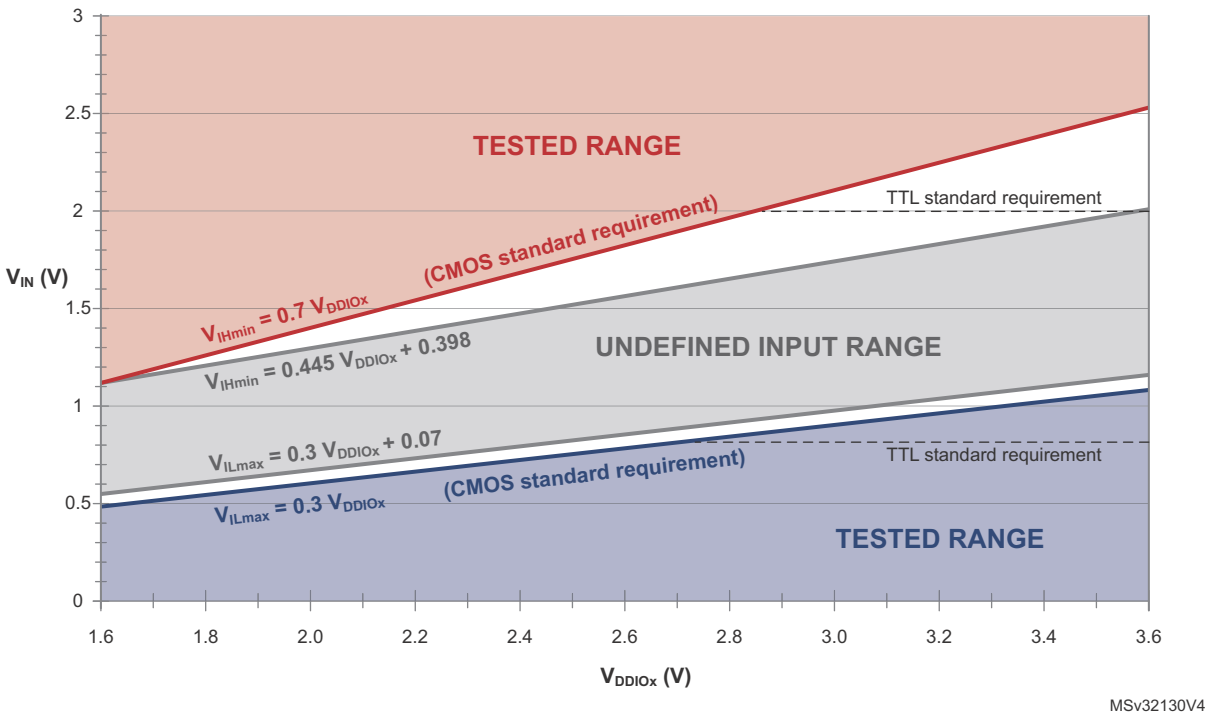
- The PB2, PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 52 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 17* for standard I/Os, and in *Figure 18* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 17. TC and TTa I/O input characteristics - CMOS port



Output voltage levels

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 53. Output voltage characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	CMOS port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH}(4)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL}(2)	Output low level voltage for an I/O pin	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	
V_{OH} (4)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–1.3	-	
V_{OL}(2)(5)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	
V_{OH}(4)(5)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OLFM+}(2)	Output low level voltage for a FTf I/O pins in FM+ mode	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	

1. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (the I/O ground pin is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O ground pin is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 20* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
5. Guaranteed by design.

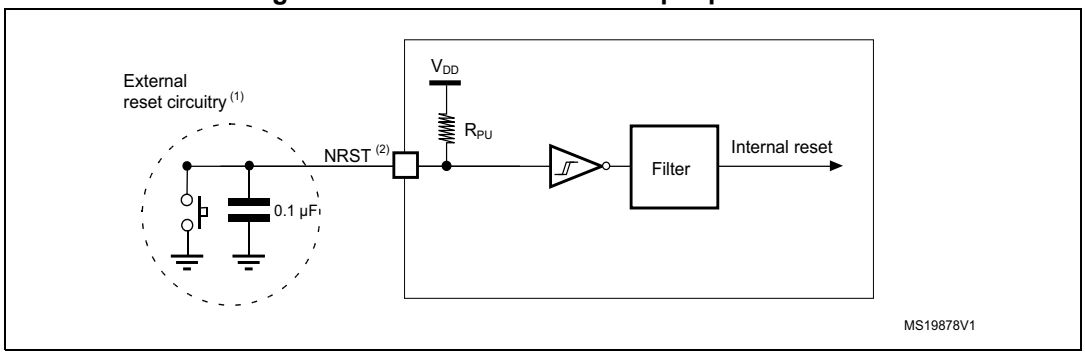
Note: I/O pins are powered from V_{DD} voltage except pins which can be used as SDADC inputs:

- The PB2, PB10 and PE7 to PE15 I/O pins are powered from V_{DDSD12}.

- PB14 to PB15 and PD8 to PD15 I/O pins are powered from V_{DDSD3}. All I/O pin ground is internally connected to V_{SS}.

V_{DD} mentioned in the Table 53 represents power voltage for a given I/O pin (V_{DD} or V_{DDSD12} or V_{DDSD3}).

Figure 20. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 55*. Otherwise the reset will not be taken into account by the device.

6.3.16 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 56*. Refer also to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 56. I^2C characteristics(1)

Symbol	Parameter	Standard		Fast mode		Fast mode +		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
t_{LOW}	Low period of the SCL clock	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	High Period of the SCL clock	4	-	0.6	-	0.26	-	µs
tr	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	300	-	120	ns
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45(2)	-	0.9(2)	-	0.45(2)	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	ns
$t_{HD;STA}$	Hold time (repeated) START condition	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0	-	0.6	-	0.26	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	0.5	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	-	550	pF

1. The I2C characteristics are the requirements from the I2C bus specification rev03. They are guaranteed by design when the I2Cx_TIMING register is correctly programmed (refer to reference manual). These characteristics are not tested in production.
2. The maximum $t_{HD;DAT}$ could be 3.45 µs, 0.9 µs and 0.45 µs for standard mode, fast mode and fast mode plus, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}$(1)	Current consumption from V_{DDA}	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160(2)	220(2)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(3)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{SRC}(3)	Signal source impedance	See *Equation 1* and *Table 61* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	-	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

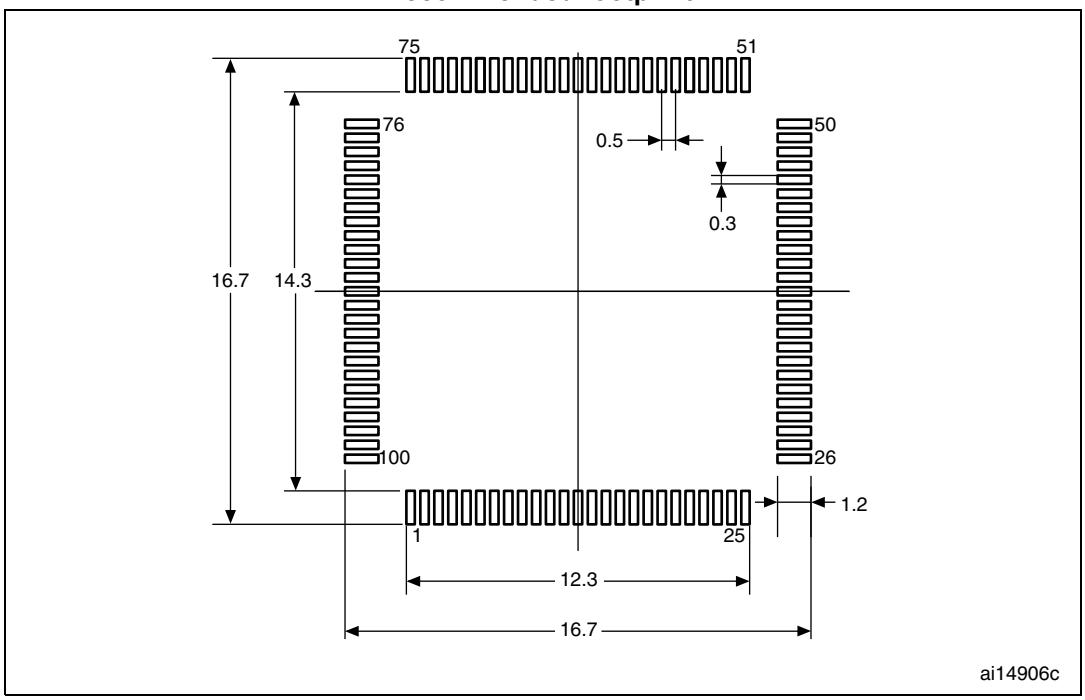
1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers

Table 78. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint

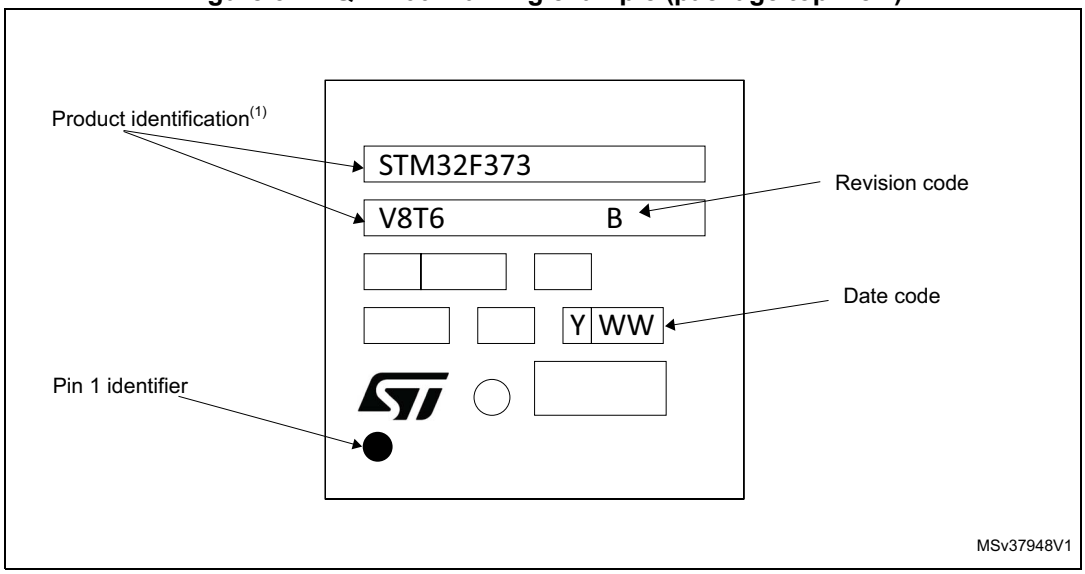


1. Dimensions are expressed in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 37. LQFP100 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.