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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373cbt7

2 Description

The STM32F373xx family is based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 72 MHz, and embedding a floating point unit (FPU), a memory protection unit (MPU) and an Embedded Trace Macrocell™ (ETM). The family incorporates high-speed embedded memories (up to 256 Kbyte of Flash memory, up to 32 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32F373xx devices offer one fast 12-bit ADC (1 Msps), three 16-bit Sigma delta ADCs, two comparators, two DACs (DAC1 with 2 channels and DAC2 with 1 channel), a low-power RTC, 9 general-purpose 16-bit timers, two general-purpose 32-bit timers, three basic timers.

They also feature standard and advanced communication interfaces: two I2Cs, three SPIs, all with muxed I2Ss, three USARTs, CAN and USB.

The STM32F373xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F373xx family offers devices in five packages ranging from 48 pins to 100 pins. The set of included peripherals changes with the device chosen.

3.7.4 Low-power modes

The STM32F373xx supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the USARTs, the I2Cs, the CEC, the USB wakeup, the COMPx and the RTC alarm.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.8 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz, while the maximum allowed frequency of the low speed APB domain is 36 MHz.

3.9 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.12 12-bit analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter is based on a successive approximation register (SAR) architecture. It has up to 16 external channels (AIN15:0) and 3 internal channels (temperature sensor, voltage reference, V_{BAT} voltage measurement) performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx) can be internally connected to the ADC start and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

3.12.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 65: Temperature sensor calibration values on page 105*.

3.12.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

3.12.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

Table 3. Capacitive sensing GPIOs available on STM32F373xx devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

1. This GPIO offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

Table 4. No. of capacitive sensing channels available on STM32F373xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F373Cx	STM32F373Rx	STM32F373Vx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3 V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. STM32F373xx pin definitions

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
1	B2	-	-	PE2	I/O	FT	(2)	TSC_G7_IO1, TRACECLK	-
2	A1	-	-	PE3	I/O	FT	(2)	TSC_G7_IO2, TRACED0	-
3	B1	-	-	PE4	I/O	FT	(2)	TSC_G7_IO3, TRACED1	-
4	C2	-	-	PE5	I/O	FT	(2)	TSC_G7_IO4, TRACED2	-
5	D2	-	-	PE6	I/O	FT	(2)	TRACED3	WKUP3, RTC_TAMPER3
6	E2	1	1	VBAT	S	-	-	Backup power supply	
7	C1	2	2	PC13(1)	I/O	TC	-	-	WKUP2, ALARM_OUT, CALIB_OUT, TIMESTAMP, RTC_TAMPER1

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
38	M7	-	-	PE7	I/O	TC	(3) (2)	-	SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	PE8	I/O	TC	(3)	-	SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	PE9	I/O	TC	(3)	-	SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8	-	-	PE10	I/O	TC	(3) (2)	-	SDADC1_AIN2P
42	M9	-	-	PE11	I/O	TC	(3) (2)	-	SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P
43	L9	-	-	PE12	I/O	TC	(3) (2)	-	SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10	-	-	PE13	I/O	TC	(3) (2)	-	SDADC1_AIN0M , SDADC2_AIN2P
45	M11	-	-	PE14	I/O	TC	(3) (2)	-	SDADC2_AIN1P, SDADC2_AIN2M
46	M12	-	-	PE15	I/O	TC	(3) (2)	USART3_RX	SDADC2_AIN0P
47	L10	-	-	PB10	I/O	TC	(3) (2)	SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	SDADC2_AIN0M
48	L11	-	-	VREFSD-	S	-	(2)	External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
49	F12	-	-	VSSSD	S	-	(2)	SDADC1, SDADC2, SDADC3 ground	
-	-	31	23	VSSSD/ VREFSD-	S	-	-	SDADC1, SDADC2, SDADC3 ground / External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
50	G12	-	-	VDDSD12	S	-	(2)	SDADC1 and SDADC2 power supply	
-	-	32	24	VDDSD	S	-	-	SDADC1, SDADC2, SDADC3 power supply	

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
51	L12	-	-	VDDSD3	S	-	(2)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S	-	-	External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(4)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(4)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN	SDADC3_AIN7P, SDADC3_AIN8M
55	K9	36	28	PD8	I/O	TC	(4)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8	-	-	PD9	I/O	TC	(4) (2)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12	-	-	PD10	I/O	TC	(4) (2)	USART3_CK	SDADC3_AIN4P
58	J11	-	-	PD11	I/O	TC	(4) (2)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10	-	-	PD12	I/O	TC	(4) (2)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P
60	H12	-	-	PD13	I/O	TC	(4) (2)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11	-	-	PD14	I/O	TC	(4) (2)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10	-	-	PD15	I/O	TC	(4) (2)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37	-	PC6	I/O	FT	(2)	TIM3_CH1, SPI1_NSS/I2S1_WS	-
64	E11	38	-	PC7	I/O	FT	(2)	TIM3_CH2, SPI1_SCK/I2S1_CK,	-
65	E10	39	-	PC8	I/O	FT	(2)	SPI1_MISO/I2S1_MCK, TIM3_CH3	-
66	D12	40	-	PC9	I/O	FT	(2)	SPI1_MOSI/I2S1_SD, TIM3_CH4	-

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DDSDx}, V_{BAT} and V_{DD})	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for V_{DD} > V_{DDA}	-	0.4	
V_{DDSDx} – V_{DDA}	Allowed voltage difference for V_{DDSDx} > V_{DDA}	-	0.4	
V_{REFSD+} – V_{DDSD3}	Allowed voltage difference for V_{REFSD+} > V_{DDSD3}	-	0.4	
V_{REF+} – V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	
	Input voltage on TC pins on SDADCx channels inputs(3)	V_{SS} - 0.3	4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$\lvert V_{REFSD-} - V_{SSx}\rvert$		-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to V_{SS}).

All main power (V_{DD}, V_{DDSD12}, V_{DDSD3} and V_{DDA}) and ground (V_{SS}, V_{SSSD}, and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

The following relationship must be respected between V_{DDA} and V_{DDSD12}: V_{DDA} must power on before or at the same time as V_{DDSD12} or V_{DDSD3} in the power up sequence. V_{DDA} must be greater than or equal to V_{DDSD12} or V_{DDSD3}.

The following relationship must be respected between V_{DDSD12} and V_{DDSD3}: V_{DDSD3} must power on before or at the same time as V_{DDSD12} in the power up sequence.
After power up (V_{DDSD12} > Vrefint = 1.2 V) V_{DDSD3} can be higher or lower than V_{DDSD12}.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I_{DDA}(1)(2)	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	µA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
$I_{SDADC12}$ + I_{SDADC3}	Supply currents in Run mode from V_{DDSD12} and V_{DDSD3} (SDADCs are off)	-	-	2.5	1	µA

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.
2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 10 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 10 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07^{(2)}$	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2^{(2)}$	
		BOOT0	-	-	$0.3V_{DD}-0.3^{(2)}$	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398^{(2)}$	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}{}^{(2)}$	-	-	
		BOOT0	$0.2V_{DD}+0.95^{(2)}$	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(2)}$	-	mV
		FT and FTf I/O	-	$100^{(2)}$	-	
		BOOT0	-	$300^{(2)}$	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa in digital mode $V_{SS} < V_{IN} < V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Guaranteed by design.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 54*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 22*.

Table 54. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12(3)	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)	CL = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time		-	12	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	34	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

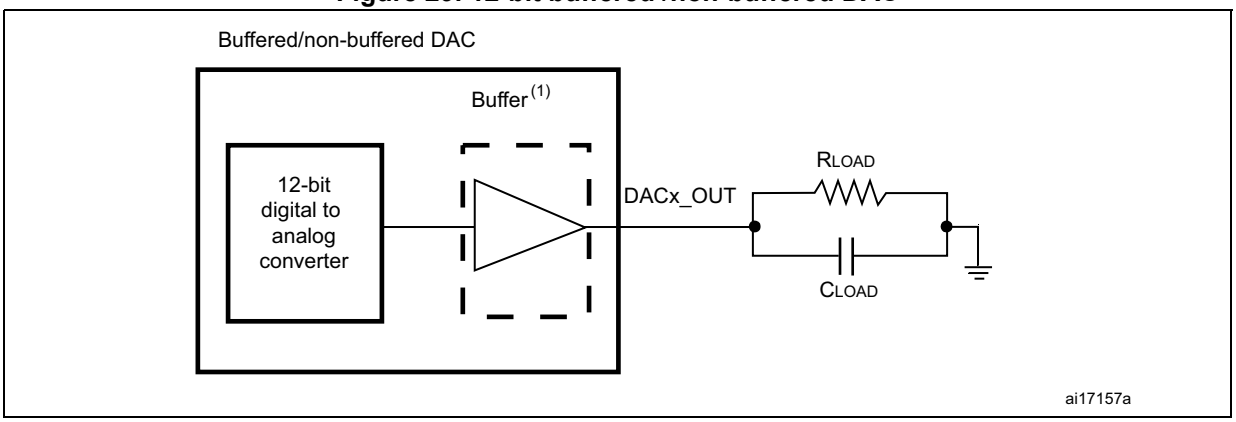
1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0313 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 19*.
3. Guaranteed by design.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F37xx reference manual RM0313 for a description of FM+ I/O mode configuration

Table 63. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	-	±10	mV
		Given for the DAC in 10-bit at V_{REF+} = 3.6 V	-	-	±3	LSB
		Given for the DAC in 12-bit at V_{REF+} = 3.6 V	-	-	±12	LSB
Gain error(3)	Gain error	Given for the DAC in 12bit configuration	-	-	±0.5	%
$t_{SETTLING}$(3)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	3	4	µs
Update rate(3)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ	-	-	1	MS/s
t_{WAKEUP}(3)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.	-	6.5	10	µs
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	No R_{LOAD}, C_{LOAD} = 50 pF	-	-67	-40	dB

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization.

Figure 29. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

Table 74. SDADC characteristics (continued)(1)

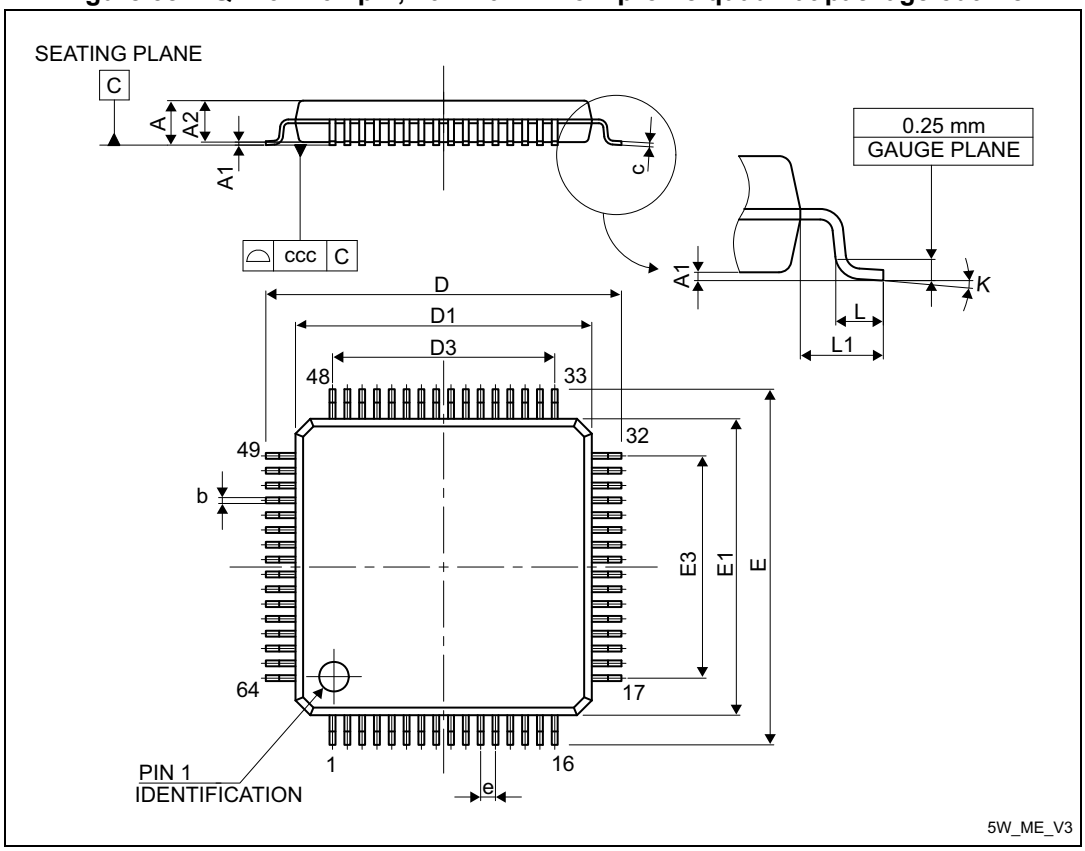
Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
EO	Offset error	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3	-	-	110	uV	after offset calibration
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	110		
						V_{REFSD+} = 3.3	-	-	100		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2	-	-	70		
						V_{REFSD+} = 3.3	-	-	100		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	-	-	90		
		Single ended mode	gain = 1	-		V_{REFSD+} = 1.2	-	-	2100		
						V_{REFSD+} = 3.3	-	-	2000		
			gain = 8			V_{REFSD+} = 1.2	-	-	1500		
						V_{REFSD+} = 3.3	-	-	1800		
$D_{voffsettemp}$	Offset drift with temperature	Differential or single ended mode, gain = 1, V_{DDSDx} = 3.3 V					-	10	15	uV/K	-
EG	Gain error	All gains, differential mode, single ended mode					-2.4	-2.7	-3.1	%	negative gain error = data result are greater than ideal
EGT	Gain drift with temperature	gain = 1, differential mode, single ended mode					-	0	-	ppm /K	-

Table 74. SDADC characteristics (continued)(1)

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SNR(5)	Signal to noise ratio	Differential mode	gain = 1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3(3)	84	85	-	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	86	88	-		
						V_{REFSD+} = 3.3	88	92	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	76	78	-		
						V_{REFSD+} = 3.3	82	86	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3(3)	76	80	-		
		Single ended mode	gain = 1	f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3	80	84	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	77	81	-		
						V_{REFSD+} = 3.3	85	90	-		
			gain = 8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2(4)	66	71	-		
						V_{REFSD+} = 3.3	74	78	-		

7.3 LQFP64 package information

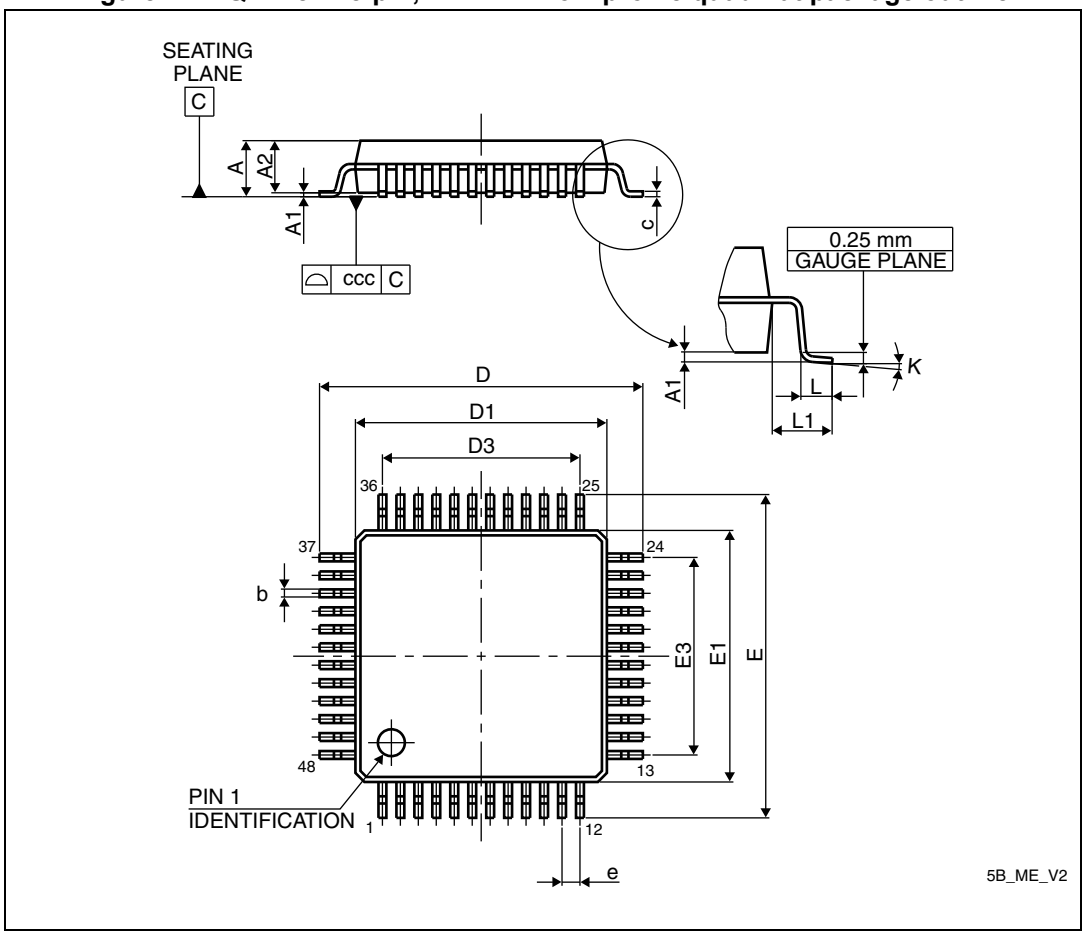
Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.4 LQFP48 package information

Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 83. Document revision history (continued)

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 28: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F373xx I2C implementation* Added *Table 8: STM32F373xx USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F373xx UFBGA100 ballout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F373xx pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F373xx pin definitions* Modified "x_CK" occurrences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Figure 9: Power supply scheme* Added Caution after *Figure 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.5.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*

Table 83. Document revision history (continued)

Date	Revision	Changes
18-Mar-2014	5	Renamed part number STM32F37x to STM32F373xx Added note1 in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V* Updated *Chapter 3.14: Digital-to-analog converter (DAC)* Updated, added note 2 and 3 in *Table 57: I2C analog filter characteristics* Renamed t_{SP} symbol with t_{AF}. Added note for EG Symbol in *Table 74: SDADC characteristics* Added all packages top view
21-Jul-2015	6	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.4* Updated *Table 11: STM32F373xx pin definitions*, *Table 19: Voltage characteristics*, *Table 49: ESD absolute maximum ratings*, *Table 74: SDADC characteristics*, *Table 76: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, and *Table 78: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* Updated *Figure 2: STM32F373xx LQFP48 pinout*, *Figure 9: Power supply scheme*, *Figure 32: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline*, *Figure 34: UFBGA100 marking example (package top view)*, *Figure 36: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 37: LQFP100 marking example (package top view)*, *Figure 38: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 39: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 40: LQFP64 marking example (package top view)*, *Figure 42: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 43: LQFP48 marking example (package top view)*. Added *Table 32: Typical and maximum current consumption from VBAT supply*, *Table 49: ESD absolute maximum ratings*, *Table 64: Comparator characteristics*, *Table 77: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 30: Maximum VREFINT scaler startup time from power down*, *Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.