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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373cct6tr

Contents

3.17.1 General-purpose timers (TIM2 to TIM5, TIM12 to TIM17, TIM19)

There are eleven synchronizable general-purpose timers embedded in the STM32F373xx (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2, 3, 4, 5 and 19

  These five timers are full-featured general-purpose timers:

  – TIM2 and TIM5 have 32-bit auto-reload up/downcounters and 32-bit prescalers

  – TIM3, 4, and 19 have 16-bit auto-reload up/downcounters and 16-bit prescalers

  These timers all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together, or with the other general-purpose timers via the Timer Link feature for synchronization or event chaining.

  The counters can be frozen in debug mode.

  All have independent DMA request generation and support quadrature encoders.

- TIM12, 13, 14, 15, 16, 17

  These six timers general-purpose timers with mid-range features:

  They have 16-bit auto-reload upcounters and 16-bit prescalers.

  – TIM12 has 2 channels

  – TIM13 and TIM14 have 1 channel

  – TIM15 has 2 channels and 1 complementary channel

  – TIM16 and TIM17 have 1 channel and 1 complementary channel

  All channels can be used for input capture/output compare, PWM or one-pulse mode output.

  The timers can work together via the Timer Link feature for synchronization or event chaining. The timers have independent DMA request generation.

  The counters can be frozen in debug mode.

3.17.2 Basic timers (TIM6, TIM7, TIM18)

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Table 7. STM32F373xx I²C implementation (continued)

I²C features(1)	I2C1	I2C2
SMBus	X	X
Wakeup from STOP	X	X

1. X = supported.

3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F373xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F373xx USART implementation

USART modes/features(1)	USART1	USART2	USART3
Hardware flow control for modem	X	X	X
Continuous communication using DMA	X	X	X
Multiprocessor communication	X	X	X
Synchronous mode	X	X	X
Smartcard mode	X	X	X
Single-wire half-duplex communication	X	X	X
IrDA SIR ENDEC block	X	X	X
LIN mode	X	X	X
Dual clock domain and wakeup from Stop mode	X	X	X
Receiver timeout interrupt	X	X	X
Modbus communication	X	X	X
Auto baud rate detection	X	X	X
Driver Enable	X	X	X

1. X = supported.

Figure 4. STM32F373xx LQFP100 pinout

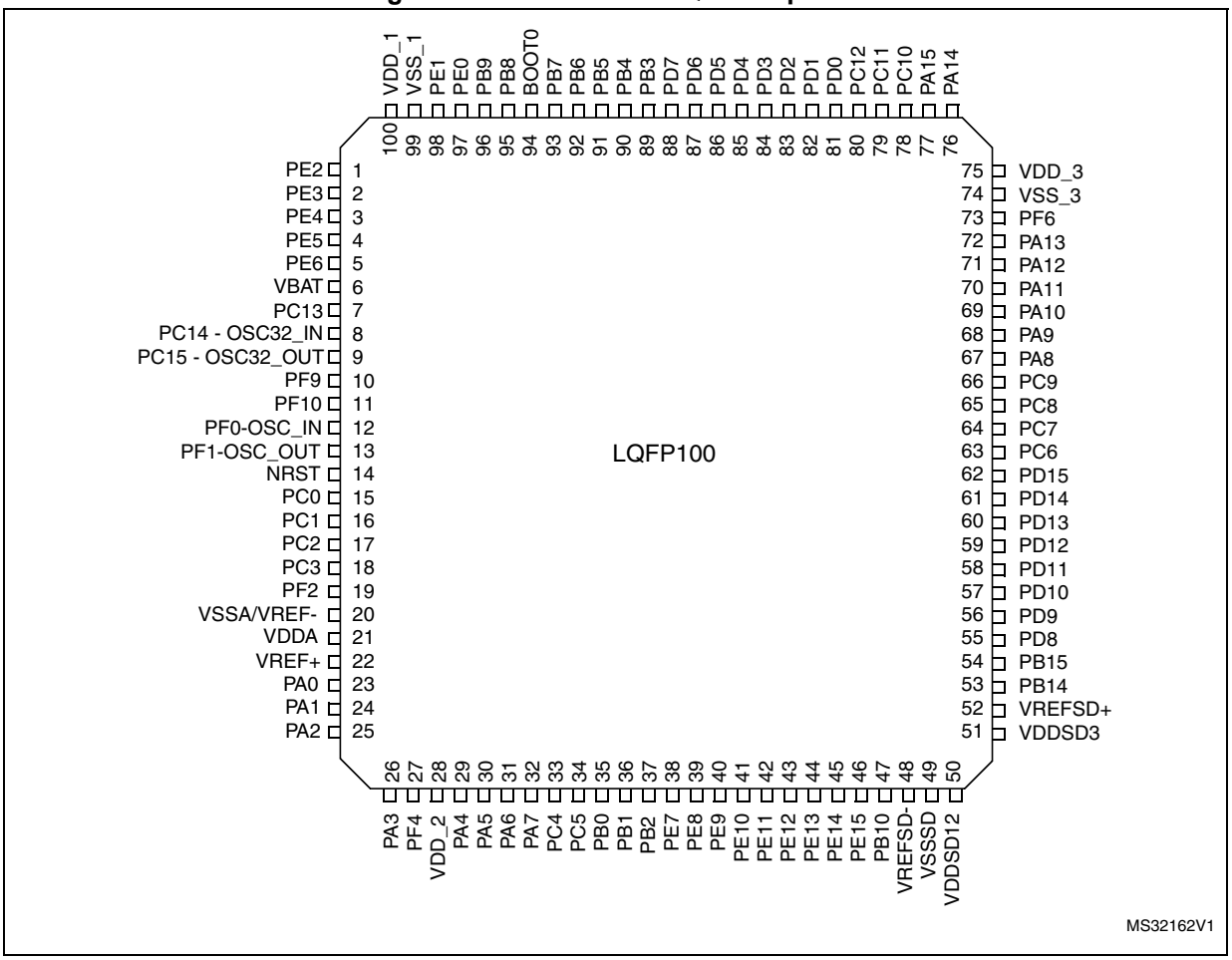


Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
67	D11	41	29	PA8	I/O	FT	-	SPI2_SCK/I2S2_CK, I2C2_SMBA, USART1_CK, TIM4_ETR, TIM5_CH1_ETR, MCO	-
68	D10	42	30	PA9	I/O	FTf	-	SPI2_MISO/I2S2_MCK, I2C2_SCL, USART1_TX, TIM2_CH3, TIM15_BKIN, TIM13_CH1, TSC_G4_IO1	-
69	C12	43	31	PA10	I/O	FTf	-	SPI2_MOSI/I2S2_SD, I2C2_SDA, USART1_RX, TIM2_CH4, TIM17_BKIN, TIM14_CH1, TSC_G4_IO2	-
70	B12	44	32	PA11	I/O	FT	-	SPI2_NSS/I2S2_WS, SPI1_NSS/I2S1_WS, USART1_CTS, CAN_RX, TIM4_CH1, USB_DM, TIM5_CH2, COMP1_OUT	-
71	A12	45	33	PA12	I/O	FT	-	SPI1_SCK/I2S1_CK, USART1_RTS, CAN_TX, USB_DP, TIM16_CH1, TIM4_CH2, TIM5_CH3, COMP2_OUT	-
72	A11	46	34	PA13	I/O	FT	-	SPI1_MISO/I2S1_MCK, USART3_CTS, IR_OUT, TIM16_CH1N, TIM4_CH3, TIM5_CH4, TSC_G4_IO3, SWDIO-JTMS	-
73	C11	47	35	PF6	I/O	FTf	-	SPI1_MOSI/I2S1_SD, USART3_RTS, TIM4_CH4, I2C2_SCL	-
74	F11	-	-	VSS_3	S	-	(2)	Ground	
75	G11	-	-	VDD_3	S	-	(2)	Digital power supply	
-	-	48	36	PF7	I/O	FTf	-	I2C2_SDA, USART2_CK	-
76	A10	49	37	PA14	I/O	FTf	-	I2C1_SDA, TIM12_CH1, TSC_G4_IO4, SWCLK-JTCK	-

Table 18. STM32F373xx peripheral register boundary addresses(1)

Bus	Boundary address	Size	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800- 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
-	0x4001 6C00 - 0x4001 FFFF	37 KB	Reserved

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 19. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DDSDx}, V_{BAT} and V_{DD})	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for V_{DD} > V_{DDA}	-	0.4	
V_{DDSDx} – V_{DDA}	Allowed voltage difference for V_{DDSDx} > V_{DDA}	-	0.4	
V_{REFSD+} – V_{DDSD3}	Allowed voltage difference for V_{REFSD+} > V_{DDSD3}	-	0.4	
V_{REF+} – V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA}	-	0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	
	Input voltage on TC pins on SDADCx channels inputs(3)	V_{SS} - 0.3	4.0	
	Input voltage on any other pin	V_{SS} - 0.3	4.0	
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$\lvert V_{REFSD-} - V_{SSx}\rvert$		-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 20: Current characteristics* for the maximum allowed injected current values.
3. VDDSD12 is the external power supply for PB2, PB10, and PE7 to PE15 I/O pins (I/O ground pin is internally connected to V_{SS}). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (I/O ground pin is internally connected to V_{SS}).

All main power (V_{DD}, V_{DDSD12}, V_{DDSD3} and V_{DDA}) and ground (V_{SS}, V_{SSSD}, and V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

The following relationship must be respected between V_{DDA} and V_{DD}: V_{DDA} must power on before or at the same time as V_{DD} in the power up sequence. V_{DDA} must be greater than or equal to V_{DD}.

The following relationship must be respected between V_{DDA} and V_{DDSD12}: V_{DDA} must power on before or at the same time as V_{DDSD12} or V_{DDSD3} in the power up sequence. V_{DDA} must be greater than or equal to V_{DDSD12} or V_{DDSD3}.

The following relationship must be respected between V_{DDSD12} and V_{DDSD3}: V_{DDSD3} must power on before or at the same time as V_{DDSD12} in the power up sequence.
After power up (V_{DDSD12} > Vrefint = 1.2 V) V_{DDSD3} can be higher or lower than V_{DDSD12}.

On-chip peripheral current consumption

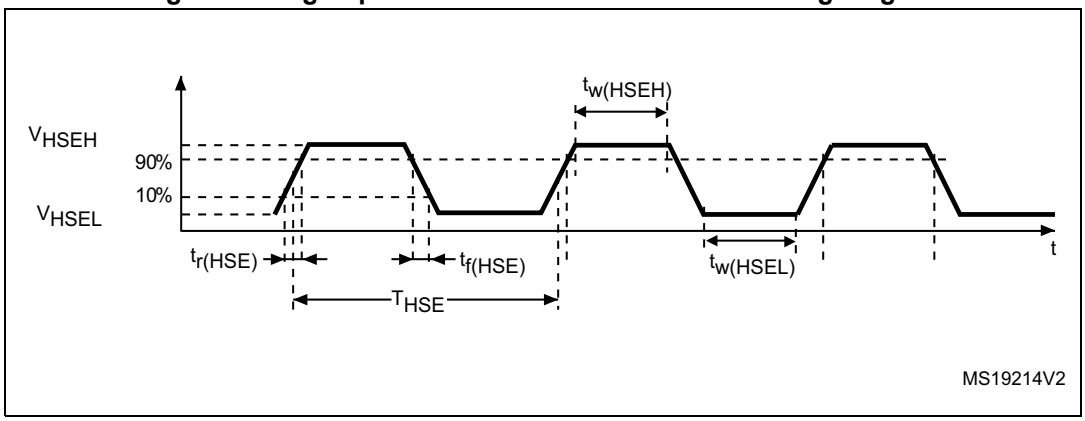
The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off;
  - with only one peripheral clocked on.
- Ambient operating temperature at 25°C and V_{DD} = V_{DDA}= 3.3 Volts.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
AHB peripherals		-
BusMatrix(2)	6.9	µA/MHz
DMA1	18.3	
DMA2	4.8	
CRC	2.6	
GPIOA	12.2	
GPIOB	11.9	
GPIOC	4.3	
GPIOD	12.0	
GPIOE	4.4	
GPIOF	3.7	
TSC	5.7	
APB2 peripherals		
APB2-Bridge(3)	4.2	
SYSCFG & COMP	2.8	
ADC1	17.7	
SPI1	12.3	
USART1	22.9	
TIM15	15.7	
TIM16	12.2	
TIM17	12.1	
TIM19	18.5	
SDAC1	10.8	
SDAC2	10.5	
SDAC3	10.3	

Figure 12. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 13*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter(1)	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	-	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	-	50	

1. Guaranteed by design.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 41*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

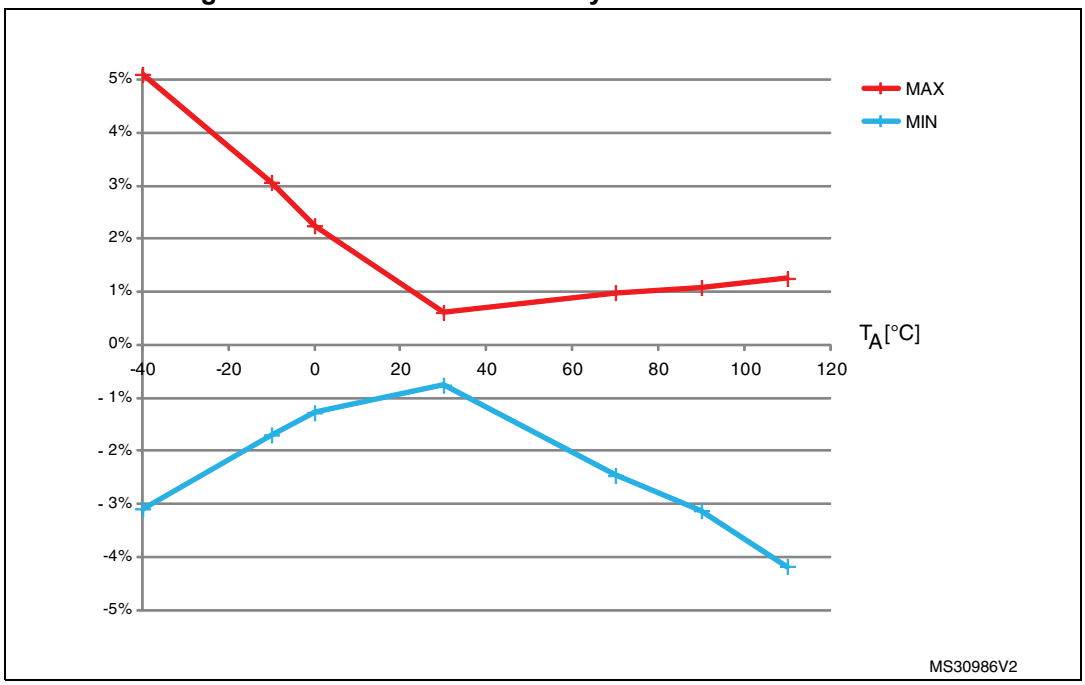
Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 10 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 01 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 10 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 01 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 16. HSI oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	60	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.

6.3.9 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22*.

Table 44. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	-	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
Jitter	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design.

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under the conditions summarized in *Table 22*. All I/Os are CMOS and TTL compliant.

Table 52. I/O static characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3V_{DD}+0.07^{(2)}$	V
		FT and FTf I/O	-	-	$0.475V_{DD}-0.2^{(2)}$	
		BOOT0	-	-	$0.3V_{DD}-0.3^{(2)}$	
		All I/Os except BOOT0 pin	-	-	$0.3V_{DD}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445V_{DD}+0.398^{(2)}$	-	-	
		FT and FTf I/O	$0.5V_{DD+0.2}{}^{(2)}$	-	-	
		BOOT0	$0.2V_{DD}+0.95^{(2)}$	-	-	
		All I/Os except BOOT0 pin	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	$200^{(2)}$	-	mV
		FT and FTf I/O	-	$100^{(2)}$	-	
		BOOT0	-	$300^{(2)}$	-	
I_{lkg}	Input leakage current (3)	TC, FT and FTf I/O TTa in digital mode $V_{SS} < V_{IN} < V_{DD}$	-	-	±0.1	µA
		TTa in digital mode $V_{DD} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	±0.2	
		FT and FTf I/O (3) $V_{DD} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	25	40	55	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

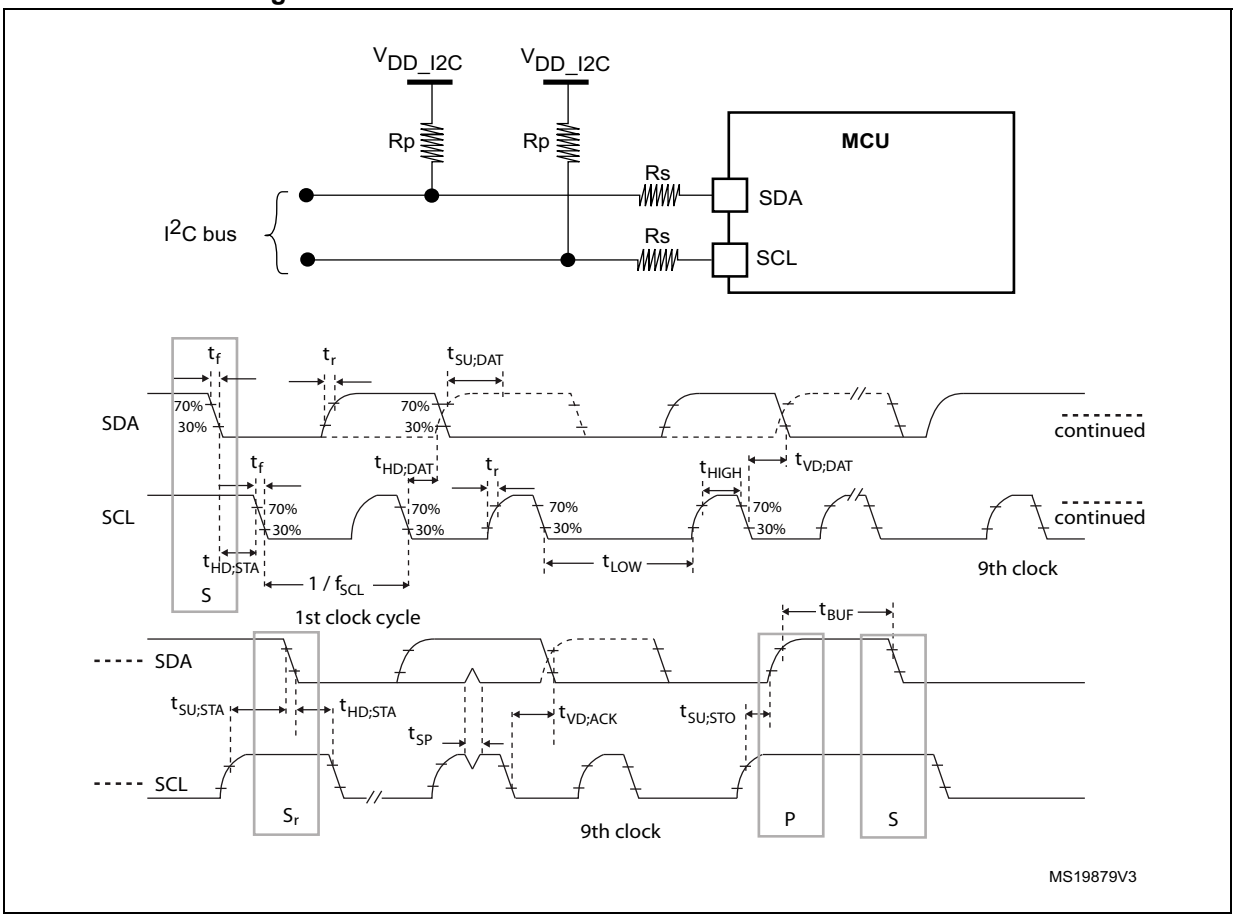
1. VDDSD12 is the external power supply for the PB2, PB10, and PE7 to PE15 I/O pins (the I/O pin ground is internally connected to VSS). VDDSD3 is the external power supply for PB14 to PB15 and PD8 to PD15 I/O pins (the I/O pin ground is internally connected to VSS). For those pins all V_{DD} supply references in this table are related to their given VDDSDx power supply.
2. Guaranteed by design.
3. Leakage could be higher than maximum value, if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Table 57. I²C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

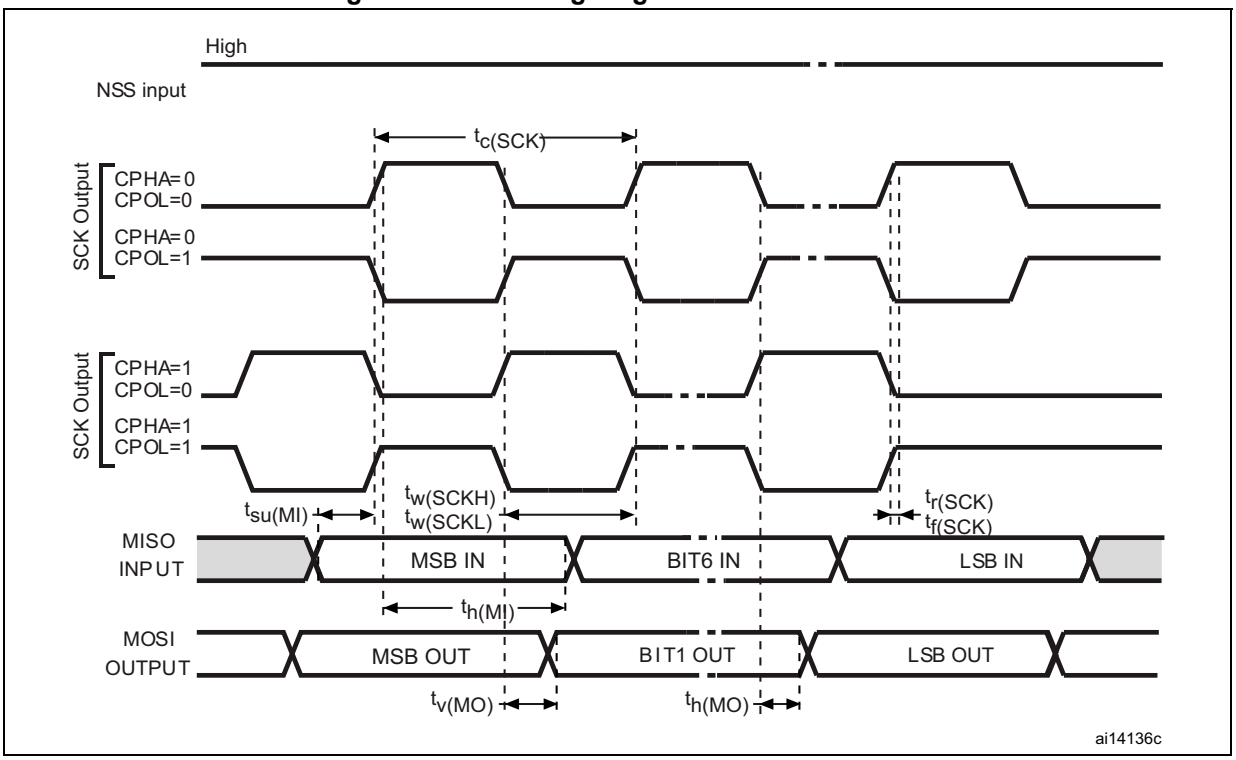
1. Guaranteed by design.
2. Spikes width below t_{AF}(min) are filtered.
3. Spikes width above t_{AF}(max) are not filtered.

Figure 21. I²C bus AC waveforms and measurement circuit



1. Legend: Rs: Series protection resistors. Rp: Pull-up resistors. V_{DD_I2C}: I2C bus supply.

Figure 24. SPI timing diagram - master mode(1)



1. Measurement points are done at $0.5V_{DD}$ level and with external C_L = 30 pF.

Table 59. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)(1)	I2S slave input clock duty cycle	Slave mode	30	70	%
f_{CK}(1) $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.528	1.539	MHz
		Slave mode	0	12.288	
$t_{r(CK)}$(1) $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	4	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	2	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	-	-	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$ (1)	I2S clock low time		312	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	3	-	
$t_{h(SD\_MR)}$(1)	Data input hold time	Master receiver	1.5	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$ (1)	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.

6.3.19 Comparator characteristics

Table 64. Comparator characteristics

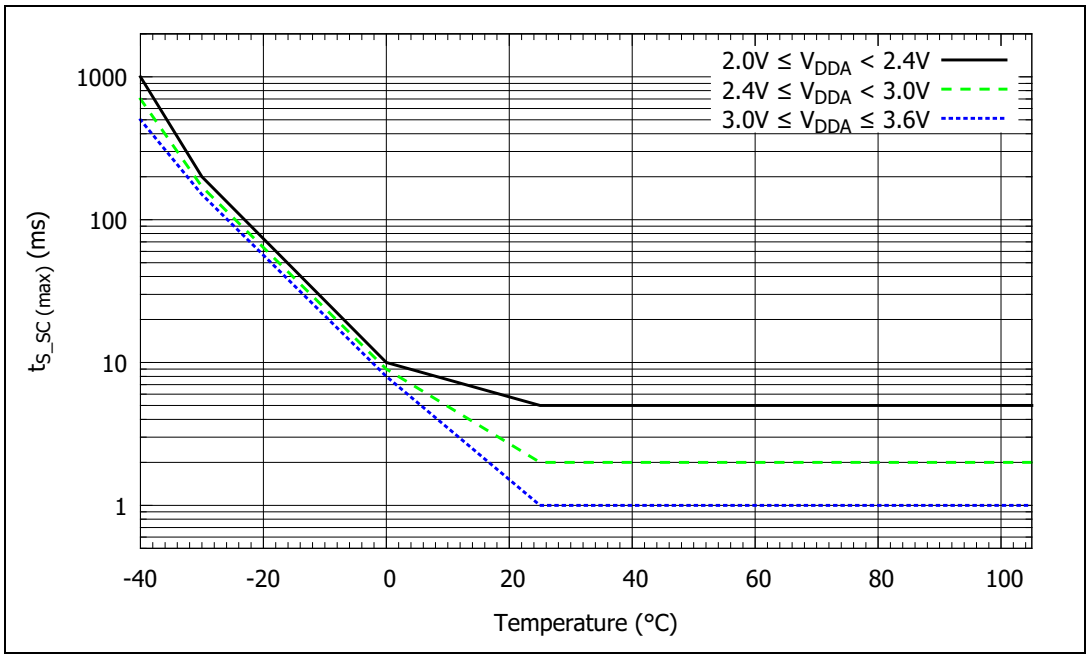
Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-		2	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}	V_{REFINT} scaler input voltage	-		-	1.2	-	V
V_{SC}	V_{REFINT} scaler offset voltage	-		-	±5	±10	mV
t_{S_SC}	Scaler startup time from power down	First V_{REFINT} scaler activation after device power on		-	-	1000(2)	ms
		Next activations				0.2	
t_{START}	Comparator startup time	Startup time to reach propagation delay specification		-	-	60	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode		-	2	4.5	µs
		Low power mode		-	0.7	1.5	
		Medium power mode		-	0.3	0.6	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	50	100	ns
			$V_{DDA} < 2.7$ V	-	100	240	
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode		-	2	7	µs
		Low power mode		-	0.7	2.1	
		Medium power mode		-	0.3	1.2	
		High speed mode	$V_{DDA} \geq 2.7$ V	-	90	180	ns
			$V_{DDA} < 2.7$ V	-	110	300	
V_{offset}	Comparator offset error	-		-	±4	±10	mV
dV_{offset}/dT	Offset error temperature coefficient	-		-	18	-	µV/°C
$I_{DD(COMP)}$	COMP current consumption	Ultra-low power mode		-	1.2	1.5	µA
		Low power mode		-	3	5	
		Medium power mode		-	10	15	
		High speed mode		-	75	100	

Table 64. Comparator characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)	-	-	0	-	mV
		Low hysteresis (COMPxHYST[1:0]=01)	High speed mode	3	8	13	
			All other power modes	5		10	
		Medium hysteresis (COMPxHYST[1:0]=10)	High speed mode	7	15	26	
			All other power modes	9		19	
		High hysteresis (COMPxHYST[1:0]=11)	High speed mode	18	31	49	
			All other power modes	19		40	

1. Guaranteed by design.
2. For more details and conditions see *Figure 30: Maximum VREFINT scaler startup time from power down*

Figure 30. Maximum V_{REFINT} scaler startup time from power down



6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers

Using the values obtained in *Table 81* T_{Jmax} is calculated as follows:

– For LQFP100, 46°C/W

T_{Jmax} = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

Figure 44. LQFP64 P_D max vs. T_A

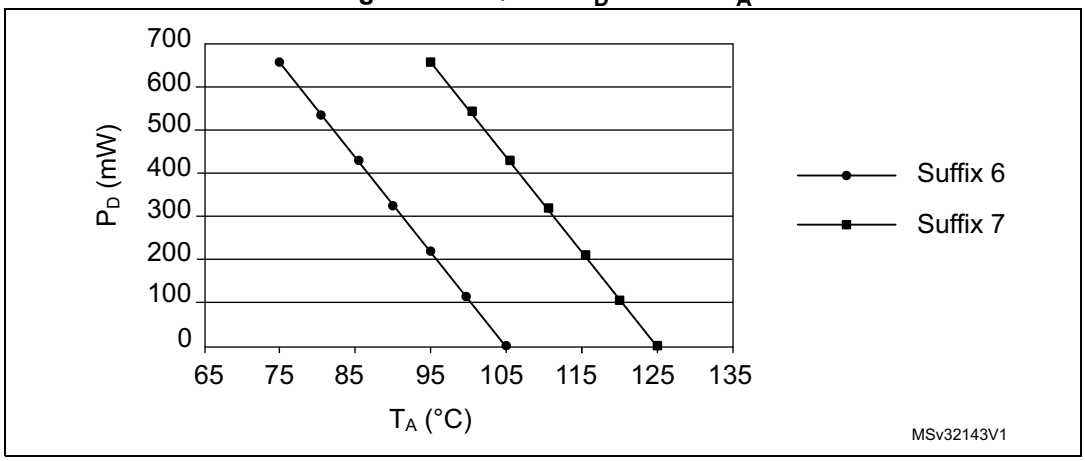


Table 83. Document revision history (continued)

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 28: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F373xx I2C implementation* Added *Table 8: STM32F373xx USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F373xx UFBGA100 ballout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F373xx pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F373xx pin definitions* Modified "x_CK" occurrences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Figure 9: Power supply scheme* Added Caution after *Figure 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.5.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*