Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373cct7

List of figures

Figure 1. Block diagram . . . 12
Figure 2. STM32F373xx LQFP48 pinout . . . 29
Figure 3. STM32F373xx LQFP64 pinout . . . 30
Figure 4. STM32F373xx LQFP100 pinout . . . 31
Figure 5. STM32F373xx UFBGA100 ballout . . . 32
Figure 6. STM32F373xx memory map . . . 48
Figure 7. Pin loading conditions . . . 52
Figure 8. Pin input voltage . . . 52
Figure 9. Power supply scheme . . . 53
Figure 10. Current consumption measurement scheme . . . 54
Figure 11. Typical V_{BAT} current consumption (LSE and RTC ON/LSEDRV[1:0]='00') . . . 65
Figure 12. High-speed external clock source AC timing diagram . . . 73
Figure 13. Low-speed external clock source AC timing diagram . . . 74
Figure 14. Typical application with an 8 MHz crystal . . . 75
Figure 15. Typical application with a 32.768 kHz crystal . . . 77
Figure 16. HSI oscillator accuracy characterization results . . . 78
Figure 17. TC and TTa I/O input characteristics - CMOS port . . . 85
Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port . . . 86
Figure 19. I/O AC characteristics definition . . . 89
Figure 20. Recommended NRST pin protection . . . 90
Figure 21. I^2C bus AC waveforms and measurement circuit . . . 92
Figure 22. SPI timing diagram - slave mode and CPHA = 0 . . . 94
Figure 23. SPI timing diagram - slave mode and CPHA = 1(1) . . . 94
Figure 24. SPI timing diagram - master mode(1) . . . 95
Figure 25. I^2S slave timing diagram (Philips protocol)(1) . . . 97
Figure 26. I^2S master timing diagram (Philips protocol)(1) . . . 97
Figure 27. ADC accuracy characteristics . . . 100
Figure 28. Typical connection diagram using the ADC . . . 100
Figure 29. 12-bit buffered /non-buffered DAC . . . 102
Figure 30. Maximum V_{REFINT} scaler startup time from power down . . . 104
Figure 31. USB timings: definition of data signal rise and fall time . . . 108
Figure 32. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline . . . 115
Figure 33. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint . . . 116
Figure 34. UFBGA100 marking example (package top view) . . . 117
Figure 35. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline . . . 118
Figure 36. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint . . . 120
Figure 37. LQFP100 marking example (package top view) . . . 120
Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline . . . 121
Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint . . . 123
Figure 40. LQFP64 marking example (package top view) . . . 123
Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline . . . 124
Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint . . . 126
Figure 43. LQFP48 marking example (package top view) . . . 126

3.17 Timers and watchdogs

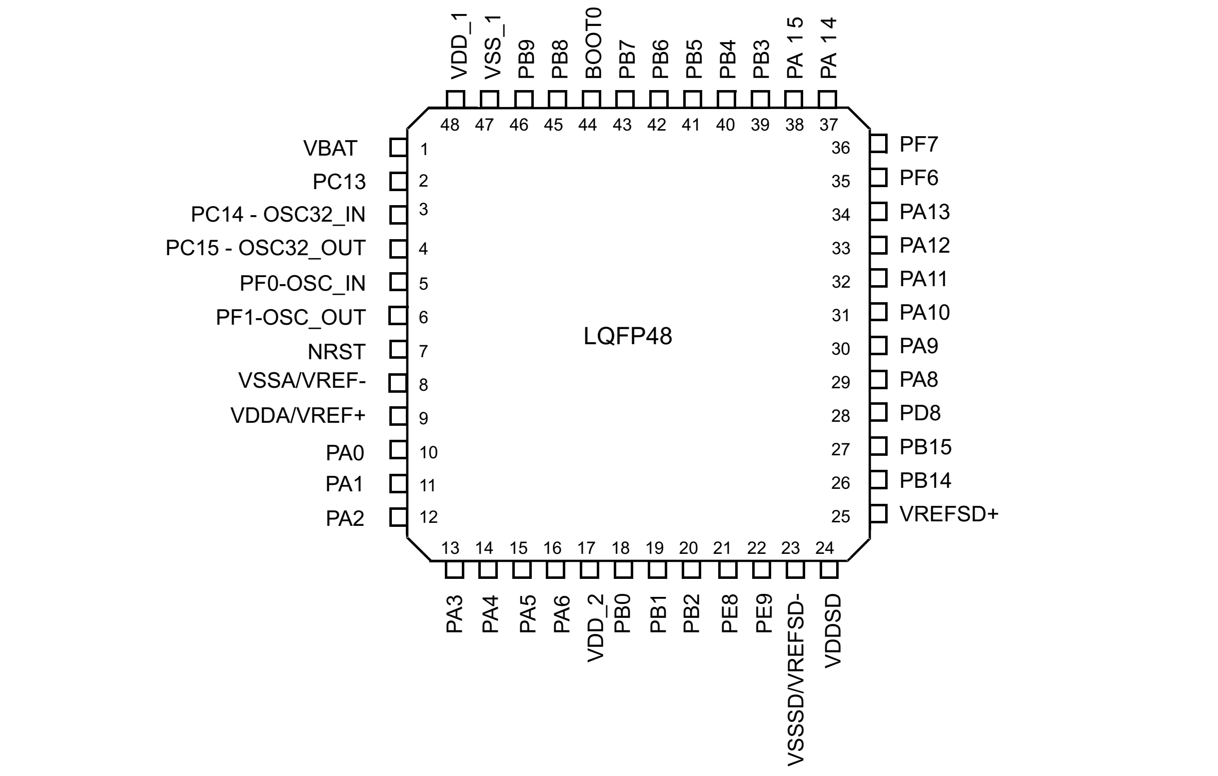
The STM32F373xx includes two 32-bit and nine 16-bit general-purpose timers, three basic timers, two watchdog timers and a SysTick timer. The table below compares the features of the advanced control, general purpose and basic timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary outputs
General-purpose	TIM2 TIM5	32-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM3, TIM4, TIM19	16-bit	Up, Down, Up/Down	Any integer between 1 and 65536	Yes	4	0
General-purpose	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	0
General-purpose	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
General-purpose	TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	0
General-purpose	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6, TIM7, TIM18	16-bit	Up	Any integer between 1 and 65536	Yes	0	0

4 Pinouts and pin description

Figure 2. STM32F373xx LQFP48 pinout



1. The above figure shows the package top view.

Figure 4. STM32F373xx LQFP100 pinout

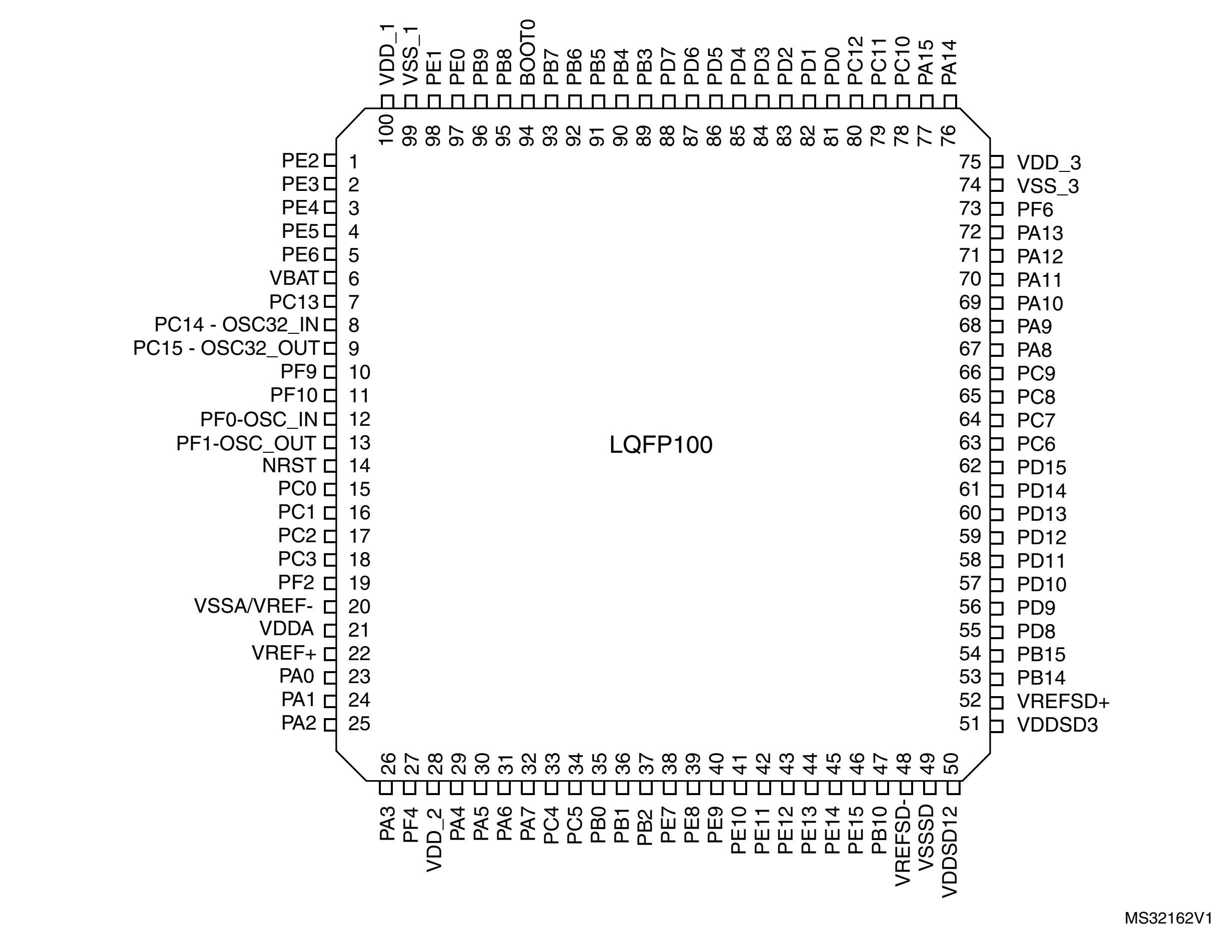


Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
51	L12	-	-	VDDSD3	S	-	(2)	SDADC3 power supply	
52	K12	33	25	VREFSD+	S	-	-	External reference voltage for SDADC1, SDADC2, SDADC3 (positive input)	
53	K11	34	26	PB14	I/O	TC	(4)	SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1	SDADC3_AIN8P
54	K10	35	27	PB15	I/O	TC	(4)	SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN	SDADC3_AIN7P, SDADC3_AIN8M
55	K9	36	28	PD8	I/O	TC	(4)	SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3	SDADC3_AIN6P
56	K8	-	-	PD9	I/O	TC	(4) (2)	USART3_RX, TSC_G6_IO4	SDADC3_AIN5P, SDADC3_AIN6M
57	J12	-	-	PD10	I/O	TC	(4) (2)	USART3_CK	SDADC3_AIN4P
58	J11	-	-	PD11	I/O	TC	(4) (2)	USART3_CTS	SDADC3_AIN3P, SDADC3_AIN4M
59	J10	-	-	PD12	I/O	TC	(4) (2)	USART3_RTS, TIM4_CH1, TSC_G8_IO1	SDADC3_AIN2P
60	H12	-	-	PD13	I/O	TC	(4) (2)	TIM4_CH2, TSC_G8_IO2	SDADC3_AIN1P, SDADC3_AIN2M
61	H11	-	-	PD14	I/O	TC	(4) (2)	TIM4_CH3, TSC_G8_IO3	SDADC3_AIN0P
62	H10	-	-	PD15	I/O	TC	(4) (2)	TIM4_CH4, TSC_G8_IO4	SDADC3_AIN0M
63	E12	37	-	PC6	I/O	FT	(2)	TIM3_CH1, SPI1_NSS/I2S1_WS	-
64	E11	38	-	PC7	I/O	FT	(2)	TIM3_CH2, SPI1_SCK/I2S1_CK,	-
65	E10	39	-	PC8	I/O	FT	(2)	SPI1_MISO/I2S1_MCK, TIM3_CH3	-
66	D12	40	-	PC9	I/O	FT	(2)	SPI1_MOSI/I2S1_SD, TIM3_CH4	-

Table 13. Alternate functions for port PB

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF15
PB0	-	-	TIM3_CH3	TSC_ G3_IO3	-	SPI_MOSI/ I2S1_SD	-	-	-	-	TIM3_ CH2	-	EVENTOUT
PB1	-	-	TIM3_CH4	TSC_ G3_IO4	-	-	-	-	-	-	-	-	EVENTOUT
PB2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
PB3	JTDO- TRACESWO	TIM2_ CH2	TIM4_ETR	TSC_ G5_IO1	-	SPI1_SCK/ I2S1_CK	SPI3_SCK/ I2S3_CK	USART2_TX	-	TIM13_ CH1	TIM3_ ETR	-	EVENTOUT
PB4	NJTRST	TIM16_ CH1	TIM3_CH1	TSC_ G5_IO2	-	SPI1_MISO /I2S1_MCK	SPI3_MISO/ I2S3_MCK	USART2_RX	-	TIM15_ CH1N	TIM17 _BKIN	-	EVENTOUT
PB5	-	TIM16_ BKIN	TIM3_CH2	-	I2C1_ SMBA	SPI1_MOSI /I2S1_SD	SPI3_MOSI /I2S3_SD	USART2_CK	-	-	TIM17 _CH1	TIM19 _ETR	EVENTOUT
PB6	-	TIM16_ CH1N	TIM4_CH1	TSC_ G5_IO3	I2C1_ SCL	-	-	USART1_TX	-	TIM15_ CH1	TIM3_ CH3	TIM19 _CH1	EVENTOUT
PB7	-	TIM17_ CH1N	TIM4_CH2	TSC_ G5_IO4	I2C1_ SDA	-	-	USART1_RX	-	TIM15_ CH2	TIM3_ CH4	TIM19 _CH2	EVENTOUT
PB8	-	TIM16_ CH1	TIM4_CH3	TSC_ SYNC	I2C1_ SCL	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	COMP1 _OUT	CAN_ RX	-	TIM19 _CH3	EVENTOUT
PB9	-	TIM17_ CH1	TIM4_CH4	-	I2C1_ SDA	SPI2_NSS/ I2S2_WS	IR-OUT	USART3_RX	COMP2 _OUT	CAN_ TX	-	TIM19 _CH4	EVENTOUT
PB10	-	TIM2_ CH3	-	TSC_ SYNCH	-	SPI2_SCK/ I2S2_CK	CEC	USART3_TX	-	-	-	-	EVENTOUT
PB14	-	TIM15_ CH1	-	TSC_ G6_IO1	-	SPI2_MISO /I2S2_MCK	-	USART3_RTS	-	TIM12_ CH1	-	-	EVENTOUT
PB15	RTC_REFIN	TIM15_ CH2	TIM15_ CH1N	TSC_ G6_IO2	-	SPI2_MOSI /I2S2_SD	-	-	-	TIM12_ CH2	-	-	EVENTOUT

Table 31. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter	Conditions		Typ@V_{DD} (V_{DD}=V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} and V_{DDSD12}	Regulator in run mode, all oscillators OFF	1.99	2.07	2.19	2.33	2.46	2.64	10.8	11.8	12.4	µA
			Regulator in low-power mode, all oscillators OFF	1.99	2.07	2.18	2.32	2.47	2.63	10.6	11.5	12.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.44	2.53	2.7	2.89	3.09	3.33	-	-	-	
			LSI OFF and IWDG OFF	1.87	1.94	2.06	2.19	2.35	2.51	4.1	4.5	4.8	
IDDAmon	Supply current for V_{DDA} and V_{DDSD12} monitoring	-		0.95	1.02	1.12	1.2	1.27	1.4	-	-	-	

1. Data based on characterization results and tested in production.
2. To obtain data with monitoring OFF is necessary to substract the IDDAmon current.

Table 32. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}							Max(2)			Unit
			= 1.65 V	= 1.8 V	= 2.0 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode" lower driving capability; LSEDRV[1:0] = '00'	0.50	0.52	0.55	0.63	0.70	0.87	0.95	1.1	1.6	2.2	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.85	0.90	0.93	1.02	1.10	1.27	1.38	1.6	2.4	3.0	

1. Crystal used: Abracon ABS07-120-32.768kHz-T with 6 pF of CL for typical values.
2. Guaranteed by characterization results.

Table 33. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	61.4	28.8	mA
			64 MHz	55.4	25.9	
			48 MHz	42.3	20.0	
			32 MHz	28.7	13.8	
			24 MHz	21.9	10.7	
			16 MHz	14.8	7.4	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	7.8	4.1	
			4 MHz	4.6	2.6	
			2 MHz	2.9	1.8	
			1 MHz	2.0	1.3	
			500 kHz	1.5	1.1	
			125 kHz	1.2	1.0	
I_{DDA}(1)(2)	Supply current in Run mode from V_{DDA} supply	Running from HSE crystal clock 8 MHz, code executing from Flash, PLL on	72 MHz	243.3	242.4	µA
			64 MHz	214.3	213.3	
			48 MHz	159.3	158.3	
			32 MHz	107.7	107.3	
			24 MHz	82.8	82.6	
			16 MHz	58.4	58.2	
		Running from HSE crystal clock 8 MHz, code executing from Flash, PLL off	8 MHz	1.2	1.2	
			4 MHz	1.2	1.2	
			2 MHz	1.2	1.2	
			1 MHz	1.2	1.2	
			500 kHz	1.2	1.2	
			125 kHz	1.2	1.2	
$I_{SDADC12}$ + I_{SDADC3}	Supply currents in Run mode from V_{DDSD12} and V_{DDSD3} (SDADCs are off)	-	-	2.5	1	µA

1. V_{DDA} monitoring is off, V_{DDSD12} monitoring is off.
2. When peripherals are enabled, power consumption of the analog part of peripherals such as ADC, DACs, Comparators, etc. is not included. Refer to those peripherals characteristics in the subsequent sections.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 52: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC and SDADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode. Under reset conditions all I/Os are configured in input floating mode - so if some inputs do not have a defined voltage level then they can generate additional consumption. This consumption is visible on V_{DD} supply and also on V_{DDSDx} supply because some I/Os are powered from SDADCx supply (all I/Os which have SDADC analog input functionality).

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
- C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

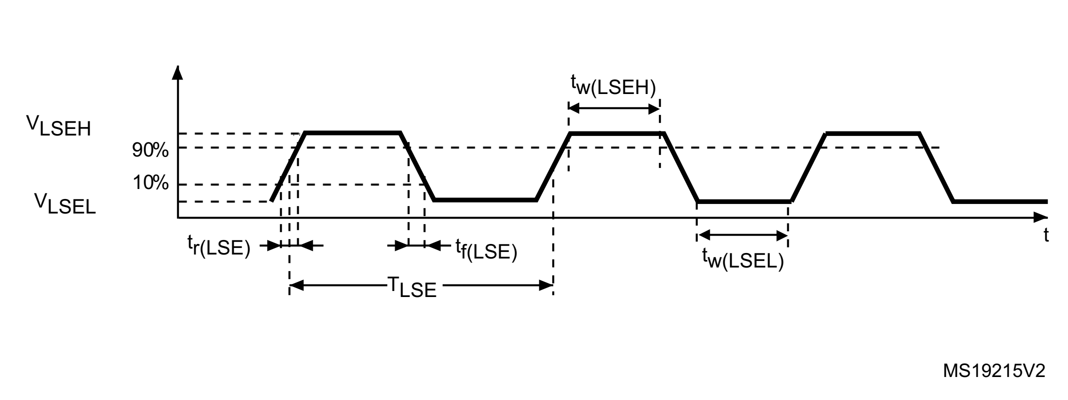
The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off;
  - with only one peripheral clocked on.
- Ambient operating temperature at 25°C and V_{DD} = V_{DDA}= 3.3 Volts.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
AHB peripherals		-
BusMatrix(2)	6.9	µA/MHz
DMA1	18.3	
DMA2	4.8	
CRC	2.6	
GPIOA	12.2	
GPIOB	11.9	
GPIOC	4.3	
GPIOD	12.0	
GPIOE	4.4	
GPIOF	3.7	
TSC	5.7	
APB2 peripherals		
APB2-Bridge(3)	4.2	
SYSCFG & COMP	2.8	
ADC1	17.7	
SPI1	12.3	
USART1	22.9	
TIM15	15.7	
TIM16	12.2	
TIM17	12.1	
TIM19	18.5	
SDAC1	10.8	
SDAC2	10.5	
SDAC3	10.3	

Figure 13. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. HSE oscillator characteristics

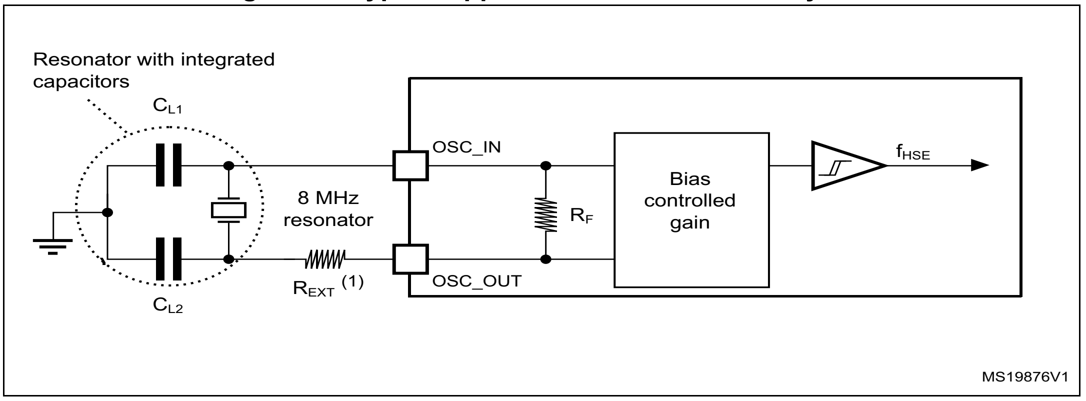
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup(3)	-	-	8.5	mA
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 3.3 V, Rm= 45 Ω, CL= 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL=5 pF@32 MHz	-	0.8	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 10 pF@32 MHz	-	1	-	
		V_{DD} = 3.3 V, Rm= 30 Ω, CL= 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 14*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 14. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 45. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (2 kB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design.

Table 46. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

Table 59. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$DuCy(SCK)$ (1)	I2S slave input clock duty cycle	Slave mode	30	70	%
f_{CK} (1) $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.528	1.539	MHz
		Slave mode	0	12.288	
$t_{r(CK)}$ (1) $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	4	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	2	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	-	-	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$ (1)	I2S clock low time		312	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	3	-	
$t_{h(SD\_MR)}$ (1)	Data input hold time	Master receiver	1.5	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$ (1)	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 60* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 22*.

Note: It is recommended to perform a calibration after each power-up.

Table 60. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	0	-	-	V
$I_{DDA(ADC)}$(1)	Current consumption from V_{DDA}	$V_{DD} = V_{DDA} = 3.3$ V	-	0.9	-	mA
I_{VREF}	Current on the V_{REF} input pin	-	-	160(2)	220(2)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(3)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{SRC}(3)	Signal source impedance	See *Equation 1* and *Table 61* for details	-	-	50	kΩ
R_{ADC}(3)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(3)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_{latr}(3)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(3)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(3)	Power-up time	-	-	-	1	µs
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1	-	18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} is present
2. Guaranteed by characterization results.
3. Guaranteed by design.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 60*

2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.14 does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Guaranteed by characterization results.

Figure 27. ADC accuracy characteristics

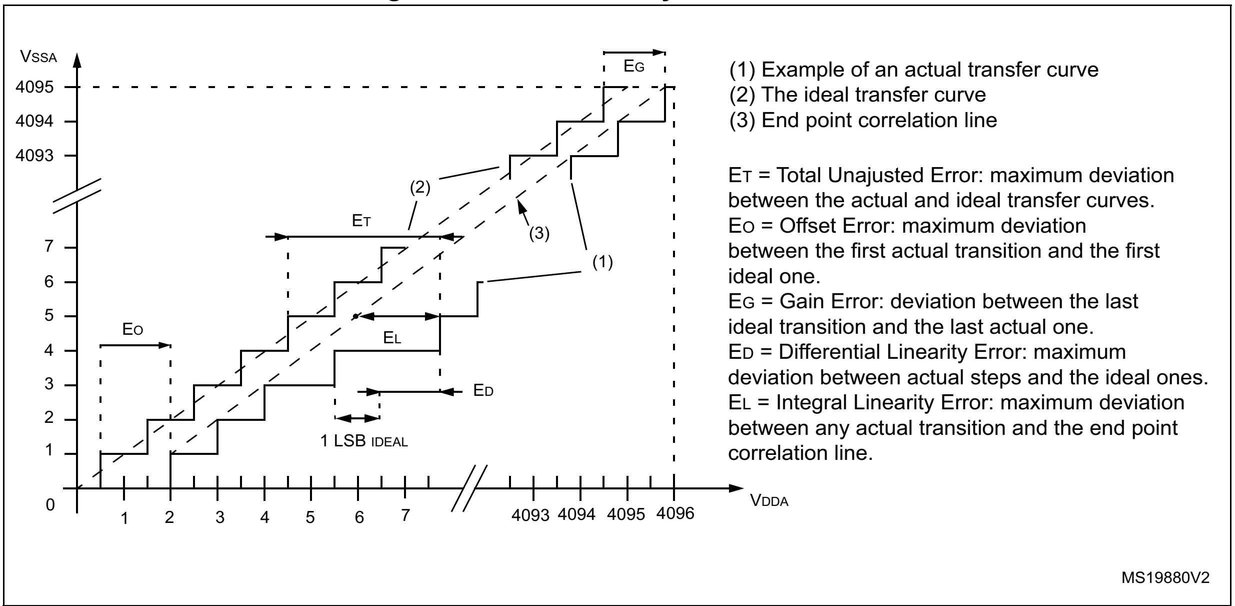
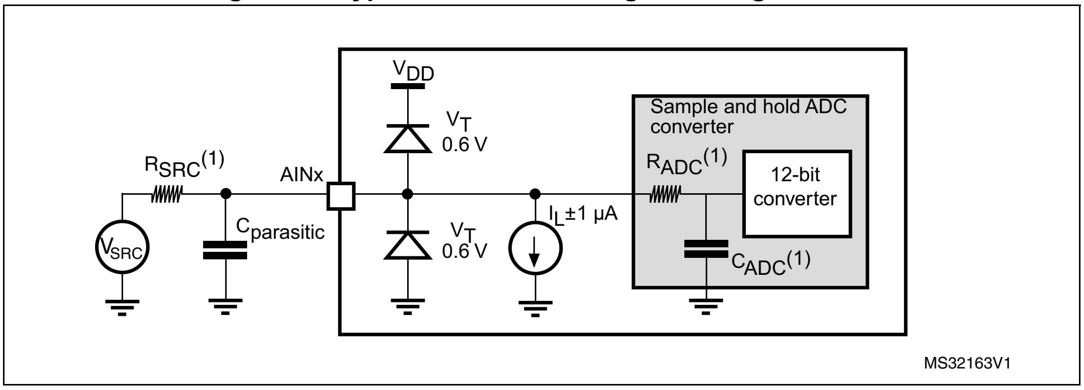


Figure 28. Typical connection diagram using the ADC



1. Refer to Table 60 for the values of R_{SRC}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

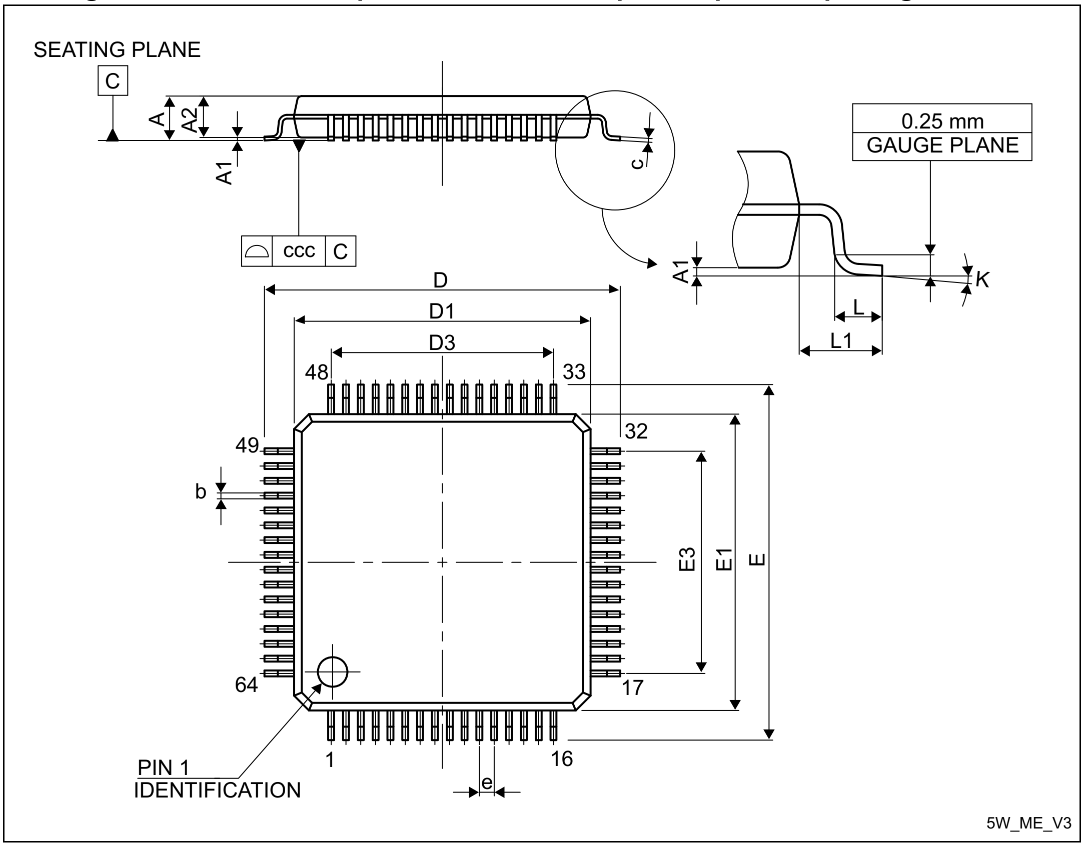
Power supply decoupling should be performed as shown in Figure 9. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 74. SDADC characteristics (continued)[1]

Symbol	Parameter	Conditions					Min	Typ	Max	Unit	Note
SINAD[5]	Signal to noise and distortion ratio	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3[3]	76	77	-	dB	ENOB = SINAD/ 6.02 - 0.292
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	75	76	-		
						V_{REFSD+} = 3.3	76	77	-		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	70	74	-		
						V_{REFSD+} = 3.3	79	85	-		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3[3]	75	81	-		
		Single ended mode	gain =1	f_{ADC} = 1.5MHz		V_{REFSD+} = 3.3	72	73	-		
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	68	71	-		
						V_{REFSD+} = 3.3	72	73	-		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	60	64	-		
						V_{REF} = 3.3	67	72	-		
THD[5]	Total harmonic distortion	Differential mode	gain =1	f_{ADC} = 1.5 MHz	V_{DDSDx} = 3.3	V_{REFSD+} = 3.3[3]	-	-77	-76	dB	-
				f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	-	-77	-76		
						V_{REFSD+} = 3.3	-	-77	-76		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	-	-85	-70		
						V_{REFSD+} = 3.3	-	-93	-80		
				f_{ADC} = 1.5 MHz		V_{REFSD+} = 3.3[3]	-	-93	-83		
		Single ended mode	gain =1	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	-	-72	-68		
						V_{REFSD+} = 3.3	-	-74	-72		
			gain =8	f_{ADC} = 6 MHz		V_{REFSD+} = 1.2[4]	-	-66	-61		
						V_{REFSD+} = 3.3	-	-75	-70		

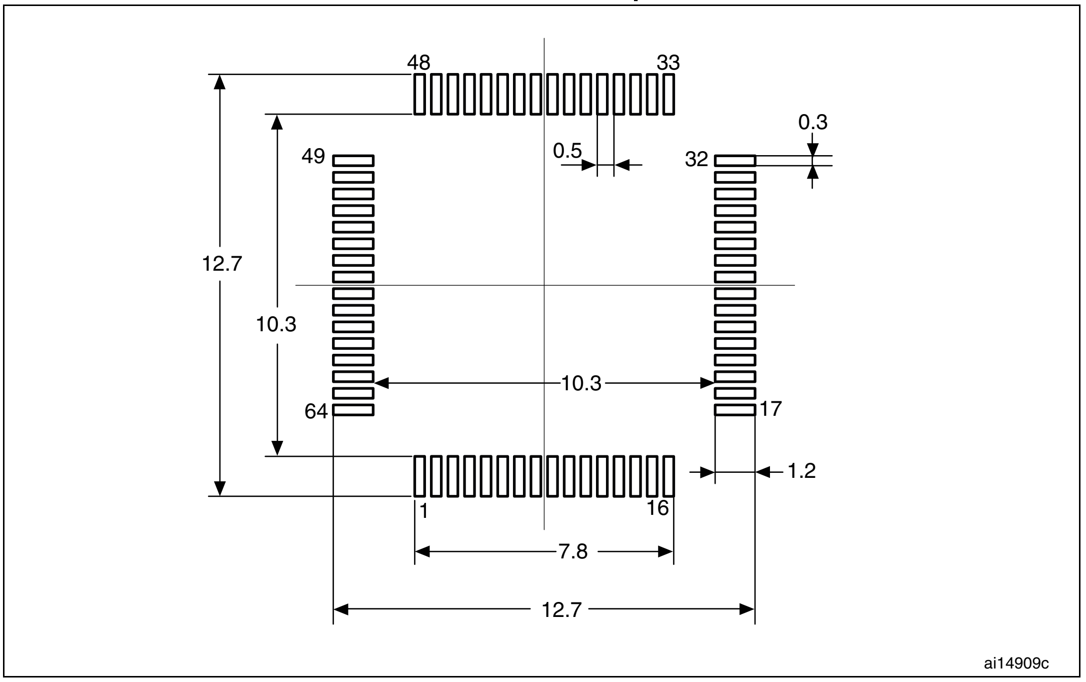
7.3 LQFP64 package information

Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Figure 39. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

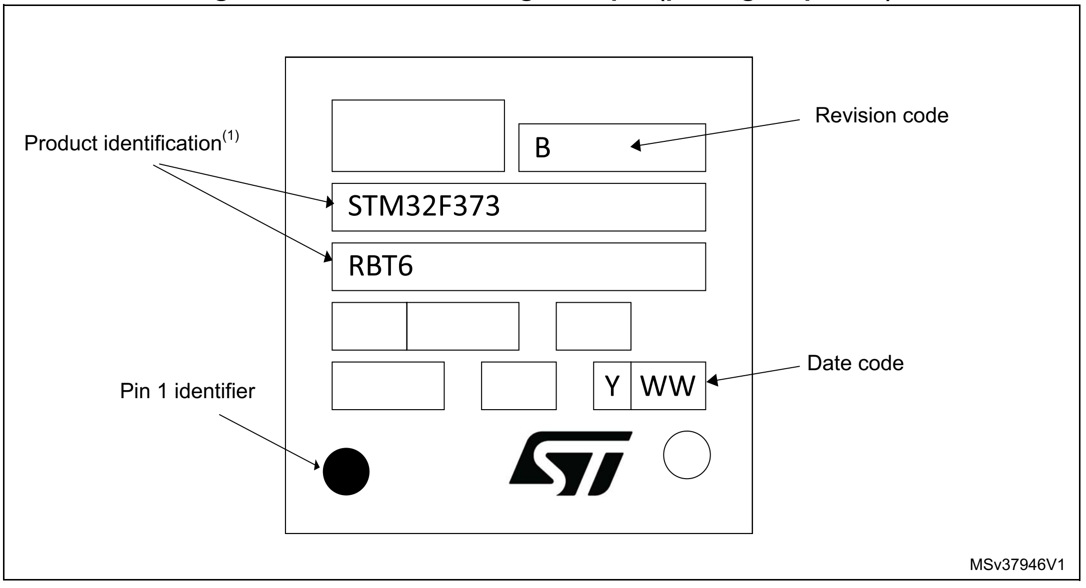


1. Dimensions are expressed in millimeters.

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 40. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 83. Document revision history (continued)

Date	Revision	Changes
18-Mar-2014	5	Renamed part number STM32F37x to STM32F373xx Added note1 in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V* Updated *Chapter 3.14: Digital-to-analog converter (DAC)* Updated, added note 2 and 3 in *Table 57: I2C analog filter characteristics* Renamed t_{SP} symbol with t_{AF}. Added note for EG Symbol in *Table 74: SDADC characteristics* Added all packages top view
21-Jul-2015	6	Updated *Section 7* Updated *Section 3.13* Updated *Section 3.7.1*, *Section 3.7.4* Updated *Table 11: STM32F373xx pin definitions*, *Table 19: Voltage characteristics*, *Table 49: ESD absolute maximum ratings*, *Table 74: SDADC characteristics*, *Table 76: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, and *Table 78: LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data* Updated *Figure 2: STM32F373xx LQFP48 pinout*, *Figure 9: Power supply scheme*, *Figure 32: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline*, *Figure 34: UFBGA100 marking example (package top view)*, *Figure 36: LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint*, *Figure 37: LQFP100 marking example (package top view)*, *Figure 38: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*, *Figure 39: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*, *Figure 40: LQFP64 marking example (package top view)*, *Figure 42: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint*, *Figure 43: LQFP48 marking example (package top view)*. Added *Table 32: Typical and maximum current consumption from VBAT supply*, *Table 49: ESD absolute maximum ratings*, *Table 64: Comparator characteristics*, *Table 77: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)*. Added *Figure 11: Typical VBAT current consumption (LSE and RTC ON/LSEDRV[1:0]='00')*, *Figure 30: Maximum VREFINT scaler startup time from power down*, *Figure 33: UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*.