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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 1x12b, 3x16b; D/A 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373r8t6tr

3 Functional overview

3.1 ARM® Cortex®-M4 core with embedded Flash and SRAM

The ARM Cortex-M4 processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU speeds up software development by using metalanguage development tools, while avoiding saturation.

With its embedded ARM core, the STM32F373xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F373xx family.

3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultralow power consumption with integrated sleep modes
- Platform security robustness with optional integrated memory protection unit (MPU).

With its embedded ARM core, the STM32F373xx devices are compatible with all ARM development tools and software.

Table 3. Capacitive sensing GPIOs available on STM32F373xx devices (continued)

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
3	TSC_G3_IO1	PC4	7	TSC_G7_IO1	PE2
	TSC_G3_IO2	PC5		TSC_G7_IO2	PE3
	TSC_G3_IO3	PB0		TSC_G7_IO3	PE4
	TSC_G3_IO4	PB1		TSC_G7_IO4	PE5
4	TSC_G4_IO1	PA9	8	TSC_G8_IO1	PD12
	TSC_G4_IO2	PA10		TSC_G8_IO2	PD13
	TSC_G4_IO3	PA13		TSC_G8_IO3	PD14
	TSC_G4_IO4	PA14		TSC_G8_IO4	PD15

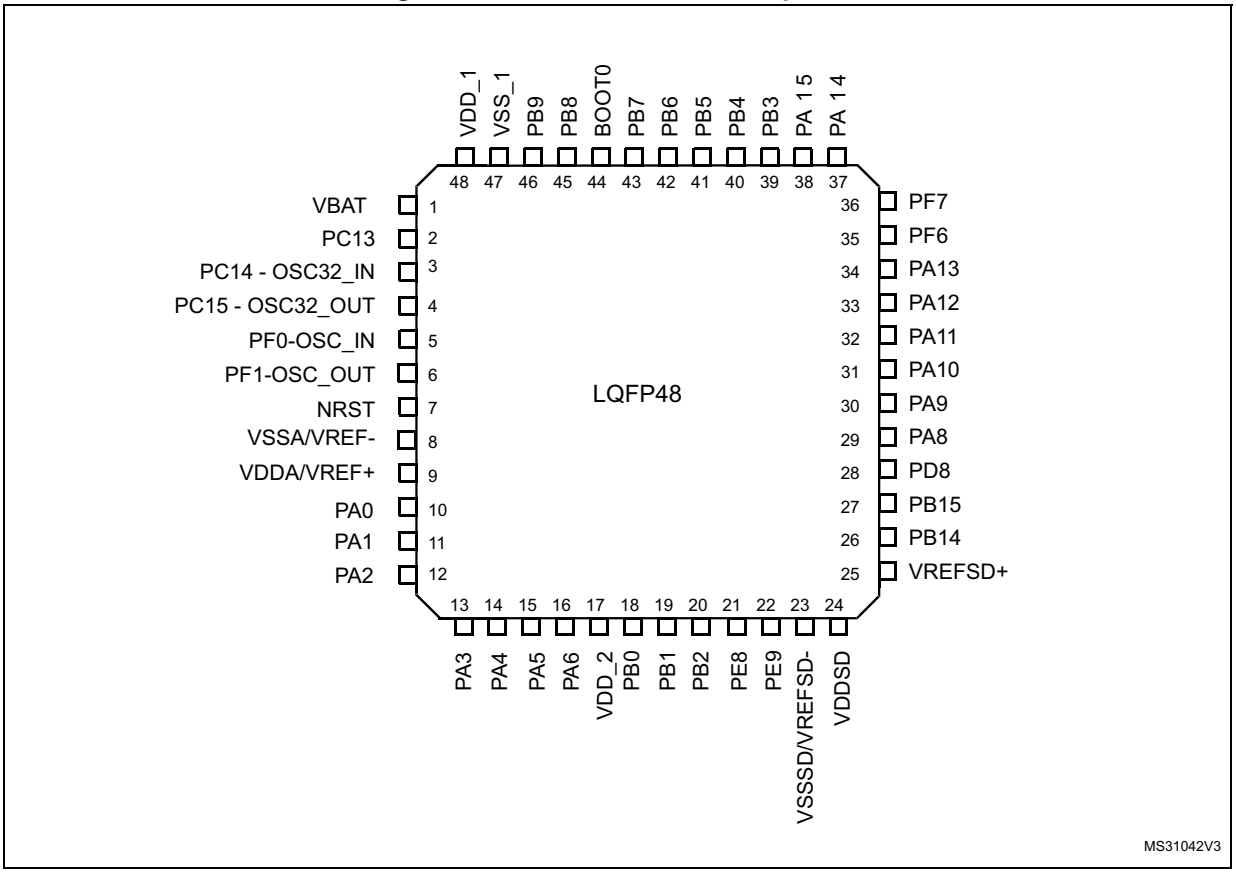
1. This GPIO offers a reduced touch sensing sensitivity. It is thus recommended to use it as sampling capacitor I/O.

Table 4. No. of capacitive sensing channels available on STM32F373xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F373Cx	STM32F373Rx	STM32F373Vx
G1	3	3	3
G2	2	3	3
G3	1	3	3
G4	3	3	3
G5	3	3	3
G6	2	2	3
G7	0	0	3
G8	0	0	3
Number of capacitive sensing channels	14	17	24

4 Pinouts and pin description

Figure 2. STM32F373xx LQFP48 pinout



1. The above figure shows the package top view.

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
38	M7	-	-	PE7	I/O	TC	(3) (2)	-	SDADC1_AIN3P, SDADC1_AIN4M, SDADC2_AIN5P, SDADC2_AIN6M
39	L7	29	21	PE8	I/O	TC	(3)	-	SDADC1_AIN8P, SDADC2_AIN8P
40	M8	30	22	PE9	I/O	TC	(3)	-	SDADC1_AIN7P, SDADC1_AIN8M, SDADC2_AIN7P, SDADC2_AIN8M
41	L8	-	-	PE10	I/O	TC	(3) (2)	-	SDADC1_AIN2P
42	M9	-	-	PE11	I/O	TC	(3) (2)	-	SDADC1_AIN1P, SDADC1_AIN2M, SDADC2_AIN4P
43	L9	-	-	PE12	I/O	TC	(3) (2)	-	SDADC1_AIN0P, SDADC2_AIN3P, SDADC2_AIN4M
44	M10	-	-	PE13	I/O	TC	(3) (2)	-	SDADC1_AIN0M , SDADC2_AIN2P
45	M11	-	-	PE14	I/O	TC	(3) (2)	-	SDADC2_AIN1P, SDADC2_AIN2M
46	M12	-	-	PE15	I/O	TC	(3) (2)	USART3_RX	SDADC2_AIN0P
47	L10	-	-	PB10	I/O	TC	(3) (2)	SPI2_SCK/I2S2_CK, USART3_TX, CEC, TSC_SYNC, TIM2_CH3	SDADC2_AIN0M
48	L11	-	-	VREFSD-	S	-	(2)	External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
49	F12	-	-	VSSSD	S	-	(2)	SDADC1, SDADC2, SDADC3 ground	
-	-	31	23	VSSSD/ VREFSD-	S	-	-	SDADC1, SDADC2, SDADC3 ground / External reference voltage for SDADC1, SDADC2, SDADC3 (negative input), negative SDADC analog input in SDADC single ended mode	
50	G12	-	-	VDDSD12	S	-	(2)	SDADC1 and SDADC2 power supply	
-	-	32	24	VDDSD	S	-	-	SDADC1, SDADC2, SDADC3 power supply	

Table 11. STM32F373xx pin definitions (continued)

Pin numbers				Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP100	UFBGA100	LQFP64	LQFP48					Alternate function	Additional functions
91	C5	57	41	PB5	I/O	FT	-	SPI1_MOSI/I2S1_SD, SPI3_MOSI/I2S3_SD, I2C1_SMBAI, USART2_CK, TIM16_BKIN, TIM3_CH2, TIM17_CH1, TIM19_ETR	-
92	B5	58	42	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TIM3_CH3, TIM4_CH1, TIM19_CH1, TIM15_CH1, TSC_G5_IO3	-
93	B4	59	43	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TIM3_CH4, TIM4_CH2, TIM19_CH2, TIM15_CH2, TSC_G5_IO4	-
94	A4	60	44	BOOT0	I	B	-	Boot memory selection	
95	A3	61	45	PB8	I/O	FTf	-	SPI2_SCK/I2S2_CK, I2C1_SCL, USART3_TX, CAN_RX, CEC, TIM16_CH1, TIM4_CH3, TIM19_CH3, COMP1_OUT, TSC_SYNC	-
96	B3	62	46	PB9	I/O	FTf	-	SPI2_NSS/I2S2_WS, I2C1_SDA, USART3_RX, CAN_TX, IR_OUT, TIM17_CH1, TIM4_CH4, TIM19_CH4, COMP2_OUT	-
97	C3	-	-	PE0	I/O	FT	(2)	USART1_TX, TIM4_ETR	-
98	A2	-	-	PE1	I/O	FT	(2)	USART1_RX	-
99	D3	63	47	VSS_1	S	-	-	Ground	
100	C4	64	48	VDD_1	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch sinks only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED)
   After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the RM0313 reference manual.
2. When using the small packages (48 and 64 pin packages), the GPIO pins which are not present on these packages, must not be configured in analog mode.
3. these pins are powered by VDDSD12.
4. these pins are powered by VDDSD3.

Table 14. Alternate functions for port PC

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0	-	EVENTOUT	TIM5_CH1_ETR	-	-	-	-	-
PC1	-	EVENTOUT	TIM5_CH2	-	-	-	-	-
PC2	-	EVENTOUT	TIM5_CH3	-	-	SPI2_MISO/I2S2_MCK	-	-
PC3	-	EVENTOUT	TIM5_CH4	-	-	SPI2_MOSI/I2S2_SD	-	-
PC4	-	EVENTOUT	TIM13_CH1	TSC_G3_IO1	-	-	-	USART1_TX
PC5	-	EVENTOUT	-	TSC_G3_IO2	-	-	-	USART1_RX
PC6	-	EVENTOUT	TIM3_CH1	-	-	SPI1_NSS/I2S1_WS	-	-
PC7	-	EVENTOUT	TIM3_CH2	-	-	SPI1_SCK/I2S1_CK	-	-
PC8	-	EVENTOUT	TIM3_CH3	-	-	SPI1_MISO/I2S1_MCK	-	-
PC9	-	EVENTOUT	TIM3_CH4	-	-	SPI1_MOSI/I2S1_SD	-	-
PC10	-	EVENTOUT	TIM19_CH1	-	-	-	SPI3_SCK/I2S3_CK	USART3_TX
PC11	-	EVENTOUT	TIM19_CH2	-	-	-	SPI3_MISO/I2S3_MCK	USART3_RX
PC12	-	EVENTOUT	TIM19_CH3	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK
PC13	-	-	-	-	-	-	-	-
PC14	-	-	-	-	-	-	-	-
PC15	-	-	-	-	-	-	-	-

On-chip peripheral current consumption

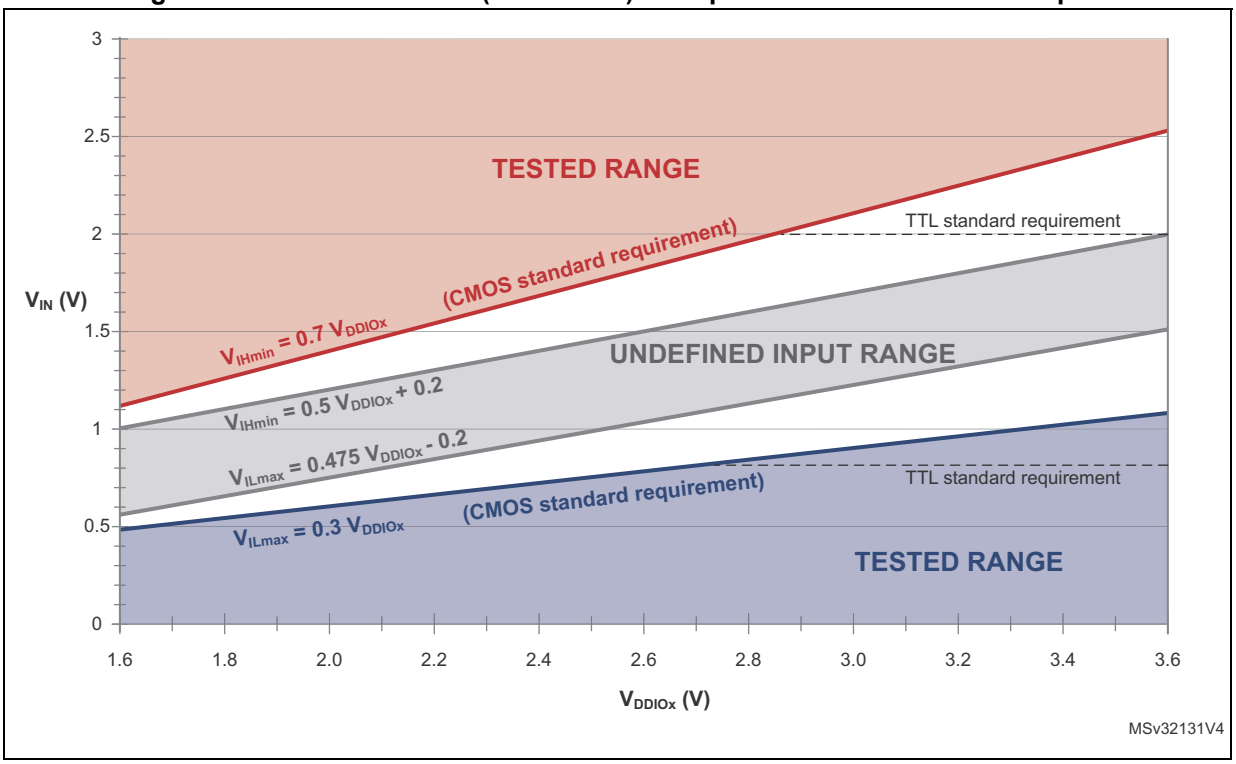
The MCU is placed under the following conditions:

- All I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off;
  - with only one peripheral clocked on.
- Ambient operating temperature at 25°C and V_{DD} = V_{DDA}= 3.3 Volts.

Table 36. Peripheral current consumption

Peripheral	Typical consumption(1)	Unit
AHB peripherals		-
BusMatrix(2)	6.9	µA/MHz
DMA1	18.3	
DMA2	4.8	
CRC	2.6	
GPIOA	12.2	
GPIOB	11.9	
GPIOC	4.3	
GPIOD	12.0	
GPIOE	4.4	
GPIOF	3.7	
TSC	5.7	
APB2 peripherals		
APB2-Bridge(3)	4.2	
SYSCFG & COMP	2.8	
ADC1	17.7	
SPI1	12.3	
USART1	22.9	
TIM15	15.7	
TIM16	12.2	
TIM17	12.1	
TIM19	18.5	
SDAC1	10.8	
SDAC2	10.5	
SDAC3	10.3	

Figure 18. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on all VDD_x and VDDSDx, plus the maximum Run consumption of the MCU sourced on V_{DD} cannot exceed the absolute maximum rating SI_{VDD} (see *Table 20*).
- The sum of the currents sunk by all the I/Os on all VSS_x and VSSSD, plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating SI_{VSS} (see *Table 20*).

Table 59. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
DuCy(SCK)(1)	I2S slave input clock duty cycle	Slave mode	30	70	%
f_{CK}(1) $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.528	1.539	MHz
		Slave mode	0	12.288	
$t_{r(CK)}$(1) $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 30 pF	-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode	4	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	4	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode	2	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode	-	-	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$ (1)	I2S clock low time		312	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$ (1)		Slave receiver	3	-	
$t_{h(SD\_MR)}$(1)	Data input hold time	Master receiver	1.5	-	
$t_{h(SD\_SR)}$ (1)		Slave receiver	1.5	-	
$t_{v(SD\_ST)}$ (1)	Data output valid time	Slave transmitter (after enable edge)	-	16	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	16	-	
$t_{v(SD\_MT)}$ (1)	Data output valid time	Master transmitter (after enable edge)	-	2	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. Guaranteed by characterization results.

Equation 1: R_{SRC} max formula

$$R_{SRC} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external signal source impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 61. R_{SRC} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{SRC} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	50
239.5	17.1	50

1. Guaranteed by design.

Table 62. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C	±1.3	±3	LSB
EO	Offset error		±1	±2	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V, T_A = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{ADC} = 14 MHz, R_{SRC} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V, T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

6.3.20 Temperature sensor characteristics

Table 65. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ± 5 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ± 5 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

Table 66. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4	-	10	µs
T_{S_temp}(2)(1)	ADC sampling time when reading the temperature	17.1	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.21 V_{BAT} monitoring characteristics

Table 67. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	-1	-	+1	%
T_{S_vbat}(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.22 Timer characteristics

The parameters given in *Table 68* are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

6.3.23 USB characteristics

Table 71. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 72. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage(2)	-	3.0(3)	3.6	V
V_{DI}(4)	Differential input sensitivity (for USB compliance)	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(4)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USB_DP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F3xxx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design.
5. R_L is the load connected on the USB drivers

Figure 31. USB timings: definition of data signal rise and fall time

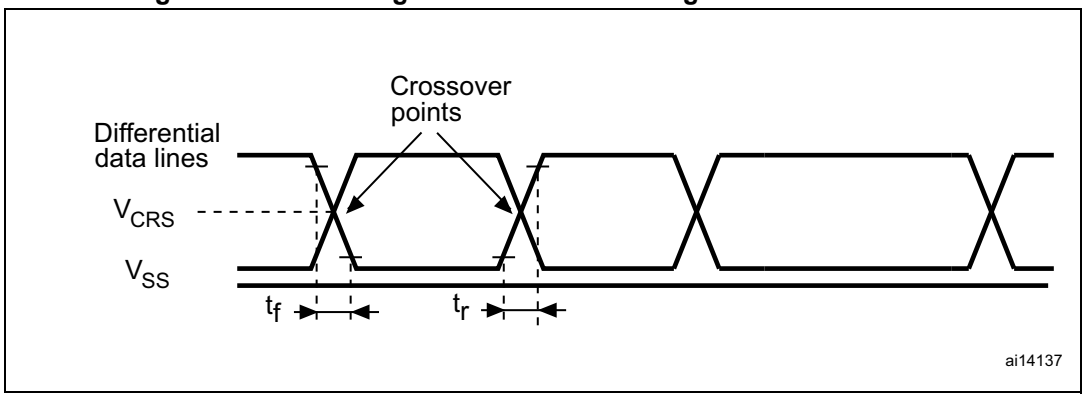


Table 73. USB: Full-speed electrical characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver characteristics						
t_r	Rise time(2)	C_L = 50 pF	4	-	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	-	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	-	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	-	2.0	V
Output driver Impedance(3)	Z_{DRV}	driving high and low	28	40	44	Ω

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-), the matching impedance is already included in the embedded driver.

6.3.24 CAN (controller area network) interface

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

6.3.25 SDADC characteristics

Table 74. SDADC characteristics (1)

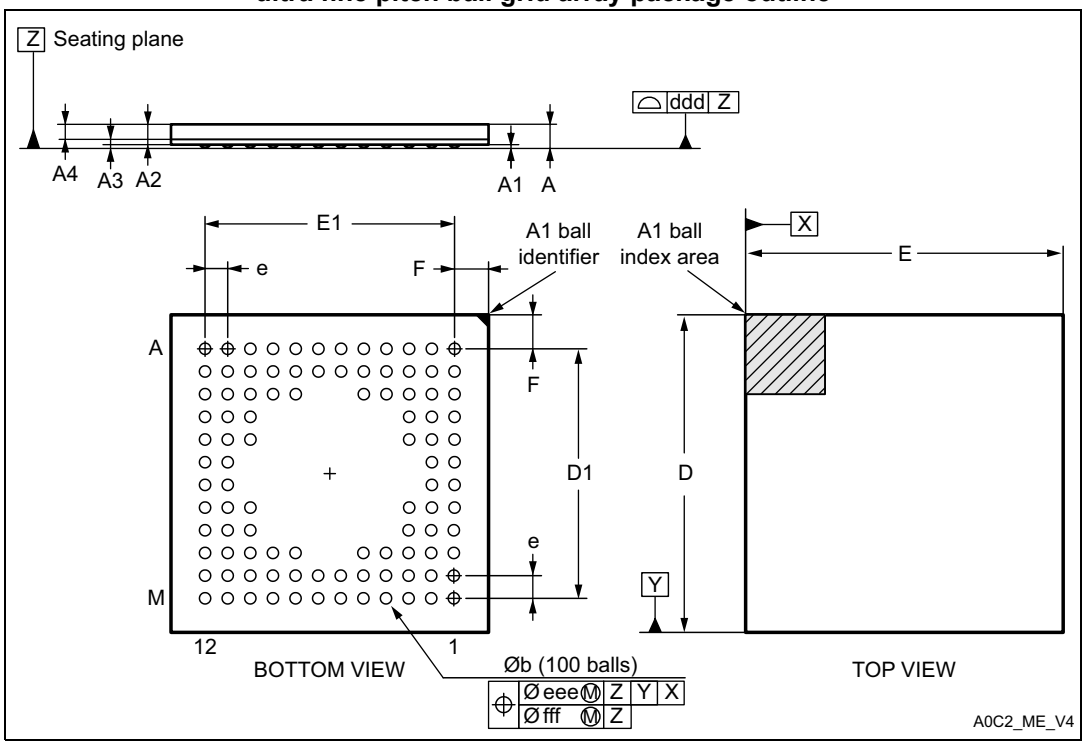
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Note
V_{DDSDx}	Power supply	Slow mode (f_{ADC} = 1.5 MHz)	2.2	-	V_{DDA}	V	-
		Normal mode (f_{ADC} = 6 MHz)	2.4	-	V_{DDA}		-
f_{ADC}	SDADC clock frequency	Slow mode (f_{ADC} = 1.5 MHz)	0.5	1.5	1.65	MHz	-
		Normal mode (f_{ADC} = 6 MHz)	0.5	6	6.3		-
V_{REFSD+}	Positive ref. voltage	-	1.1	-	V_{DDSDx}	V	-

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 UFBGA100 package information

Figure 32. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



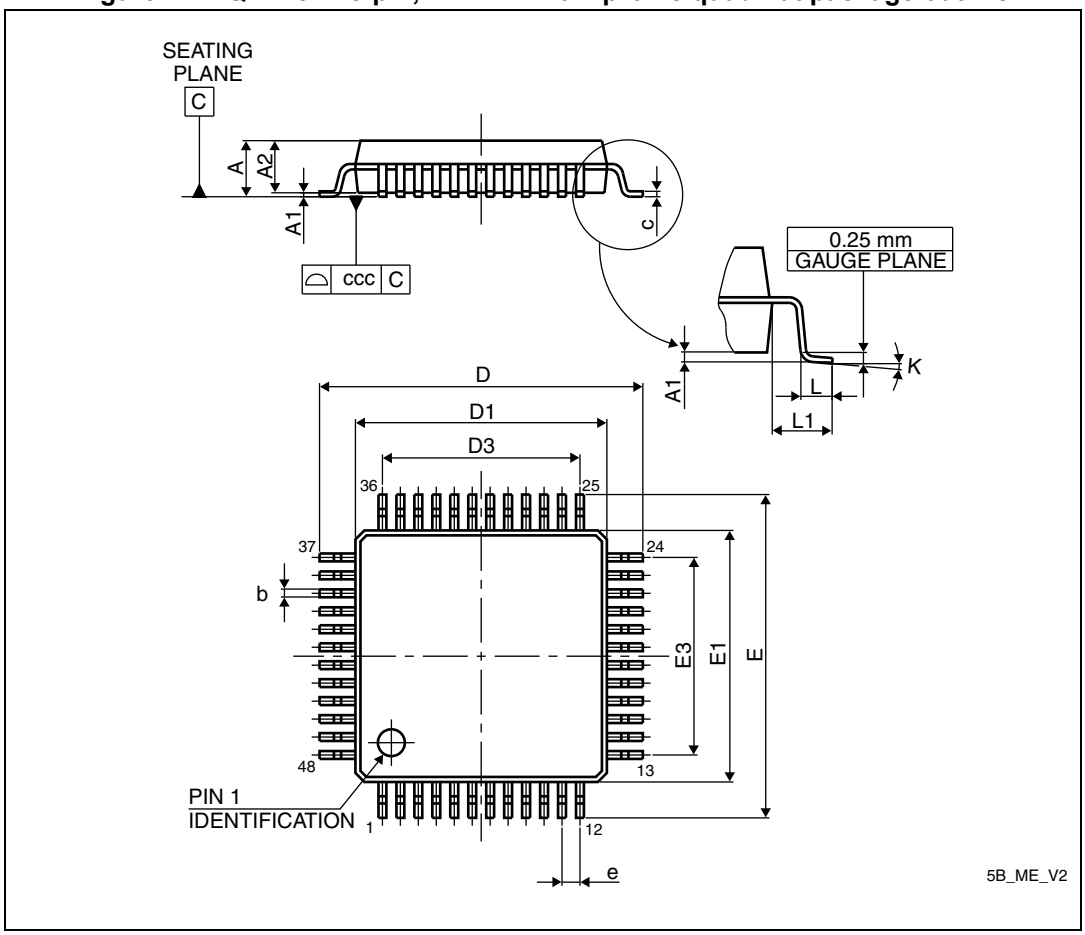
1. Drawing is not to scale.

Table 76. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.200	0.250	0.300	0.0079	0.0098	0.0118

7.4 LQFP48 package information

Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Using the values obtained in *Table 81* T_{Jmax} is calculated as follows:

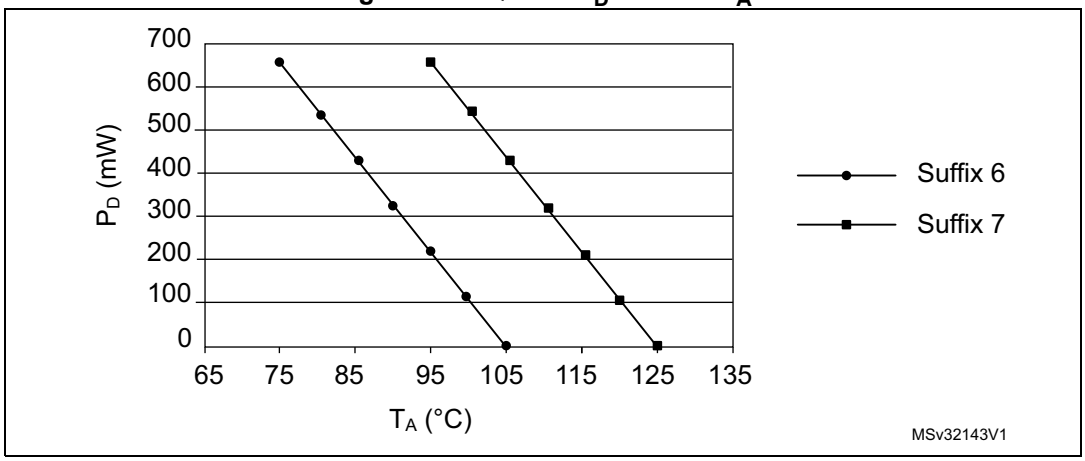
– For LQFP100, 46°C/W

T_{Jmax} = 115 °C + (46°C/W × 98.8 mW) = 115 °C + 4.54 °C = 119.5 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*).

Figure 44. LQFP64 P_D max vs. T_A



8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 82. Ordering information scheme

Example: STM32 F 373 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

373 = STM32F373xx

Pin count

C = 48 pins

R = 64 pins

V = 100 pins

Code size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

H = BGA

Temperature range

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

Options

xxx = programmed parts

TR = tape and reel

Table 83. Document revision history (continued)

Date	Revision	Changes
07-Sep-2012	2 (cont'd)	Filled values in *Table 70: WWDG min-max timeout value @72 MHz (PCLK)* Filled values in *Table 58: SPI characteristics* Filled values in *Table 59: I2S characteristics* Replaced *Table 60: ADC characteristics* Added values in *Table 74: SDADC characteristics* Modified footnote in *Table 75: VREFSD+ pin characteristics* Replaced 'AIN' with 'SRC' in *Table 61: RSRC max for fADC = 14 MHz* and *Figure 28: Typical connection diagram using the ADC* Reordered chapters and Cover page features. Added subsection to GPIOS in *Table 2: Device overview* Aligned SRAM with USB in *Figure 1: Block diagram* Added "Do not reconfigure..." sentence in *Section 3.9: General-purpose input/outputs (GPIOs)* Added *Table 7: STM32F373xx I2C implementation* Added *Table 8: STM32F373xx USART implementation* Merged SPI and I2S into one section Reshaped *Figure 5: STM32F373xx UFBGA100 ballout* and removed ADC10 Added notes column, modified I/O structure values and pin, function names, removed TIM1_TX & TIM1_RX in *Table 11: STM32F373xx pin definitions* Added the note "do not reconfigure..." after *Table 11: STM32F373xx pin definitions* Modified "x_CK" occurrences to "I2Sx_CK" in *Table 12: Alternate functions for port PA* to *Table 17: Alternate functions for port PF* Added two GP I/Os in *Figure 9: Power supply scheme* Added Caution after *Figure 9: Power supply scheme* Added Max values in *Table 23: Operating conditions at power-up / power-down* Modified (1) footnote in *Table 24: Embedded reset and power control block characteristics* Added row to *Table 27: Embedded internal reference voltage* Added the note " It is recommended..." under *Table 51: I/O current injection susceptibility* Modified *Table 51: I/O current injection susceptibility* Modified temperature and current values in *Section 7.5.2: Selecting the product temperature range* Added crystal EPSON-TOYOCOM bullet under *Typical current consumption* Modified *Figure 9: Power supply scheme* Removed Boot 0 section Modified *Table 73: USB: Full-speed electrical characteristics*