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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 24K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 1x12b, 3x16b; D/A 3x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f373rbt6 |

# List of tables

# 1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F373xx microcontrollers.

This STM32F373xx datasheet should be read in conjunction with the RM0313 reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the Cortex®-M4 with FPU core, please refer to:

- Cortex®-M4 with FPU Technical Reference Manual, available from www.arm.com.
- STM32F3xxx and STM32F4xxx Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

Table 7. STM32F373xx I²C implementation (continued)

| I²C features(1) | I2C1 | I2C2 |
|---|---|---|
| SMBus | X | X |
| Wakeup from STOP | X | X |

1. X = supported.

## 3.20 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32F373xx embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3).

All USARTs interfaces are able to communicate at speeds of up to 9 Mbit/s.

They provide hardware management of the CTS and RTS signals, they support IrDA SIR ENDEC, the multiprocessor communication mode, the single-wire half-duplex communication mode, Smartcard mode (ISO/IEC 7816 compliant), autobaudrate feature and have LIN Master/Slave capability. The USART interfaces can be served by the DMA controller.

Refer to *Table 8* for the features of USART1, USART2 and USART3.

Table 8. STM32F373xx USART implementation

| USART modes/features(1) | USART1 | USART2 | USART3 |
|---|---|---|---|
| Hardware flow control for modem | X | X | X |
| Continuous communication using DMA | X | X | X |
| Multiprocessor communication | X | X | X |
| Synchronous mode | X | X | X |
| Smartcard mode | X | X | X |
| Single-wire half-duplex communication | X | X | X |
| IrDA SIR ENDEC block | X | X | X |
| LIN mode | X | X | X |
| Dual clock domain and wakeup from Stop mode | X | X | X |
| Receiver timeout interrupt | X | X | X |
| Modbus communication | X | X | X |
| Auto baud rate detection | X | X | X |
| Driver Enable | X | X | X |

1. X = supported.

## 3.24 Universal serial bus (USB)

The STM32F373xx embeds an USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

## 3.25 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

## 3.26 Embedded trace macrocell™

The ARM embedded trace macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F373xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

**Figure 4. STM32F373xx LQFP100 pinout**

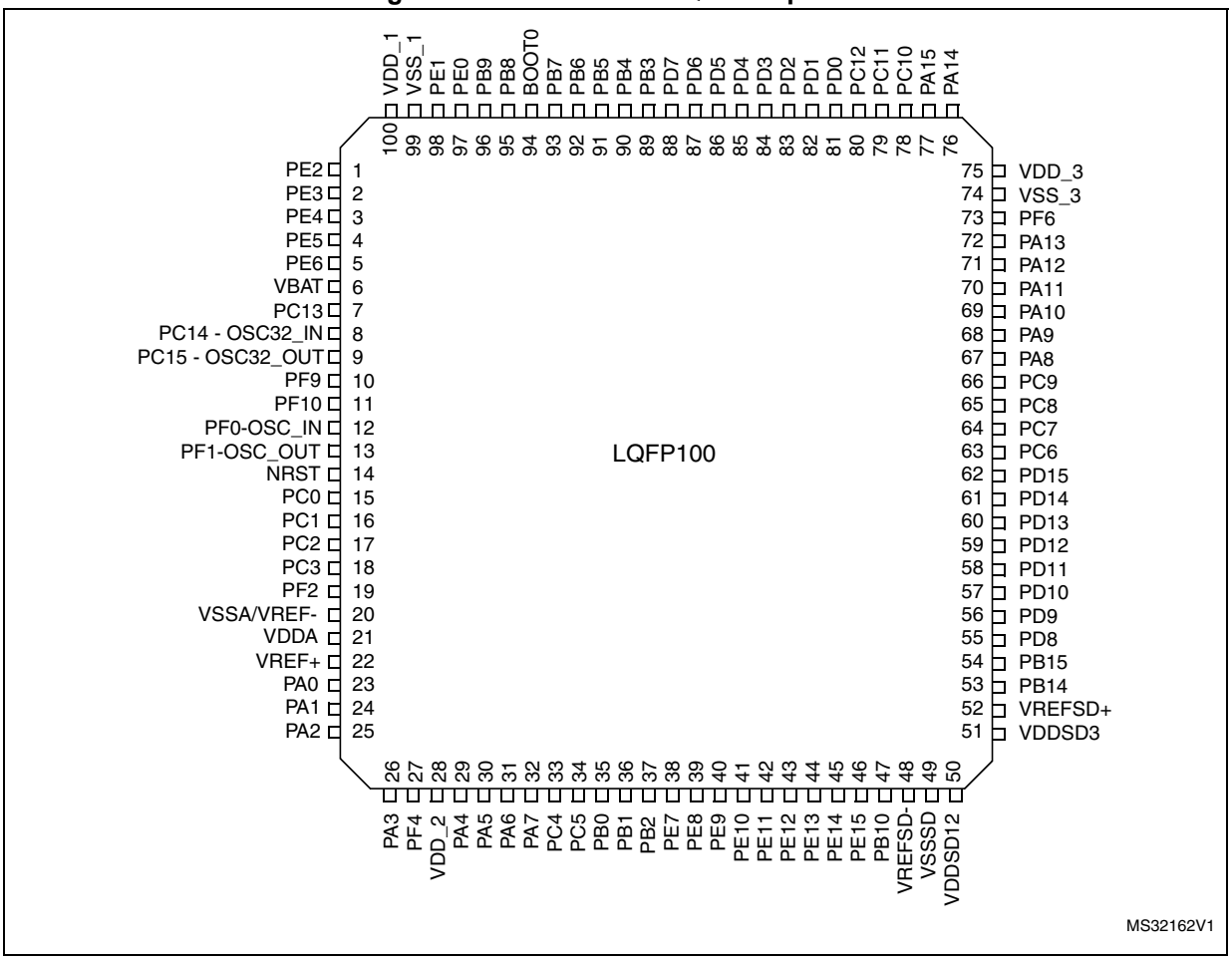
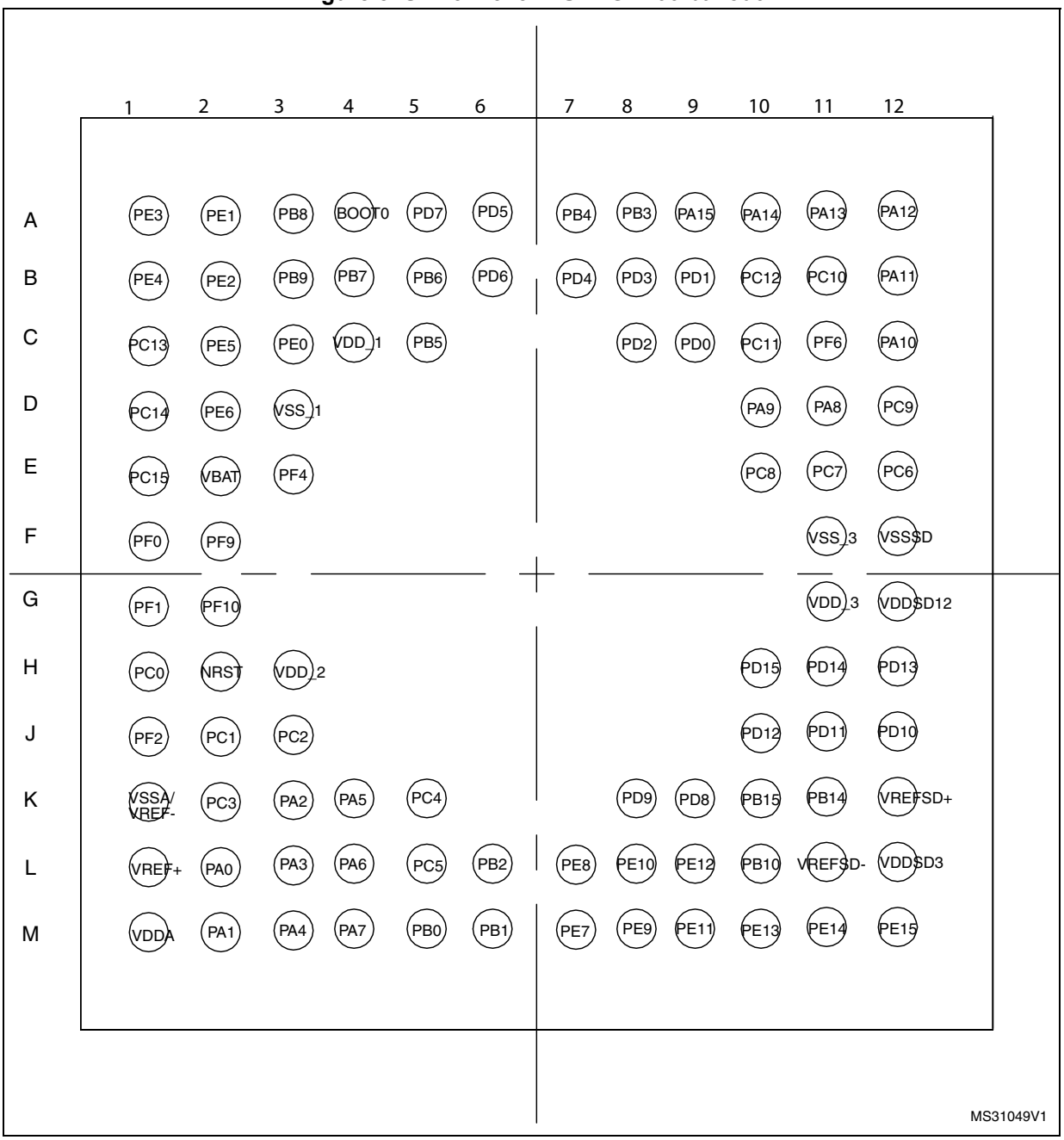


**Figure 5. STM32F373xx UFBGA100 ballout**




1. The above figure shows the package top view.

Table 11. STM32F373xx pin definitions (continued)

| Pin numbers | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | UFBGA100 | LQFP64 | LQFP48 | | | | | Alternate function | Additional functions |
| 51 | L12 | - | - | VDDSD3 | S | - | (2) | SDADC3 power supply | |
| 52 | K12 | 33 | 25 | VREFSD+ | S | - | - | External reference voltage for SDADC1, SDADC2, SDADC3 (positive input) | |
| 53 | K11 | 34 | 26 | PB14 | I/O | TC | (4) | SPI2_MISO/I2S2_MCK, USART3_RTS, TIM15_CH1, TIM12_CH1, TSC_G6_IO1 | SDADC3_AIN8P |
| 54 | K10 | 35 | 27 | PB15 | I/O | TC | (4) | SPI2_MOSI/I2S2_SD, TIM15_CH1N, TIM15_CH2, TIM12_CH2, TSC_G6_IO2, RTC_REFIN | SDADC3_AIN7P, SDADC3_AIN8M |
| 55 | K9 | 36 | 28 | PD8 | I/O | TC | (4) | SPI2_SCK/I2S2_CK, USART3_TX, TSC_G6_IO3 | SDADC3_AIN6P |
| 56 | K8 | - | - | PD9 | I/O | TC | (4) (2) | USART3_RX, TSC_G6_IO4 | SDADC3_AIN5P, SDADC3_AIN6M |
| 57 | J12 | - | - | PD10 | I/O | TC | (4) (2) | USART3_CK | SDADC3_AIN4P |
| 58 | J11 | - | - | PD11 | I/O | TC | (4) (2) | USART3_CTS | SDADC3_AIN3P, SDADC3_AIN4M |
| 59 | J10 | - | - | PD12 | I/O | TC | (4) (2) | USART3_RTS, TIM4_CH1, TSC_G8_IO1 | SDADC3_AIN2P |
| 60 | H12 | - | - | PD13 | I/O | TC | (4) (2) | TIM4_CH2, TSC_G8_IO2 | SDADC3_AIN1P, SDADC3_AIN2M |
| 61 | H11 | - | - | PD14 | I/O | TC | (4) (2) | TIM4_CH3, TSC_G8_IO3 | SDADC3_AIN0P |
| 62 | H10 | - | - | PD15 | I/O | TC | (4) (2) | TIM4_CH4, TSC_G8_IO4 | SDADC3_AIN0M |
| 63 | E12 | 37 | - | PC6 | I/O | FT | (2) | TIM3_CH1, SPI1_NSS/I2S1_WS | - |
| 64 | E11 | 38 | - | PC7 | I/O | FT | (2) | TIM3_CH2, SPI1_SCK/I2S1_CK, | - |
| 65 | E10 | 39 | - | PC8 | I/O | FT | (2) | SPI1_MISO/I2S1_MCK, TIM3_CH3 | - |
| 66 | D12 | 40 | - | PC9 | I/O | FT | (2) | SPI1_MOSI/I2S1_SD, TIM3_CH4 | - |

**Table 13. Alternate functions for port PB**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PB0 | - | - | TIM3_CH3 | TSC_ G3_IO3 | - | SPI_MOSI/ I2S1_SD | - | - | - | - | TIM3_ CH2 | - | EVENTOUT |
| PB1 | - | - | TIM3_CH4 | TSC_ G3_IO4 | - | - | - | - | - | - | - | - | EVENTOUT |
| PB2 | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| PB3 | JTDO-TRACESWO | TIM2_ CH2 | TIM4_ETR | TSC_ G5_IO1 | - | SPI1_SCK/ I2S1_CK | SPI3_SCK/ I2S3_CK | USART2_TX | - | TIM13_ CH1 | TIM3_ ETR | - | EVENTOUT |
| PB4 | NJTRST | TIM16_ CH1 | TIM3_CH1 | TSC_ G5_IO2 | - | SPI1_MISO /I2S1_MCK | SPI3_MISO/ I2S3_MCK | USART2_RX | - | TIM15_ CH1N | TIM17 _BKIN | - | EVENTOUT |
| PB5 | - | TIM16_ BKIN | TIM3_CH2 | - | I2C1_ SMBA | SPI1_MOSI /I2S1_SD | SPI3_MOSI /I2S3_SD | USART2_CK | - | - | TIM17 _CH1 | TIM19 _ETR | EVENTOUT |
| PB6 | - | TIM16_ CH1N | TIM4_CH1 | TSC_ G5_IO3 | I2C1_ SCL | - | - | USART1_TX | - | TIM15_ CH1 | TIM3_ CH3 | TIM19 _CH1 | EVENTOUT |
| PB7 | - | TIM17_ CH1N | TIM4_CH2 | TSC_ G5_IO4 | I2C1_ SDA | - | - | USART1_RX | - | TIM15_ CH2 | TIM3_ CH4 | TIM19 _CH2 | EVENTOUT |
| PB8 | - | TIM16_ CH1 | TIM4_CH3 | TSC_ SYNC | I2C1_ SCL | SPI2_SCK/ I2S2_CK | CEC | USART3_TX | COMP1 _OUT | CAN_ RX | - | TIM19 _CH3 | EVENTOUT |
| PB9 | - | TIM17_ CH1 | TIM4_CH4 | - | I2C1_ SDA | SPI2_NSS/ I2S2_WS | IR-OUT | USART3_RX | COMP2 _OUT | CAN_ TX | - | TIM19 _CH4 | EVENTOUT |
| PB10 | - | TIM2_ CH3 | - | TSC_ SYNCH | - | SPI2_SCK/ I2S2_CK | CEC | USART3_TX | - | - | - | - | EVENTOUT |
| PB14 | - | TIM15_ CH1 | - | TSC_ G6_IO1 | - | SPI2_MISO /I2S2_MCK | - | USART3_RTS | - | TIM12_ CH1 | - | - | EVENTOUT |
| PB15 | RTC_REFIN | TIM15_ CH2 | TIM15_ CH1N | TSC_ G6_IO2 | - | SPI2_MOSI /I2S2_SD | - | - | - | TIM12_ CH2 | - | - | EVENTOUT |

**Table 15. Alternate functions for port PD**

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|---|---|---|---|---|---|---|---|---|
| PD0 | - | EVENTOUT | TIM19_CH4 | - | - | - | - | CAN_RX |
| PD1 | - | EVENTOUT | TIM19_ETR | - | - | - | - | CAN_TX |
| PD2 | - | EVENTOUT | TIM3_ETR | - | - | - | - | - |
| PD3 | - | EVENTOUT | - | - | - | SPI2_MISO/I2S2_MCK | - | USART2_CTS |
| PD4 | - | EVENTOUT | - | - | - | SPI2_MOSI/I2S2_SD | - | USART2_RTS |
| PD5 | - | EVENTOUT | - | - | - | - | - | USART2_TX |
| PD6 | - | EVENTOUT | - | - | - | SPI2_NSS/I2S2_WS | - | USART2_RX |
| PD7 | - | EVENTOUT | - | - | - | SPI2_SCK/I2S2_CK | - | USART2_CK |
| PD8 | - | EVENTOUT | - | TSC_G6_IO3 | - | SPI2_SCK/I2S2_CK | - | USART3_TX |
| PD9 | - | EVENTOUT | - | TSC_G6_IO4 | - | - | - | USART3_RX |
| PD10 | - | EVENTOUT | - | - | - | - | - | USART3_CK |
| PD11 | - | EVENTOUT | - | - | - | - | - | USART3_CTS |
| PD12 | - | EVENTOUT | TIM4_CH1 | TSC_G8_IO1 | - | - | - | USART3_RTS |
| PD13 | - | EVENTOUT | TIM4_CH2 | TSC_G8_IO2 | - | - | - | - |
| PD14 | - | EVENTOUT | TIM4_CH3 | TSC_G8_IO3 | - | - | - | - |
| PD15 | - | EVENTOUT | TIM4_CH4 | TSC_G8_IO4 | - | - | - | - |

**Table 34. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ | | Unit |
|---|---|---|---|---|---|---|
| | | | | Peripherals enabled | Peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode from $V_{DD}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on | 72 MHz | 42.8 | 6.9 | mA |
| | | | 64 MHz | 38.2 | 6.2 | |
| | | | 48 MHz | 28.9 | 4.8 | |
| | | | 32 MHz | 19.5 | 3.4 | |
| | | | 24 MHz | 14.7 | 2.7 | |
| | | | 16 MHz | 10.2 | 2.0 | |
| | | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off | 8 MHz | 5.2 | 1.2 | |
| | | | 4 MHz | 3.4 | 1.1 | |
| | | | 2 MHz | 2.2 | 0.9 | |
| | | | 1 MHz | 1.6 | 0.9 | |
| | | | 500 kHz | 1.4 | 0.8 | |
| | | | 125 kHz | 1.1 | 0.8 | |
| $I_{DDA}$(1) | Supply current in Sleep mode from $V_{DDA}$ supply | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL on | 72 MHz | 242.9 | 241.5 | µA |
| | | | 64 MHz | 213.7 | 212.7 | |
| | | | 48 MHz | 158.8 | 158.0 | |
| | | | 32 MHz | 107.6 | 107.3 | |
| | | | 24 MHz | 82.7 | 82.6 | |
| | | | 16 MHz | 58.3 | 58.2 | |
| | | Running from HSE crystal clock 8 MHz, code executing from Flash or RAM, PLL off | 8 MHz | 1.2 | 1.2 | |
| | | | 4 MHz | 1.2 | 1.2 | |
| | | | 2 MHz | 1.2 | 1.2 | |
| | | | 1 MHz | 1.2 | 1.2 | |
| | | | 500 kHz | 1.2 | 1.2 | |
| | | | 125 kHz | 1.2 | 1.2 | |

1. $V_{DDA}$ monitoring is off, $V_{DDSD12}$ monitoring is off.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 50. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset occurrence or oscillator frequency deviation).

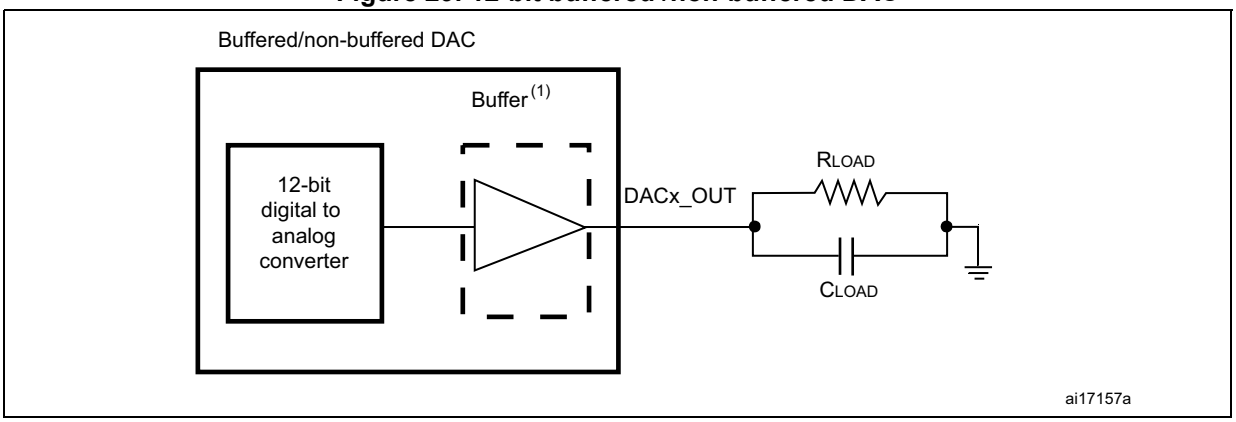
The test results are given in *Table 51*.

**Table 63. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Offset(3) | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}$/2) | - | - | - | ±10 | mV |
| | | Given for the DAC in 10-bit at $V_{REF+}$ = 3.6 V | - | - | ±3 | LSB |
| | | Given for the DAC in 12-bit at $V_{REF+}$ = 3.6 V | - | - | ±12 | LSB |
| Gain error(3) | Gain error | Given for the DAC in 12bit configuration | - | - | ±0.5 | % |
| $t_{SETTLING}$(3) | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ | - | 3 | 4 | µs |
| Update rate(3) | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ | - | - | 1 | MS/s |
| $t_{WAKEUP}$(3) | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. | - | 6.5 | 10 | µs |
| PSRR+ (1) | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement | No $R_{LOAD}$, $C_{LOAD}$ = 50 pF | - | -67 | -40 | dB |

1. Guaranteed by design.
2. Quiescent mode refers to the state of the DAC keeping a steady value on the output, so no dynamic consumption is involved.
3. Guaranteed by characterization.

**Figure 29. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

**Table 74. SDADC characteristics (continued)(1)**

| Symbol | Parameter | Conditions | | | | | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| EO | Offset error | Differential mode | gain = 1 | $f_{ADC}$ = 1.5 MHz | $V_{DDSDx}$ = 3.3 | $V_{REFSD+}$ = 3.3 | - | - | 110 | uV | after offset calibration |
| | | | | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$ = 1.2 | - | - | 110 | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | - | - | 100 | | |
| | | | gain = 8 | $f_{ADC}$ = 6 MHz | | $V_{REFSD+}$ = 1.2 | - | - | 70 | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | - | - | 100 | | |
| | | | | $f_{ADC}$ = 1.5 MHz | | $V_{REFSD+}$ = 3.3 | - | - | 90 | | |
| | | Single ended mode | gain = 1 | - | | $V_{REFSD+}$ = 1.2 | - | - | 2100 | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | - | - | 2000 | | |
| | | | gain = 8 | | | $V_{REFSD+}$ = 1.2 | - | - | 1500 | | |
| | | | | | | $V_{REFSD+}$ = 3.3 | - | - | 1800 | | |
| $D_{voffsettemp}$ | Offset drift with temperature | Differential or single ended mode, gain = 1, $V_{DDSDx}$ = 3.3 V | | | | | - | 10 | 15 | uV/K | - |
| EG | Gain error | All gains, differential mode, single ended mode | | | | | -2.4 | -2.7 | -3.1 | % | negative gain error = data result are greater than ideal |
| EGT | Gain drift with temperature | gain = 1, differential mode, single ended mode | | | | | - | 0 | - | ppm /K | - |

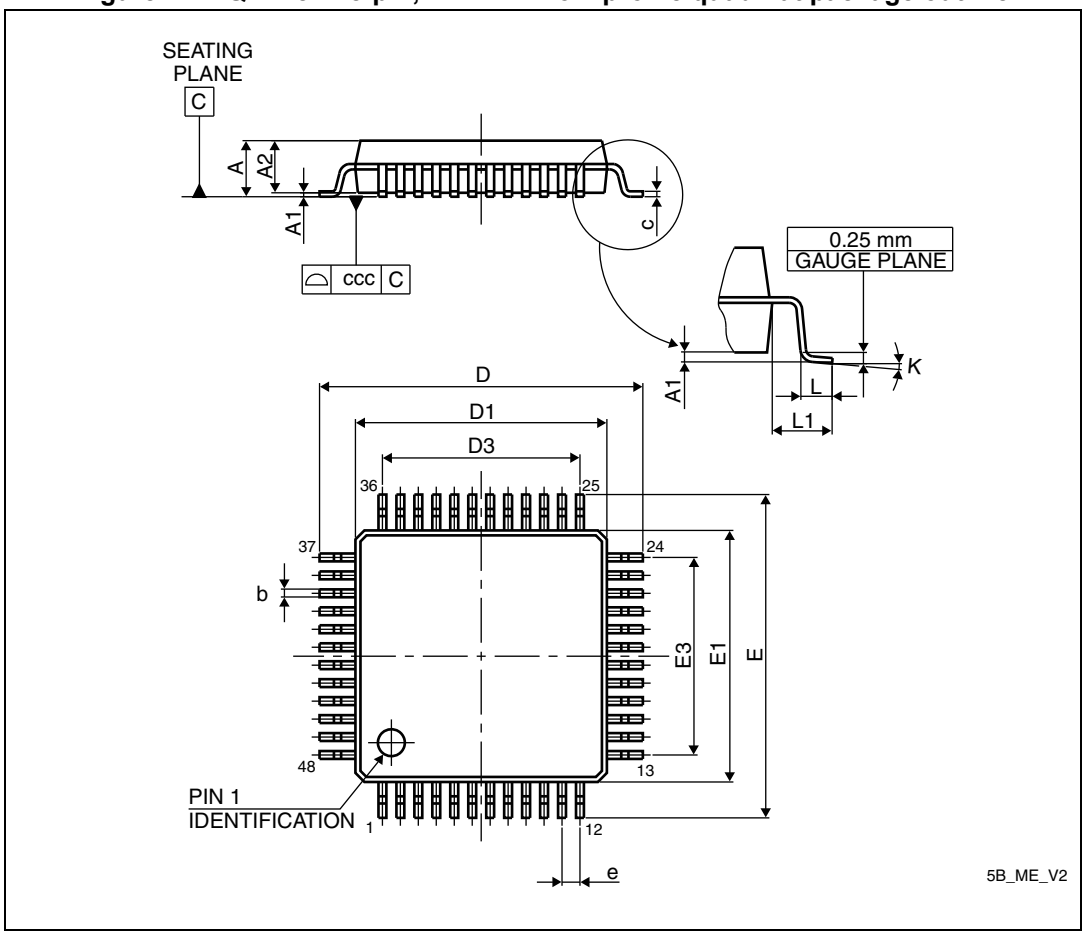
**Table 79. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 7.4 LQFP48 package information

**Figure 41. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**



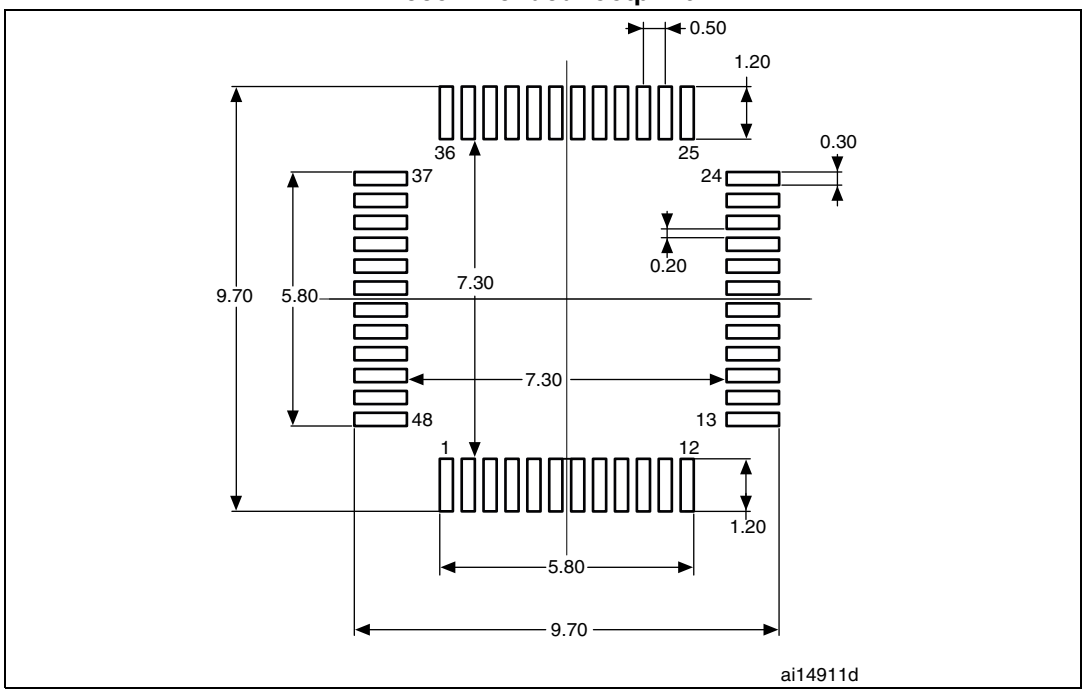

1. Drawing is not to scale.

**Table 80. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 42. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**

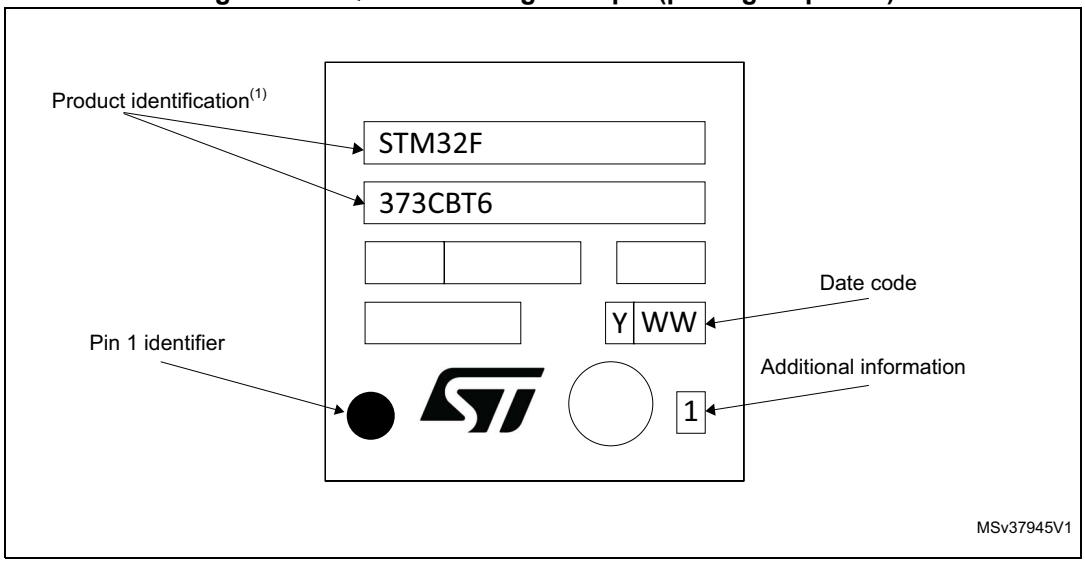



1. Dimensions are expressed in millimeters.

## Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 43. LQFP48 marking example (package top view)**




1. Samples marked “ES” are to be considered as “Engineering Samples”: i.e. they are intended to be sent to customer for electrical compatibility evaluation and may be used to start customer qualification where specifically authorized by ST in writing. In no event ST will be liable for any customer usage in production. Only if ST has authorized in writing the customer qualification Engineering Samples can be used for reliability qualification trials.

# 8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

**Table 82. Ordering information scheme**

**Example**: STM32 F 373 R 8 T 6 x

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = General-purpose

**Sub-family**

373 = STM32F373xx

**Pin count**

C = 48 pins

R = 64 pins

V = 100 pins

**Code size**

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

**Package**

T = LQFP

H = BGA

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C

7 = Industrial temperature range, –40 to 105 °C

**Options**

xxx = programmed parts

TR = tape and reel

# 9 Revision history

Table 83. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 18-Jun-2012 | 1 | Initial release. |
| 07-Sep-2012 | 2 | Added 'F' to all 'Cortex-M4' occurrences<br>Modified the shapes of *Figure 2: STM32F373xx LQFP48 pinout* to *Figure 4: STM32F373xx LQFP100 pinout*<br>Added two rows 'VREFSD+ - VDDSD3' and 'VREF+ - VDDA' in *Table 19: Voltage characteristics*<br>Removed PB0 in footnote of *Table 19: Voltage characteristics* and in *Section 6.3.14: I/O port characteristics*<br>Added a paragraph after '...power up sequence' in *Section 6.2: Absolute maximum ratings* and after '...in output mode' in *I/O system current consumption*<br>Corrected SDAC_VREF+ in *Figure 9: Power supply scheme*<br>Modified *Table 20: Current characteristics*<br>Added BGA100 in *Table 22: General operating conditions*<br>Added values in *Table 27: Embedded internal reference voltage*<br>Filled values in *Table 28: Typical and maximum current consumption from VDD supply at VDD = 3.6 V*<br>Filled values in *Table 29: Typical and maximum current consumption from VDDA supply*<br>Filled values in *Table 30: Typical and maximum VDD consumption in Stop and Standby modes*<br>Removed table: "Typical and maximum VDDA consumption in Stop modes"<br>Filled values in *Table 31: Typical and maximum VDDA consumption in Stop and Standby modes*<br>Added VBAT values in *Table 32: Typical and maximum current consumption from VBAT supply*<br>Added typ values in *Table 33: Typical current consumption in Run mode, code with data processing running from Flash* and *Table 34: Typical current consumption in Sleep mode, code running from Flash or RAM*<br>Added max value in *Table 41: LSE oscillator characteristics (fLSE = 32.768 kHz)*<br>Modified min and max values in *Table 42: HSI oscillator characteristics*<br>Added values in *Table 37: Low-power mode wakeup timings*<br>Added Class values in *Table 47: EMS characteristics*<br>Modified values in *Table 48: EMI characteristics*<br>Added values in *Table 49: ESD absolute maximum ratings*<br>Added class value in *Table 50: Electrical sensitivities*<br>Modified values and descriptions in *Table 51: I/O current injection susceptibility* |